Audio precision

SYSTEM ONE

SERVICE MANUAL

Volume 1 of 2

Audio Precision System One Service Manual

This System One Service Manual has been distributed by Audio Precision as a courtesy, without warranty of any kind, free-of-charge to qualified technicians wishing to adjust, service and/or repair System One instruments. If you are unable to perform the desired service on your own, or prefer to have your System One instrument adjusted, serviced and/or repaired by Audio Precision, please contact the Audio Precision Technical Support department. They will provide you with pricing information and a Return Authorization Number prior to sending an instrument to the factory:

techsupport@audioprecision.com

1-800-231-7350

The System One is an obsolete product and has been out of production for over 3 years. Our stock of replacement parts is highly limited, and in some cases nearly depleted. Audio Precision will not be able to provide repair and adjustment services beyond December 31, 2007 unless pre-approved by the Service Manager.

Please be mindful that if you use this Service Manual to adjust, service and/or repair your own System One instrument, Audio Precision does not support or warrant its contents and/or use in any way.

Also, any reference to the term “Calibrate” or “Calibration” within this Service Manual does **not** constitute the ISO (International Standards Organization) definition of a calibration. The term “Calibrate” or “Calibration” within this Service Manual is used only to define “an adjustment to factory specification.”

SERVICE MANUAL

AUDIO PRECISION SYSTEM ONE

Revision 4.0
December 28, 1992

Copyright (C) 1988, 1991, 1992 by Audio Precision Inc.
PO Box 2209, Beaverton, Oregon 97075 USA
Telephone 503-627-0832
FAX 503-641-8906
Telex 283957 AUDIO UR

TABLE OF CONTENTS

SECTION 1 - GENERAL INFORMATION

This section contains general information about System One nomenclature, configurations and how to identify them, digital interface options, and the Audio Precision Interface Bus (APIB).

SECTION 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This service manual supports all versions and options of the Audio Precision **SYSTEM ONE**, the **SWR-122** family of switchers, the **DCX-127** multi-function interface accessory, and the **SIA-322** serial interface adapter.

All information is believed to be accurate as of the publication date. Please report any errors to Audio Precision, Box 2209, Beaverton Oregon 97075 (USA).

1.2 SYSTEM CONFIGURATIONS

System One is manufactured in eight standard configurations designated by the product nomenclature **SYS-xx** or **SYS-xxx**. The system configuration can be determined from the following desciptions, or from the connector panel figures shown on pages 1-2 to 1-5.

NOTE: The main signal connectors may differ from the XLR types shown in the figures without changing the system configuration.

SYS-22 Configuration

Dual channel generator and analyzer system. The upper left front panel contains the generator output connectors and the upper right front panel contains the analyzer input connectors. The lower left front panel contains three BNC connectors providing auxiliary signals from the generator. The lower right front panel contains five bnc connectors for monitoring the analyzer signals and connecting an external filter. Blank back panels.

SYS-11 Configuration

Single channel generator and analyzer system. Otherwise virtually identical to the SYS-22.

SYS-20 Configuration

Dual channel generator only system with identical functionality as the SYS-22. The upper right front panel contains a pair of 3-pin male XLR connectors to provide interconnection for the generator monitor function. If option "DSP" is installed, the upper right front panel will also contain a 7-pin male XLR connector to provide additional DSP related signal interconnections to a complementary SYS-202 or SYS-302. The lower right front panel is blank.

SYS-02 Configuration

Dual channel analyzer only system with identical functionality as the SYS-22. The upper left front panel contains a pair of female XLR connectors to provide interconnection to a SYS-20 for the generator monitor function. The lower left front panel is blank. The lower right front panel contains five bnc connectors, identical to the SYS-22 configuration.

SYS-222 Configuration

"System One + DSP". Dual channel generator and analyzer system including the digital signal processing module for FFTs and other specialized testing. The front panels are identical to the SYS-22 configuration except for the lower left panel which contains six bnc connectors. Blank back panels.

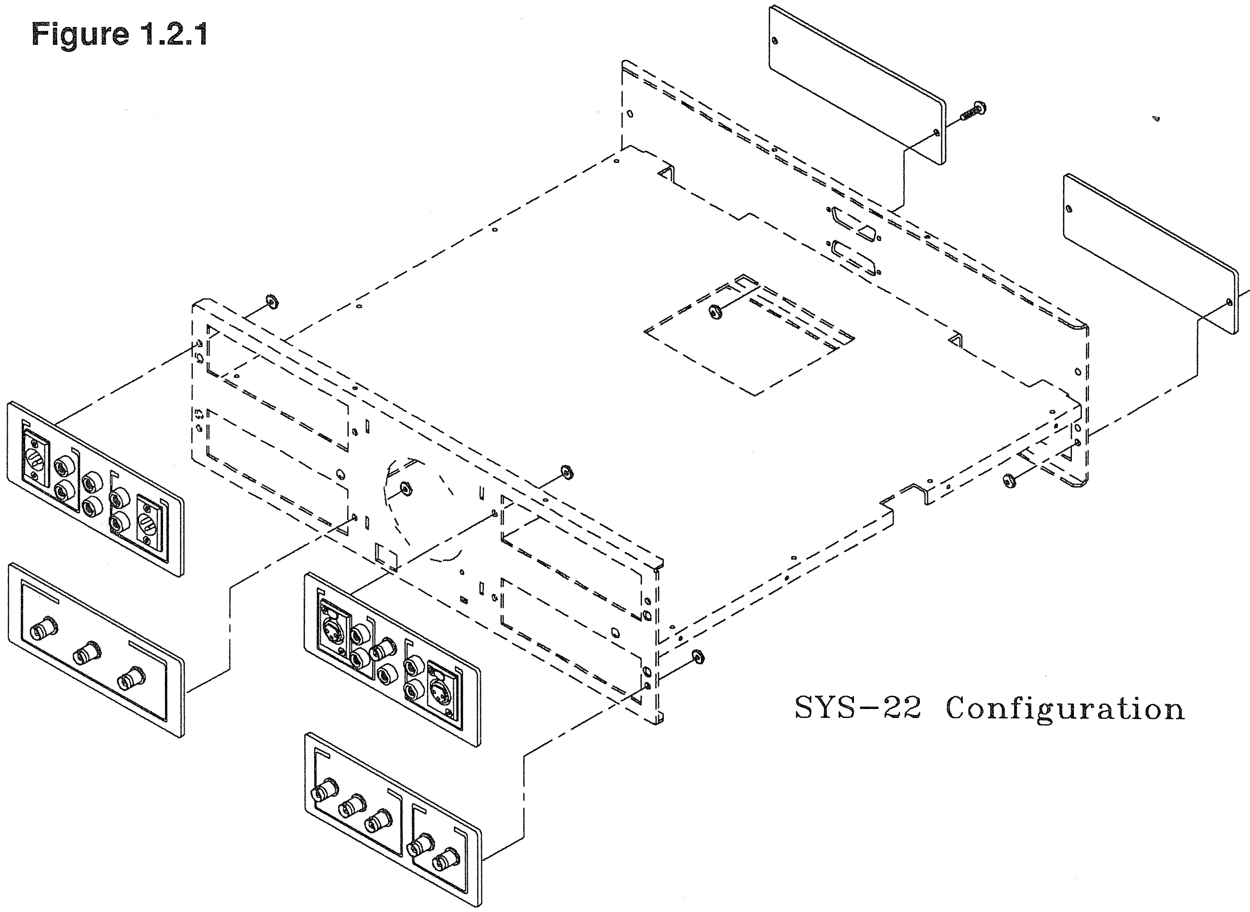
SYS-202 Configuration

Similar to the SYS-222 except the analog generator is deleted. The upper left front panel contains a pair of 3-pin female XLR connectors to provide interconnection to a SYS-20 for the generator monitor function plus a 7-pin female XLR for DSP related signals.

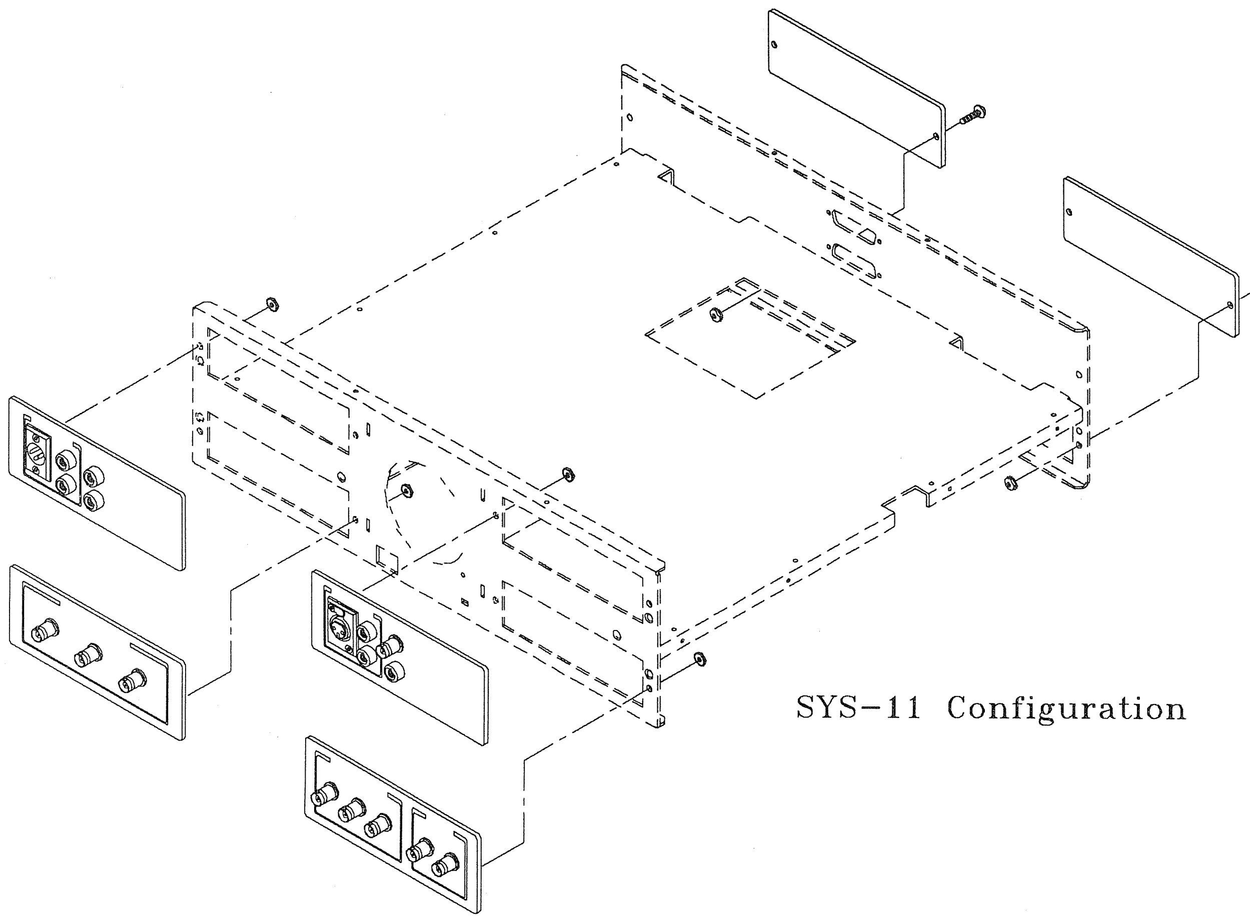
SYS-322 Configuration

"System One Dual Domain". Dual channel generator and analyzer system including the digital signal processing module for FFTs and other specialized testing, plus

Figure 1.2.1

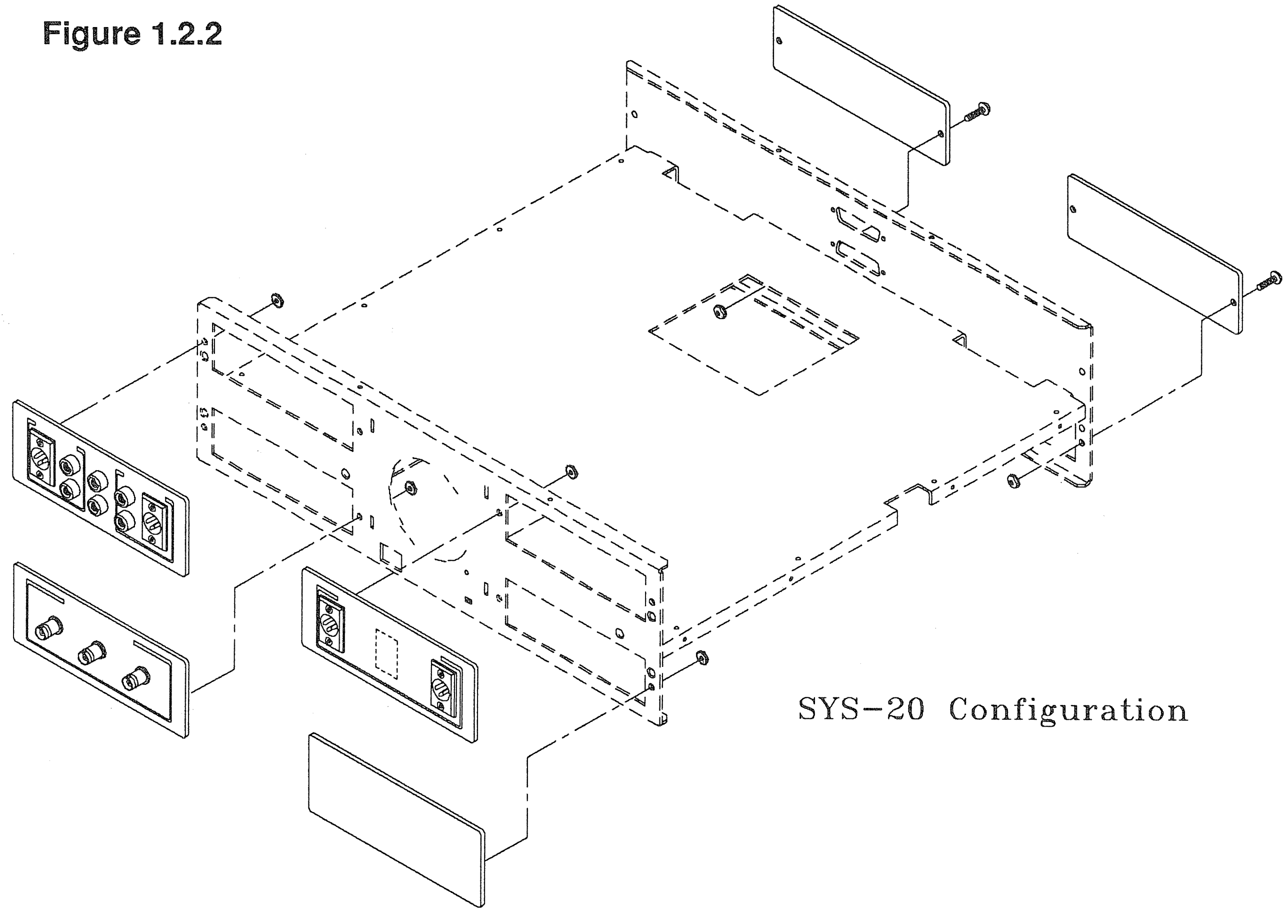


SYS-22 Configuration

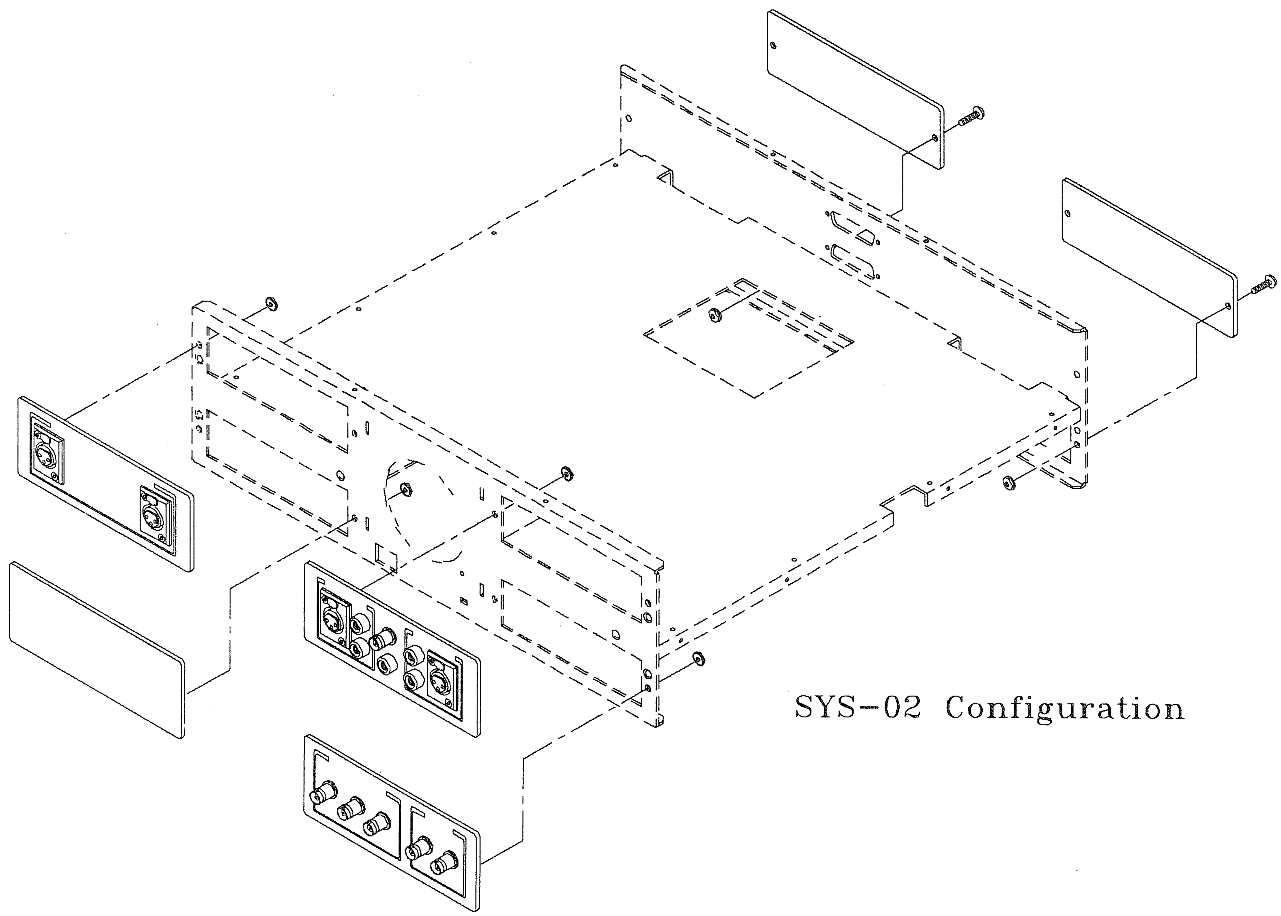


SYS-11 Configuration

Figure 1.2.2

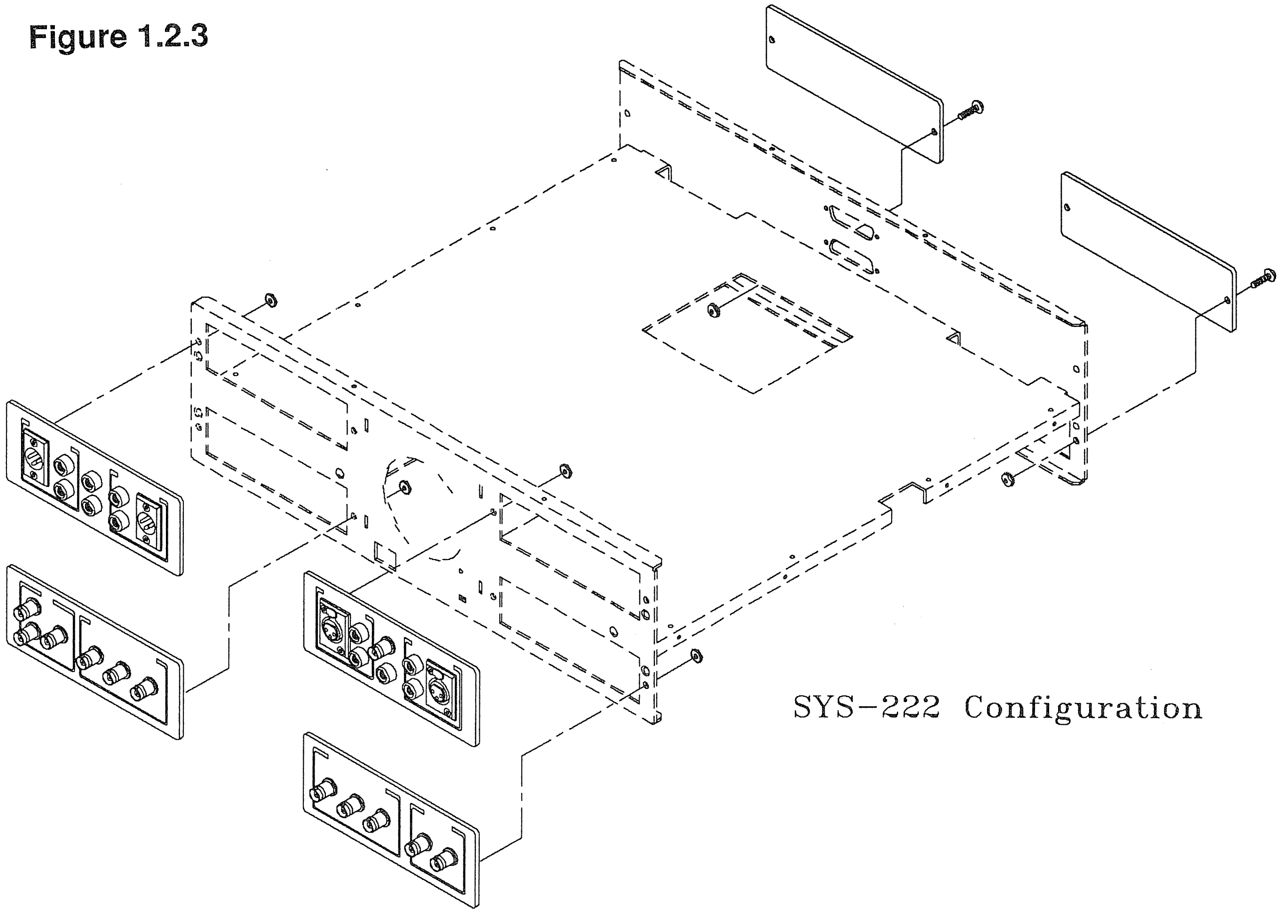


SYS−20 Configuration

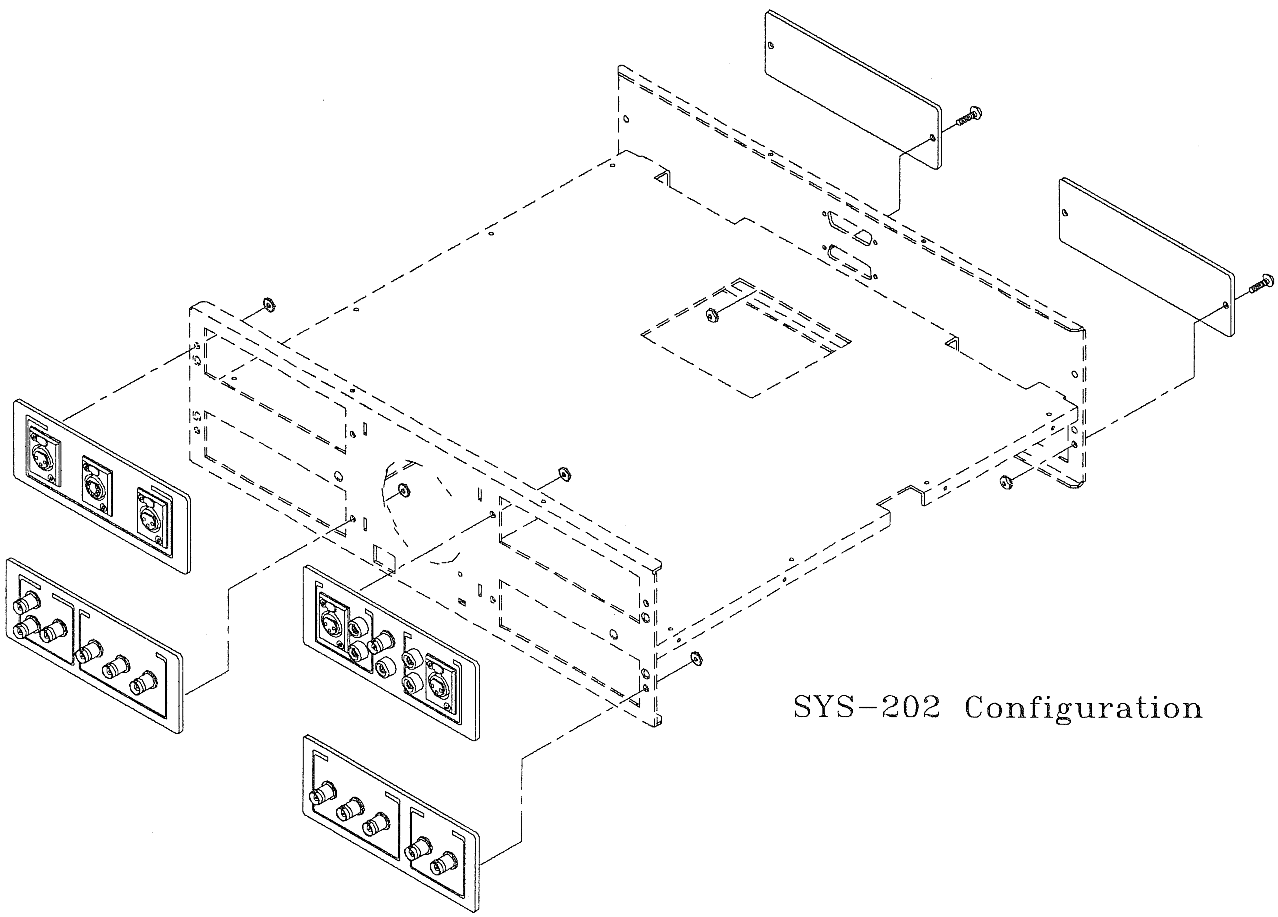


SYS−02 Configuration

Figure 1.2.3

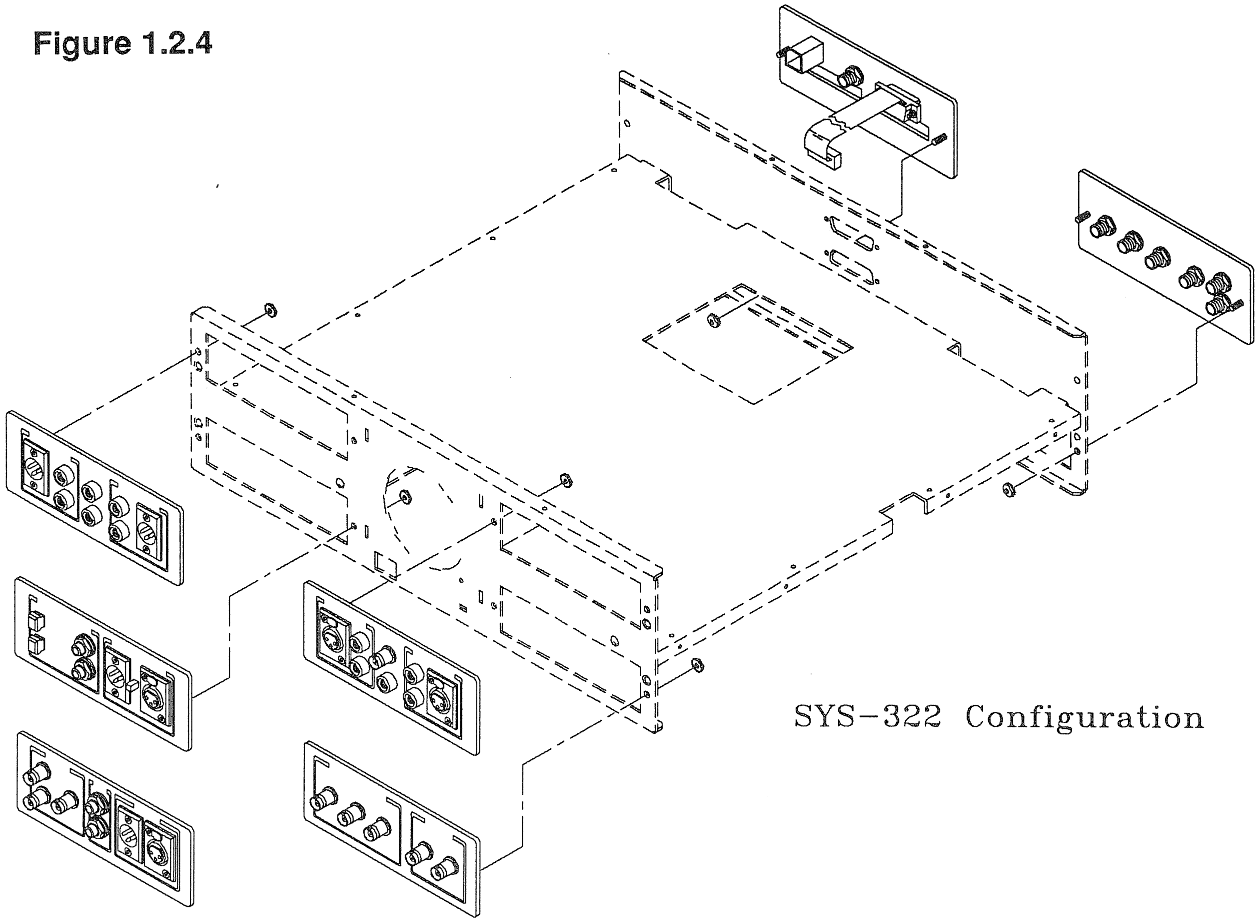


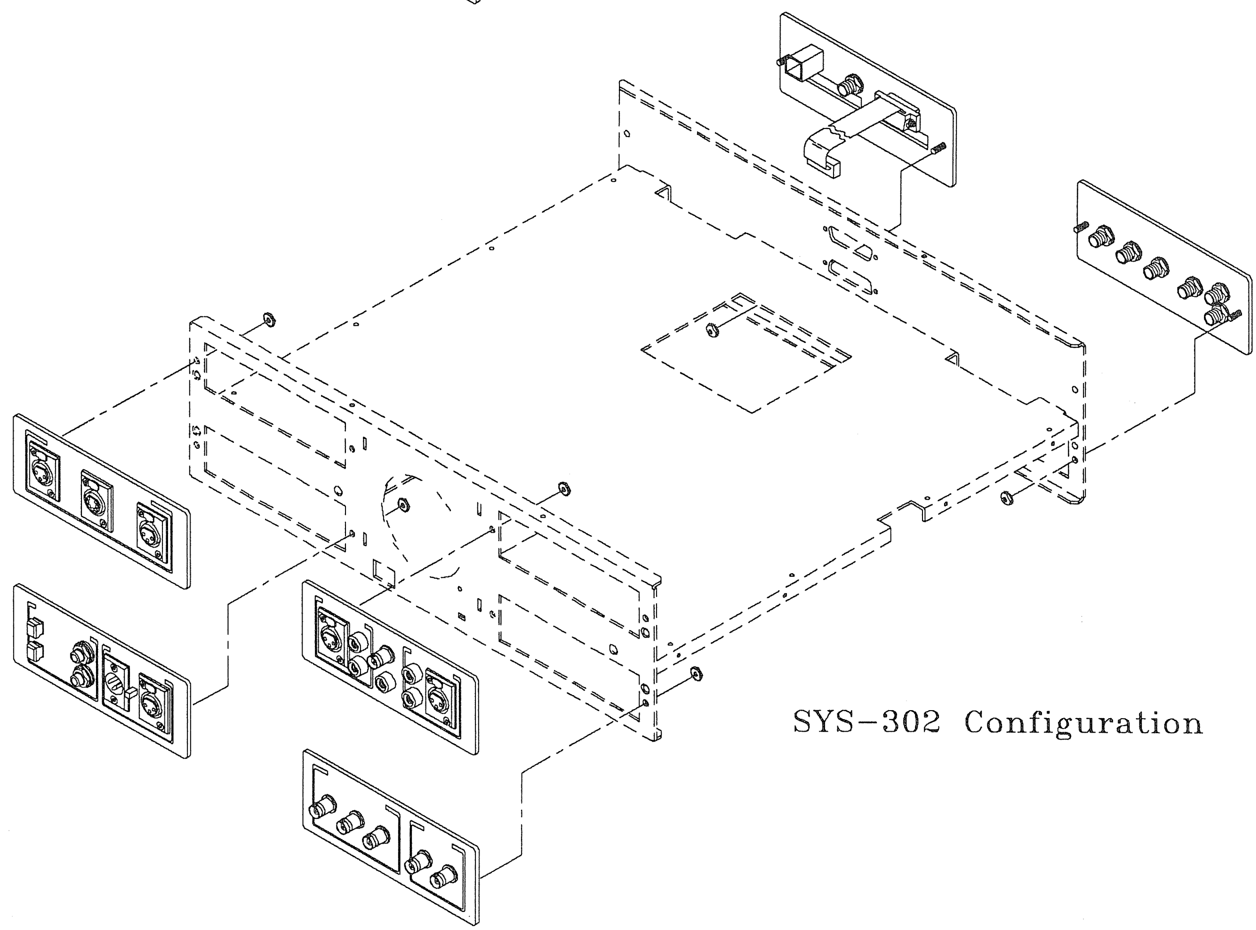
SYS-222 Configuration



SYS-202 Configuration

Figure 1.2.4


SYS-322 Configuration


SYS-302 Configuration

additional capability and connectors for digital signal generation and analysis. The lower left front panel contains a variety of digital audio signal connectors. The lower right back panel contains parallel digital I/O connectors plus bnc connectors for the dsp analog I/O. The lower left back panel contains 3 bnc connectors for the generator auxiliary signals.

SYS-302 Configuration

Similar to the SYS-322 except the analog generator is deleted. The upper left front panel contains a pair of 3-pin female XLR connectors to provide interconnection to a SYS-20 for the generator monitor function plus a 7-pin female XLR for DSP related signals.

1.3 DIGITAL INTERFACE VERSIONS

The System One hardware can not function without host computer control. All systems contain one of three different digital interfaces designated by the letter code "A", "S", or "G" appended to the system configuration nomenclature. Thus, for example, the SYS-322A contains the A-version interface.

> *NOTE: Early production units with serial numbers 10001 to 10299 did not include a letter suffix in their original system nomenclature. These units contain the A-version digital interface.*

The digital interface option can also be determined by observing the connector types and/or the system configuration decal located on the back chassis panel of System One. Systems with the A-version interface will have either one or two 25-pin D-subminiature connectors labeled with the words "Audio Precision Interface (APIB)". Systems with the S-version interface will have a pair of 25-pin D-subminiature connectors (one for APIB and one for RS-232) plus a DIP switch for baud rate selection. Systems with the G-version interface will have a single 25-pin D-subminiature connector for the APIB, IEEE-488 connector, and a DIP switch for setting the instrument address.

A-Version Interface

The A-version interface is an 8-bit parallel bus optimized for Audio Precision instrument control. It is referred to as the "APIB" (Audio Precision Interface Bus) throughout this manual. See section 1.4 for more information about the operation of the APIB. Units with the "A" version interface include a digital interface card that is installed in the host computer, a digital interconnection cable, and an extensive software program (S1.EXE) to operate the hardware, create and run tests and procedures, process data, and display results.

S-Version Interface

The S-version interface provides both APIB and RS-232 control capability (but not simultaneously). Baud rate is selected by rear panel accessible DIP switches. Setting all the baud rate DIP switches to the "up" position activates the APIB. Please note that the APIB must be used when servicing or calibrating a System One.

G-Version Interface

The G-version interface provides both APIB and IEEE-488 control capability (but not simultaneously). Address selection is set by rear panel accessible DIP switches. Setting all the address DIP switches to the "up" position activates the APIB. Please note that the APIB must be used when servicing or calibrating a System One.

1.4 THE APIB DIGITAL INTERFACE

Computer Interface Cards

Because the Audio Precision digital interface is unique, an Audio Precision interface card must be installed in one of the expansion slots of the host computer. There have been three versions of the digital interface card:

PCI-1 For IBM PC-XT-AT or compatible computers. Includes a 9-pin ***female*** D-subminiature connector for the original version Microsoft bus (parallel) mouse. ***This version is no longer in production.***

PCI-2 Current or replacement version for IBM PC-XT-AT or compatible computer. Includes a 9-pin ***male*** D-subminiature connector for general purpose serial port usage.

PCI-3 For the IBM PS/2 family of computers. Not compatible with the PC-XT-AT.

Hardware Interface

The interface between the host computer and the Audio Precision System One is a byte-wide bidirectional link with multiplexed address and data information. This allows interfacing with any computer which has two available I/O ports. It consists of eight data/address lines, four host driven control lines and three open collector lines driven from Audio Precision equipment. All information is sent and received over these lines under the control of the host computer. Direction of information flow and timing is controlled by the host.

The interface allows for "daisy chaining" of several pieces of equipment to the same host without additional interface cards. The drive capability of the lines is up to 24 receivers, depending on the cable lengths involved. The interface allows for up to 256 addresses, normally allocated in groups of 16 per functional device on the bus. This gives a maximum of 16 devices.

TABLE 1.4.1 lists the connector pin assignments. Brief functional descriptions are given below.

E0 - E7 are the bidirectional lines which handle address and data information. They have a controlled rise and fall time to minimize emitted RFI and to eliminate coupling into the control lines.

EA is the address strobe line. The host places the desired address on the bus and, after it is settled, pulses the address strobe line high. The address information is latched in each receiver on the falling edge of the strobe.

EW is the data write strobe line. The host places the desired data on the bus and, after it is settled, pulses this line high. The data is latched on the falling edge of the strobe.

ER is the data read strobe line. The host pulls this line high and the addressed device will place the data to be sent on the bus. The host then inputs the data and pulls the data read strobe low again.

ERST forces a power-on reset. This places all devices on the bus into a known state and places generator outputs and analyzer inputs into safe disconnected states. The normal state of the line is low, a high will force reset. This line has been designed to force a reset if the interface cable is disconnected.

/ATT is an open collector line driven by the receiving devices. If the address currently latched into the receivers is used by any of the devices this line will be pulled low. This serves two purposes. First, the buffer on the System One interface card uses this line to know that it should be active. Secondly, the host computer can tell if a card is present by writing its address and looking for the "/ATT" line to go low.

/EIRQ is an open collector line driven by the receiving devices. If any device wants to signal the host that a task is completed or that attention is requested, this line is pulsed low. The PCI card is designed to latch the low pulse or to be interrupted by the pulse.

PWR indicates the state of all devices on the interface. If any unit loses power, this line will be pulled low.

/AUX is a general purpose line reserved for future use.

TABLE 1.4.1
INTERFACE PIN ASSIGNMENTS

NAME	INTERFACE PIN	DESCRIPTION	POLARITY
GROUND	1	Ground	
E0	2	Data/Address Bit 0	
E1	3	Data/Address Bit 1	
E2	4	Data/Address Bit 2	
E3	5	Data/Address Bit 3	
E4	6	Data/Address Bit 4	
E5	7	Data/Address Bit 5	
E6	8	Data/Address Bit 6	
E7	9	Data/Address Bit 7	
ER	10	Read Strobe	Active high
EW	11	Write Strobe	Active high
EA	12	Address Strobe	Active high
/EIRQ	13	Interrupt Request	Active low
/ATT	14	Valid Address	Active low
/AUX	15	Auxiliary Signal	Active low
ERST	16	Reset Drive	Active high
PWR	17	Power Good	Active high
GROUND	18-25	Ground	

Software Interface

All I/O is performed through four locations in the computer. Data is read and written at the base address plus 3. The System One module port address is written to the base address plus 2. Reads from base address plus 2 access the status lines /AUX, PWR, /ATT, and a latched version of the interrupt line /EIRQ.

For DMA from the System One to the computer the interface will delay data by one byte. This is due to an inconsistency in the IBM PC of the I/O channel not ready protocol. If for example the DMA controller is set to transfer a block of 100 points, the first point will be the last byte read from the System One before the DMA and the 100th byte of DMA data will be lost.

This requires one of two programming approaches for proper DMA action. The first byte of the desired DMA may be read with a normal read sequence. The remaining bytes are then read with a DMA transfer of the full length (100 in the above example). The first DMA point will now be correct since it is a duplicate of the point previously read. The other approach to input DMA is to transfer one more point than is necessary (101 in the above example) and throw the first point away. DMA from the computer to the System One will take place normally with no special attention.

1.5 CIRCUIT BOARD IDENTIFICATION

Nomenclature and Versions

System One circuit board nomenclature consists of a three character sequence followed by a hyphen and a single digit number. The three letters indicate the board type and the number indicates the board version. Typical examples include "GEN-1" and "MFI-5", etc. In cases where there are multiple versions of a given board, it is imperative that the correct version be determined before servicing.

Identification Decals

Every circuit board has an identification decal mounted in a clearly visible location that contains a production code number. This number has the format "ABCx-yyyyy-zz" or "ABCx-yyyyy" where "ABC" is the circuit board type (MFI, W&F, DSP, etc.) and "x" is the version. This identification rule applies to all boards ***except*** the LVF, PHA, and DIS (see next sub-section).

Special Note for LVF, PHA, and DIS Modules

A major modification occurred during the early production history of the LVF, PHA, and DIS modules that added a second independent signal path for simultaneous two channel amplitude measurements. The version number in all three board names was changed to "-2" at this time, however the production code numbers continued using x = 1. For these three modules only, the first digit of the next 5-digit sequence must be examined to determine the version:

For the LVF module only: a first digit of 1 to 5 signifies a "-1" version, while 6 or higher signifies a "-2" version. Thus, for example, "LVF1-2yyyy-zz" identifies a LVF-1. "LVF1-6yyyy-zz" identifies a LVF-2.

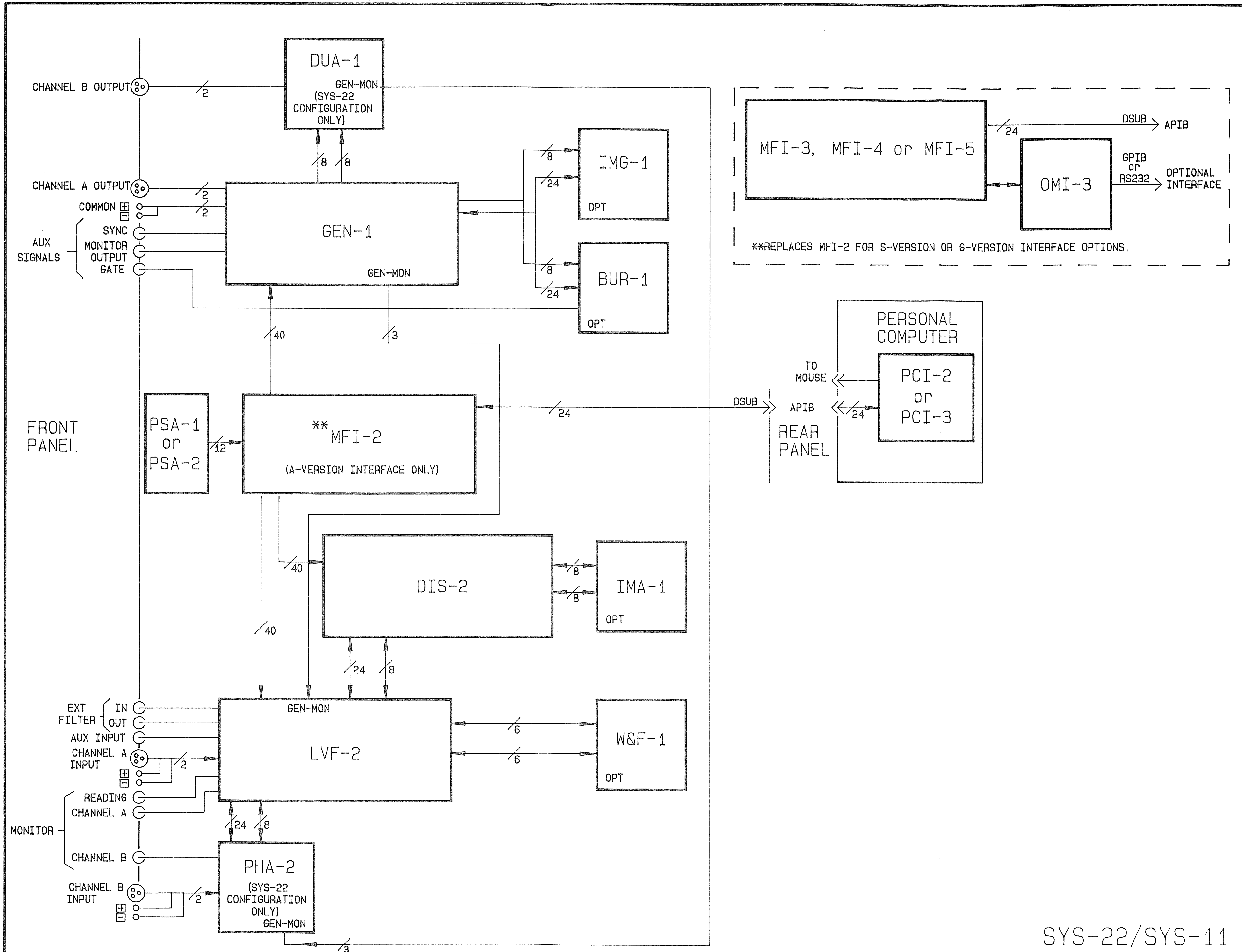
For the PHA and DIS modules: a first digit of 1 to 6 signifies a "-1" version, while 7 or higher signifies a "-2" version. Thus, for example, "DIS1-3yyyy-zz" identifies a DIS-1. "DIS1-7yyyy-zz" identifies a DIS-2.

The mainframe serial number provides the easiest means of version identification. Only very early production units with serial numbers 10001-10299 contain the original "-1" versions of all three modules. All later units (serial number 20300 and higher) contain the "-2" versions. The technical documentation for the LVF-1, PHA-1, and DIS-1 is located in the Section 7 supplement in Volume 2 because only a relatively small number of units contain the "-1" versions.

SECTION 2 - BLOCK DIAGRAMS

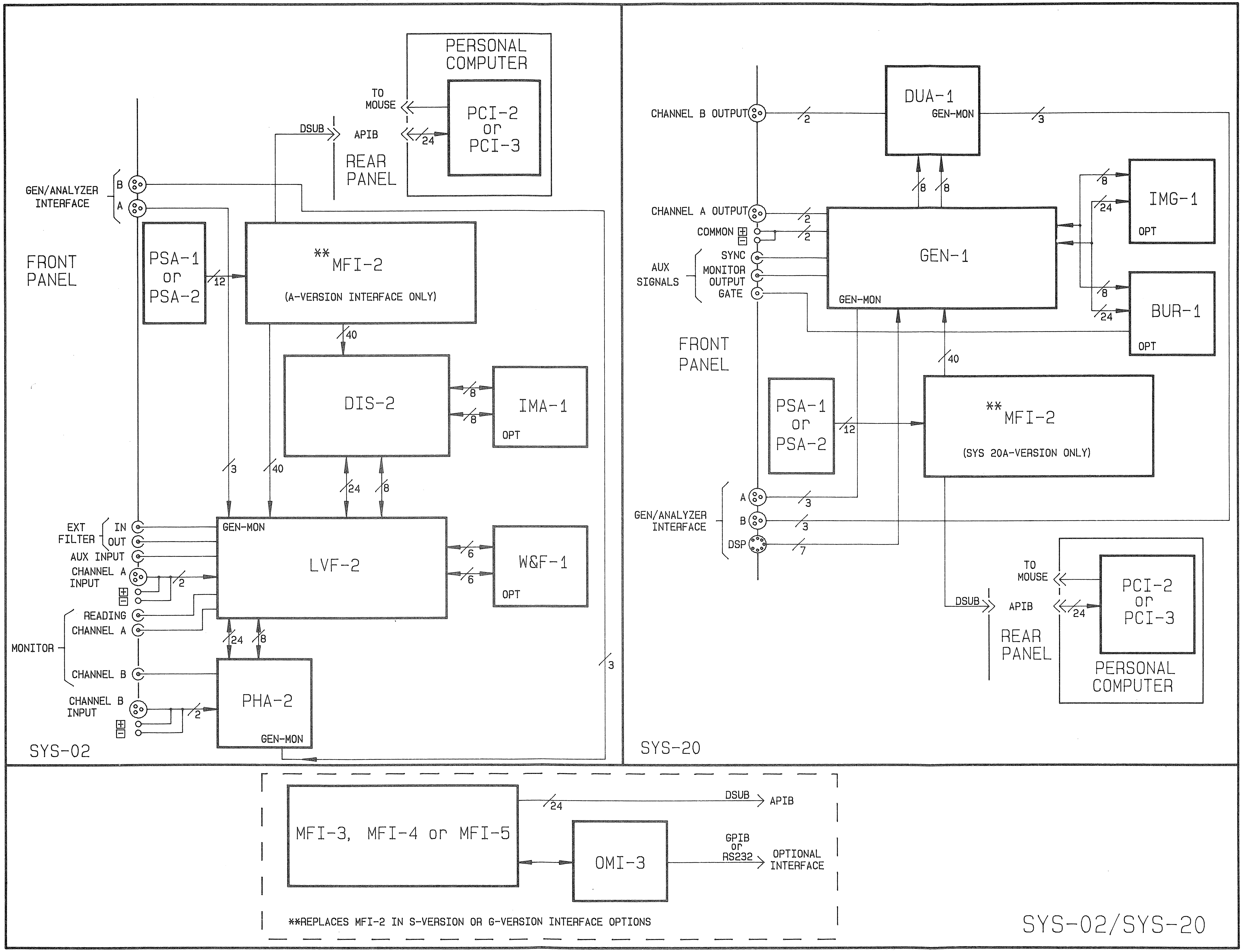
This section contains the block diagrams for the eight standard System One configurations. Every configuration includes a common design chassis, enclosure, power supply, digital interface, and one or more functional modules. All blocks are given a three letter alpha code plus a numerical suffix (for example "GEN-1") that directly corresponds with the circuit description and schematics with the same title.

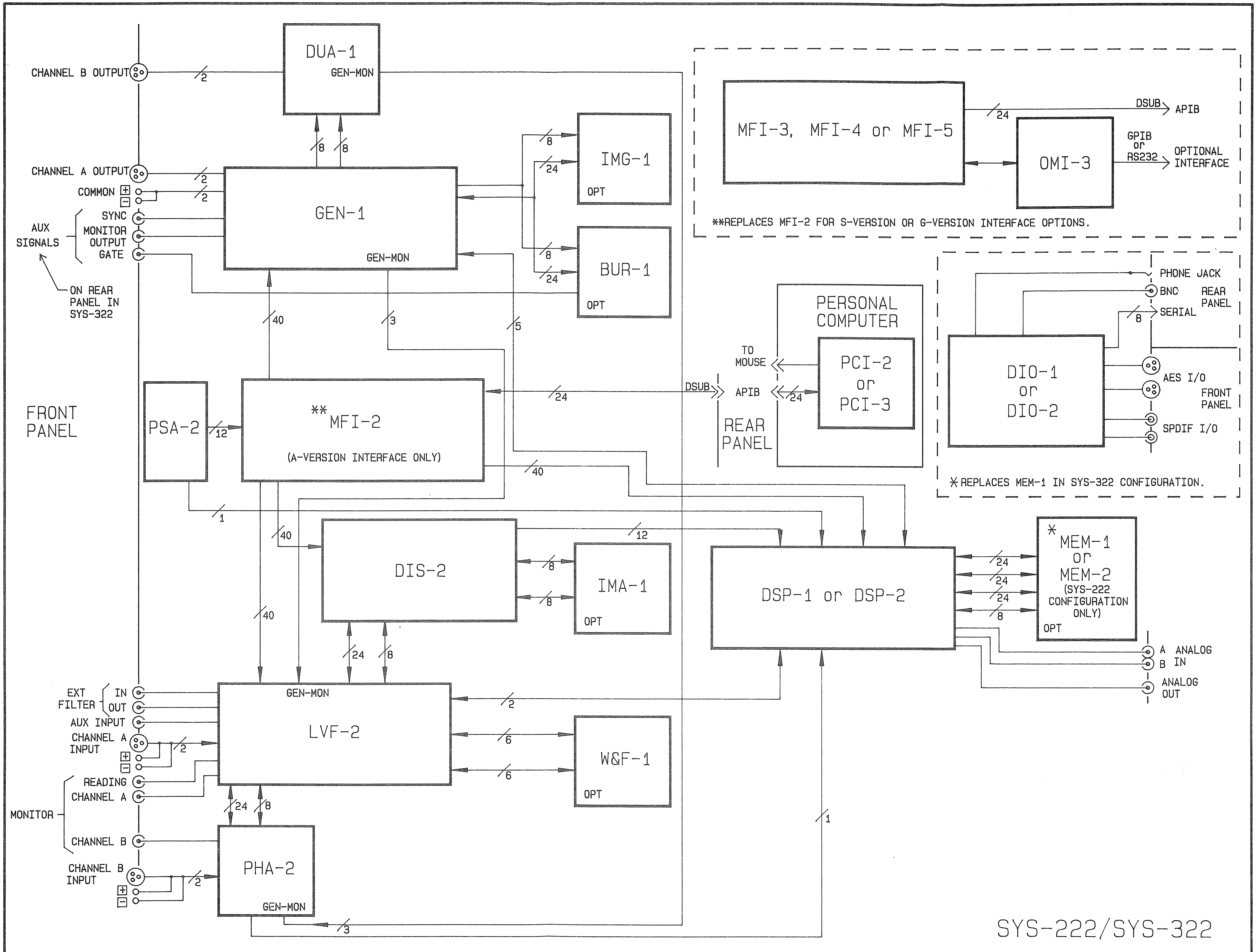
See Section 6 in the second volume of this service manual for diagrams showing the location of the circuit boards.

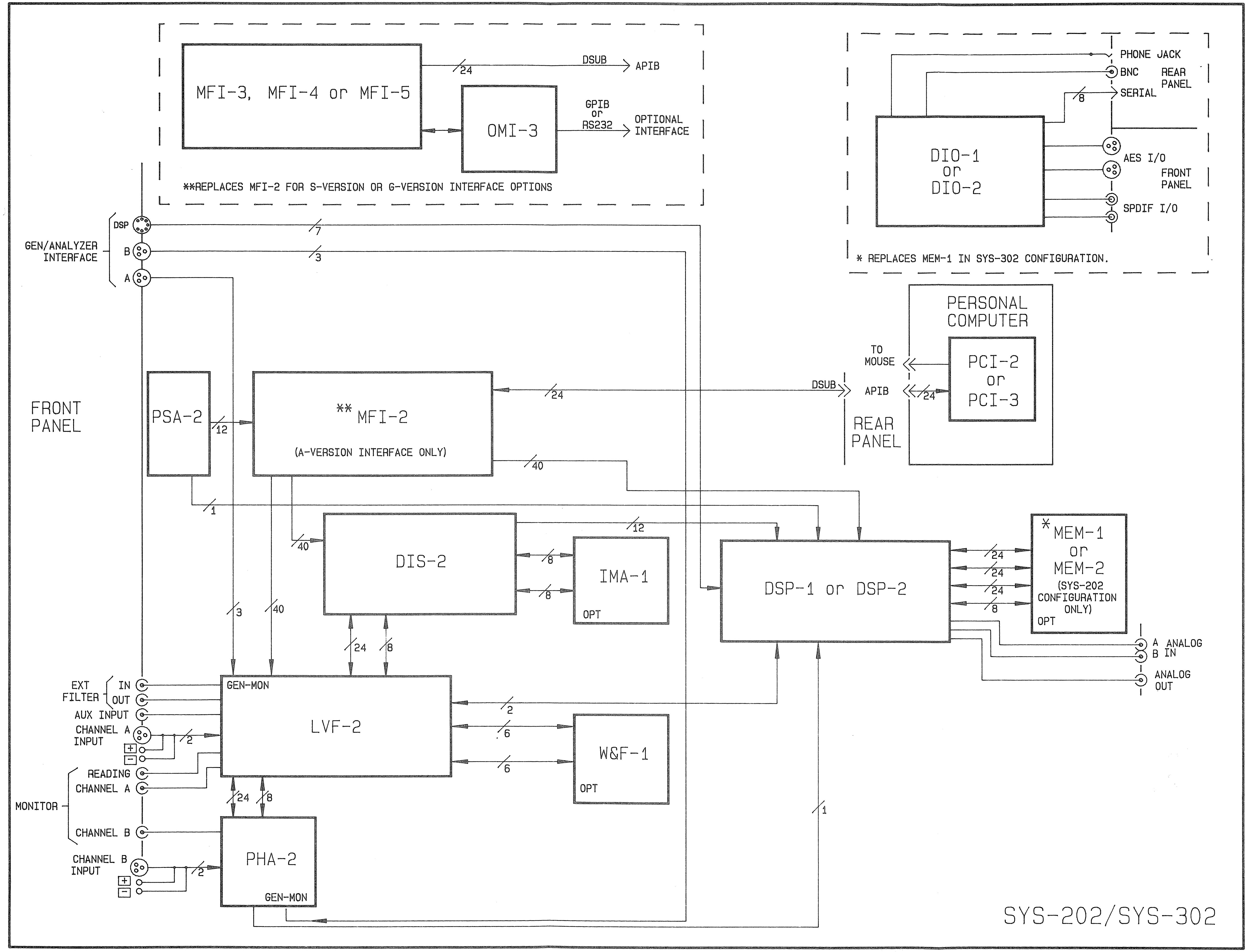


DUA-1
GEN-MON
(SYS-22 CONFIGURATION ONLY)
CHANNEL B OUTPUT
CHANNEL A OUTPUT
COMMON
AUX SIGNALS
SYNC
MONITOR OUTPUT
GATE
GEN-1
GEN-MON
IMG-1
OPT
BUR-1
OPT
MFI-3, MFI-4 or MFI-5
DSUB
APIB
OMI-3
GPIB or RS232
OPTIONAL INTERFACE
**REPLACES MFI-2 FOR S-VERSION OR G-VERSION INTERFACE OPTIONS.
PERSONAL COMPUTER
PCI-2 or PCI-3
TO MOUSE
APIB
DSUB
REAR PANEL
FRONT PANEL
PSA-1 or PSA-2
**MFI-2
(A-VERSION INTERFACE ONLY)
DIS-2
IMA-1
OPT
EXT FILTER
IN
OUT
AUX INPUT
CHANNEL A INPUT
GEN-MON
LVF-2
W&F-1
OPT
MONITOR
READING
CHANNEL A
CHANNEL B
CHANNEL B INPUT
PHA-2
(SYS-22 CONFIGURATION ONLY)
GEN-MON
2
8
24
40
3
12
6

SYS-22/SYS-11


PERSONAL COMPUTER
PCI-2 or PCI-3
TO MOUSE
APIB
DSUB
REAR PANEL
GEN/ANALYZER INTERFACE
B
A
FRONT PANEL
PSA-1 or PSA-2
12
**MFI-2
(A-VERSION INTERFACE ONLY)
40
DIS-2
IMA-1
OPT
8
3
24
EXT FILTER
IN
OUT
AUX INPUT
CHANNEL A INPUT
GEN-MON
LVF-2
W&F-1
6
2
MONITOR
READING
CHANNEL A
CHANNEL B
CHANNEL B INPUT
PHA-2
SYS-02
CHANNEL B OUTPUT
DUA-1
CHANNEL A OUTPUT
COMMON
AUX SIGNALS
SYNC
MONITOR
OUTPUT
GATE
GEN-1
IMG-1
BUR-1
(SYS 20A-VERSION ONLY)
DSP
7
SYS-20
MFI-3, MFI-4 or MFI-5
OMI-3
GPIB or RS232
OPTIONAL INTERFACE
**REPLACES MFI-2 IN S-VERSION OR G-VERSION INTERFACE OPTIONS
SYS-02/SYS-20


DUA-1
GEN-MON
CHANNEL B OUTPUT
CHANNEL A OUTPUT
COMMON
AUX SIGNALS
SYNC
MONITOR OUTPUT
GATE
ON REAR PANEL IN SYS-322
GEN-1
GEN-MON
IMG-1
OPT
BUR-1
OPT
MFI-3, MFI-4 or MFI-5
OMI-3
DSUB
APIB
GPIB or RS232
OPTIONAL INTERFACE
**REPLACES MFI-2 FOR S-VERSION OR G-VERSION INTERFACE OPTIONS.
PERSONAL COMPUTER
PCI-2 or PCI-3
TO MOUSE
APIB
REAR PANEL
PHONE JACK
BNC
REAR PANEL
SERIAL
DIO-1 or DIO-2
AES I/O
FRONT PANEL
SPDIF I/O
⁎REPLACES MEM-1 IN SYS-322 CONFIGURATION.
FRONT PANEL
PSA-2
**MFI-2
(A-VERSION INTERFACE ONLY)
DIS-2
IMA-1
OPT
DSP-1 or DSP-2
⁎MEM-1 or MEM-2
(SYS-222 CONFIGURATION ONLY)
OPT
A ANALOG IN
B
ANALOG OUT
EXT FILTER
IN
OUT
AUX INPUT
CHANNEL A INPUT
LVF-2
GEN-MON
W&F-1
OPT
MONITOR
READING
CHANNEL A
CHANNEL B
CHANNEL B INPUT
PHA-2
GEN-MON
SYS-222/SYS-322


MFI-3, MFI-4 or MFI-5
DSUB
24
APIB
OMI-3
GPIB
or
RS232
OPTIONAL
INTERFACE
**REPLACES MFI-2 FOR S-VERSION OR G-VERSION INTERFACE OPTIONS
PHONE JACK
BNC
SERIAL
REAR
PANEL
8
DIO-1
or
DIO-2
AES I/O
FRONT
PANEL
SPDIF I/O
* REPLACES MEM-1 IN SYS-302 CONFIGURATION.
GEN/ANALYZER
INTERFACE
DSP
B
A
7
3
PERSONAL
COMPUTER
TO
MOUSE
APIB
PCI-2
or
PCI-3
REAR
PANEL
FRONT
PANEL
PSA-2
12
** MFI-2
(A-VERSION INTERFACE ONLY)
40
1
DIS-2
IMA-1
OPT
DSP-1 or DSP-2
*MEM-1
or
MEM-2
(SYS-202
CONFIGURATION
ONLY)
OPT
A ANALOG
B IN
ANALOG
OUT
EXT
FILTER
IN
OUT
AUX INPUT
CHANNEL A
INPUT
GEN-MON
LVF-2
W&F-1
6
2
MONITOR
READING
CHANNEL A
CHANNEL B
CHANNEL B
INPUT
PHA-2
GEN-MON
SYS-202/SYS-302

SECTION 3
CALIBRATION & MAINTENANCE

This section contains information on calibration, checking performance, cleaning, troubleshooting tips, and repair.

DO NOT attempt to repair or service System One, or any of its accessories, unless properly qualified.

SECTION 3
CALIBRATION & MAINTENANCE

3.1 GENERAL INFORMATION

Software Diskettes

All of the calibration and performance check procedures are contained in the four software diskettes included with this manual. The current version is 2.10A with a revision date of December 1992 or later. ***DO NOT use or mix files with earlier 2.10A revisions.***

Software based procedures are provided instead of written procedures because of the inherent complexity of System One. They enable the automatic control of hardware settings, ranges and signal conditions, and include all necessary instructions and operator prompts.

Host Computer Requirements

A DOS-based host computer containing at least 400K of free memory and the Audio Precision hardware interface card is required to operate the System One or DCX-127. Units with the "G" or "S" version digital interface must use the APIB port (see Section 1.3).

Running a Procedure

The calibration and performance check procedures run under the Audio Precision System One control program called S1.EXE, and a basic familiarity with its operation is assumed. Refer to the System One Operator's Manual for more information.

To perform a calibration or performance check procedure, insert the "S1.EXE" diskette into the A (or B) drive of the host computer and change the DOS default disk drive specification if necessary. Type "**S1CAL**" and press <Enter> to automatically load the System One control program S1.EXE with optimum buffer size allocations. This process may take up to 60 seconds depending upon computer and disk drive speed.

When the System One logo appears, remove the "S1.EXE" diskette and replace with the desired calibration or performance check diskette. Type "L" then "P" (Load Procedure) to view the various procedure choices. The procedure names are closely related to the module/option nomenclature. Select the desired procedure using the arrow keys and press <Enter>. Type "R" then "P" (Run Procedure), or press <Enter> twice, to begin. A procedure may be aborted at any time by pressing the <F1> function key.

Special Note for SYS-20, SYS-02, SYS-202, and SYS-302 System One Configurations

The System One calibration and performance check software requires the presence of both generator and analyzer functions. A generator-only or analyzer-only configuration must be paired with a second System One of complementary configuration for proper operation. If this is not possible, please contact Audio Precision for more information.

Recommended Calibration Interval

Audio Precision recommends a 12 month calibration interval for the System One and DCX-127. More frequent calibration may be indicated depending upon exposure to environmental extremes or physical abuse. A complete re-calibration is also recommended following major repair, modification, or option installation.

The SWR-122 family of switchers and the SIA-322 serial interface adapter do not require calibration.

Test Points

Certain test points are composed of 200 Ohm resistors mounted on end. These points have been provided to avoid potential capacitive loading effects or interference problems from external test equipment. Unless otherwise noted, any convenient chassis point may be used as the ground reference for voltage and signal measurements.

3.2 SYSTEM ONE CALIBRATION

Test Equipment Requirements

The following test equipment is required to calibrate the System One. Minimum performance characteristics and examples of recommended models are listed.

1) DC Voltmeter: ±0.1% to 25 Volts (Fluke 8842A)

2) AC Voltmeter: ±0.1% at 1 kHz, ±0.5% at 100 kHz (Fluke 8842A)

3) Counter: ±10 PPM to 25 MHz, ≥6 digits resolution (Phillips PM6666)

4) General purpose dual channel 100 MHz oscilloscope (Any suitable Tektronix or HP model)

Preparation for Calibration

Unplug the ac power cord and remove both the top and bottom instrument covers. Also remove the internal U-shaped shields enclosing the power supply and mainframe interface assemblies (see Figure 6.1 in Section 6).

Position the unit upside down to gain access to the power supply module. ***DO NOT stand the unit on its side!*** Reconnect the ac power mains cord and turn the power switch on. Be sure the ac power line is within nominal limits. Allow at least 30 minutes for circuit stabilization before proceeding with adjustments.

> WARNING!
> *Hazardous voltages exist inside System One whenever it is plugged into an ac power source. DO NOT touch or probe any component associated with the power transformer primary circuit, unless the power cord has been unplugged.*

If calibration is taking place following repair or circuit board removal, be sure to replace all mounting hardware before making adjustments. Many of the circuit boards depend upon grounding paths through the mounting hardware for proper operation.

Calibration Outline

The following System One calibration procedures are contained on the "Calibration Procedures" diskette. They must be performed in the order listed to avoid incorrect results. Please note that many procedures are valid only with certain configurations or options. Calibration must be performed between +20°C and +25°C only.

1 - **CAL-SYS.PRO** (All units)

Adjusts the ±15 V regulated power supplies and the 20 MHz master clock. (Note: This procedure replaces CAL-PS.PRO and CAL-20M.PRO in previous versions of the calibration software.)

2 - **CAL-GEN.PRO** (All units except SYS-02, SYS-202, and SYS-302)

Adjusts the GEN module (main analog generator) frequency accuracy, amplitude accuracy, flatness, and low frequency distortion.

3 - **CAL-LVF.PRO** (All units except SYS-20)

Adjusts the LVF module (main analyzer) detectors, low frequency filter response, and high frequency flatness. Also adjusts the channel-A attenuator compensation and CMRR.

4 - **CAL-PHA.PRO** (All units except SYS-11 and SYS-20)

Adjusts the PHA module channel-B attenuator compensation, CMRR, and phasemeter.

5 - **CAL-DIS.PRO** (All units except SYS-20)

Adjusts the DIS module notch filter control loops and "LEVEL" meter calibration.

6 - **CAL-DSP.PRO** (SYS-202, SYS-222, SYS-302, and SYS-322 only)

Adjusts the DSP module anti-alias filter phase matching, A/D converter, D/A converter, master clock duty cycle, and EEROM calibration constants.

7 - **CAL-BUR.PRO** (Units with option "BUR" only)

Adjusts amplitude calibration of the optional burst, noise, and squarewave generators located on the BUR option board.

8 - **CAL-IMD.PRO** (Units with option "IMD" only)

The IMD option normally consists of two circuit boards. Part 1 checks the response and gain accuracy of the IMD analyzer filter located on the IMA board. Part 2 adjusts the frequency and amplitude accuracy of the IMD test signal generators located on the IMG board.

9 - **CAL-W&F.PRO** (Units with option "W&F" only)

Adjusts the detectors and calibration accuracy of the wow and flutter analyzer located on the W&F option board. This procedure executes a special compiled program that synthesizes a calibrated FM source by rapidly toggling the normal generator output between two measured frequencies.

10 - **CAL-FBP.PRO** (Units with "FBP-xxxx" option filters)

Adjusts the gain accuracy of option bandpass filters installed on the LVF module.

Adjustment Location Drawings

The individual calibration procedures display simplified figures showing the approximate location of adjustments and test points. More detailed drawings can be found in Section 3.8. Access holes are provided in those satellite or option boards that mount above adjustments located on the larger module circuit boards.

3.3 DCX-127 CALIBRATION

Test Equipment Requirements

The following test equipment are required to calibrate the DCX-127. Minimum performance characteristics and examples of recommended models are given.

1) DC Calibrator: ±0.01% to 500 Volts
   (Fluke 5100B)

2) DC Voltmeter: ±0.01% to 25 Volts
   (Fluke 8842A)

3) 1.50-1.90 kOhm resistor, value known to ±0.01%

4) 15.0-19.0 kOhm resistor, value known to ±0.01%

5) 150-190 kOhm resistor, value known to ±0.01%

6) 1.50-2.00 MOhm resistor, value known to ±0.03%

Preparation for Calibration

Unplug the ac power cord and remove the top cover only. Do not remove the bottom cover. See Figure 6.6 in Section 6 for more detail regarding screw locations.

Reconnect the ac power source, and turn the power switch on. Be sure the ac power line voltage is within nominal limits. Allow at least 30 minutes for circuit stabilization before proceeding with adjustments.

> **WARNING!**
> *Hazardous voltages exist inside the DCX-127 whenever it is plugged into an ac power source. DO NOT touch or probe any component associated with the power transformer primary circuit, unless the power cord has been unplugged.*

The DMM board guard shield must be installed for proper calibration. All of the DMM adjustments are accessible through holes in the shield.

Calibration Outline

The following DCX-127 calibration procedures are provided on the "Calibration Procedures" software diskette. These procedures contain all necessary instructions, adjustment location figures, and operator prompts. They will automatically set the hardware to the proper modes and ranges. DCX-127 calibration must be performed between +20°C and +25°C only.

1 - **CAL-DCM.PRO**

Adjusts the accuracy of the 4-1/2 digit dc voltmeter and ohmmeter.

2 - **CAL-DCV.PRO**

Adjusts the offset, accuracy, and common-mode rejection of the programmable dc sources.

Adjustment Location Drawings

The individual calibration procedures display simplified figures showing the approximate location of adjustments and test points. More detailed drawings can be found in Section 3.8.

3.4 PERFORMANCE CHECKS

A variety of performance check procedures are provided on the software diskettes labeled "Performance Checks" and "DSP Performance Checks". These procedures are fully automated and require no special equipment other than commonly available cables. Test data is compared to published specifications or other derivable limits. Pass-fail results are automatically displayed at the end of each procedure.

NOTE: Audio Precision reserves the right to change specifications without prior notice.

Performance check procedures are useful for quickly checking the operation of System One or any of its major options. They are also useful for testing upgrades, isolating a problem during trouble-shooting, or verifying the effectiveness of a repair. If a test failure should occur then adjustment or troubleshooting may be indicated. Under no circumstances should a performance check procedure be used for determining absolute calibration.

Performance Check Procedures

The following procedures are included on the "Performance Checks" diskette. It is recommended that "SYSCHEK.PRO" be run before any other procedure to assert the basic functionality of the system. A failure during this procedure may invalidate many subsequent checks. Allow at least 10 minutes for circuit stabilization before conducting a performance check.

SYSCHEK.PRO (All System One units) Checks basic system operation by testing overall accuracy, ranging, flatness, residual distortion, noise, and phase difference. (Ignore the results of the phasemeter test when checking the single channel SYS-11 configuration.)

CHEK-IMD.PRO Checks the operation of the IMD option (IMG board in the generator section, IMA board in the analyzer section) by testing the relative calibration of three different IMD test signals and overall system residual IMD performance.

CHEK-BUR.PRO Checks the operation of the BUR option by testing the relative calibration of the toneburst, squarewave, and noise signals.

CHEK-W&F.PRO Checks the operation of the Wow & Flutter analyzer option. Calibration is checked using a compiled utility program that toggles the generator output between two frequencies to obtain a calibrated FM source with squarewave modulation. This program automatically corrects for the mathematically predictable error using squarewave modulation and displays the equivalent sinewave modulation results.

CHEK-DCX.PRO - Checks DCX-127 operation by testing DMM dc measurement accuracy, the programmable dc output accuracy, and the digital I/O function.

CHEK-PCI.PRO - Checks operation of the PCI card installed in the host computer by testing the short interval timer circuit. This program compares readings obtained from the timer to the computer's real time clock.

Option Filters

The following procedures are also included on the "Performance Checks" diskette for checking the most popular System One option filters. The procedure names are closely related to the filter nomenclature for ease in selection. Many filters have similar names, so be sure the correct procedure is chosen!

FIL-AWT.PRO - Checks the response of the A-weighting filter.

FIL-CCR.PRO - Checks the response of the CCIR Rec 468 weighting filter.

FIL-CIT.PRO - Checks the response of the CCITT weighting filter.

FIL-CMS.PRO - Checks the response of the C-message weighting filter.

FIL-CWT.PRO - Checks the response of the C-weighting filter.

FIL-RCR.PRO - Checks the response of the FM receiver testing audio bandpass filter.

FIL-D50F.PRO - Checks the response of the 50-usec deemphasis filter.

FIL-D75.PRO - Checks the response of the 75-usec deemphasis filter.

FIL-D75B.PRO - Checks the response of the 75-usec deemphasis plus 15.734 kHz pilot suppression filter.

FIL-D75F.PRO - Checks the response of the 75-usec deemphasis plus 19.00 kHz pilot suppression filter.

FBP-XXX.PRO - Checks the response of the FBP-xxxx family of 1/3-octave bandpass filters. The procedure automatically prompts the operator to enter the bandpass center frequency in Hz.

FLP-XXX.PRO - Checks the response of the FLP-10K, FLP-15K, FLP-19K, FLP-20K, and FLP-22K precision bandwidth limiting filters. The procedure automatically prompts the operator to enter the filter cutoff frequency in Hz.

NOTE: This procedure may give invalid results with other FLP-xxx filters not specifically listed above.

DSP Performance Check Procedures

The following procedures are included on the "DSP Performance Checks" diskette.

CHEK-DSP.PRO Checks the operation of the DSP module in SYS-202, SYS-222, SYS-302, and SYS-322 configurations by testing the dual channel A/D and single channel D/A converter signal paths.

CHEK-DIO.PRO - Checks the operation of the DIO module in SYS-302 and SYS-322 configurations by testing the AES-EBU serial digital audio I/O path.

3.5 CLEANING

Enclosure, Covers, and Shields

Remove accumulated dust on the instrument chassis and other mechanical parts with a soft cloth or small brush. A mild detergent may be used to remove remaining dirt or stains. Do not use strong or abrasive cleaners. Wipe all surfaces clean with a damp cloth.

Fan Filter

The System One fan filter should be cleaned whenever there is a visible buildup of dust. Disconnect the instrument from the ac power source and carefully unsnap the protective grill using a flat blade screwdriver. Remove accumulated dust by blowing compressed air through the filter in the reverse direction, or using a low power vacuum cleaner. Wash the filter in hot water and dry thoroughly before replacing. Replace the filter if there is any sign of decomposition.

Connectors and Connector Panels

Clean with a cotton swab or soft cloth dampened in isopropyl alcohol (IPA) or water. Digital signal connectors should be inspected periodically for bent or damaged pins.

CAUTION
To avoid damage to the paint and lettering, do not use cleaning agents that contain petroleum based solvents or abrasive compounds. Use only isopropyl alcohol or water.

Internal Components and Circuit Boards

Remove dust with clean, dry, low pressure air. A soft, dry brush may be required to loosen particles that resist removal. Always use good static control procedures when handling or cleaning circuit assemblies to avoid component damage.

3.6 REPAIR INFORMATION

Static Sensitive Components

Many electrical components are susceptible to static electricity damage, and can be altered or destroyed by a relatively small discharge. Static discharges can significantly degrade the low noise performance of some op-amps and cause precision metal film resistors to shift out of tolerance. MOS devices are particularly susceptible and require special attention.

Please observe the following precautions to reduce the possibility of accidental static damage:

1. Minimize the handling of components or assemblies. Store in static-free containers until needed.
2. Avoid handling components by their leads.
3. Wear a wrist strap.
4. Use a grounded soldering iron and antistatic suction type or wick type desoldering tools.
5. Maintain a static-free work station and environment. Do not allow any object capable of generating or holding a static charge on the work station surface.

Obtaining Replacement Parts

All electrical and mechanical parts can be obtained directly from Audio Precision or through an authorized Audio Precision distributor. When ordering a part please include the following information:

1. Audio Precision part number

2. Schematic and component number (if electrical)

3. Component description

Standard electronic components and hardware can often be obtained from a local commercial source. Please check the Electrical Parts List (located at the end of each schematic section) for the correct value, rating, tolerance, and other information before ordering a part from a source other than Audio Precision. When selecting a replacement part, remember that its physical size and shape may also affect performance.

If there is a discrepancy between the documentation and the actual unit, replace a component only with the same value as originally installed, or contact Audio Precision. Certain components may be factory selected to optimize specific performance characteristics.

Soldering

A good soldering technique is essential to insure high reliability and performance.

A 15-25 watt, pencil type soldering iron is strongly recommended for most repairs. A 40-60 watt soldering iron may be required to remove certain larger components such as the signal transformer on the GEN-1 module, or the filter capacitors on the power supply board. Using too high of wattage iron can cause the etched circuit paths to separate from the board base material, or melt wiring insulation. Multi-layer circuit boards require extreme care to prevent breaking inner layer connections.

CAUTION

Save the circuit board, not a suspected bad component! Clip out ICs or components to the extent possible before un-soldering. The remaining lead stubs will be much easier to remove with less chance of board damage.

Always keep the soldering iron tip properly tinned to insure good hear transfer. Protect heat sensitive components by holding the component lead with a pair of long-nose plier between the component body and the solder joint. Apply only enough heat to remove the component or to make a good solder joint. Solder should flow smoothly into the joint. Avoid using too much solder. Excess solder should be removed from connections to minimize stray capacitance effects.

Use only an electronics grade 60/40 rosin-core solder. Audio Precision strongly discourages the use of solders containing water soluble flux for repair work. Water soluble flux residues can be very conductive, even when diluted. They are extremely difficult to remove without thoroughly washing the entire circuit board.

Excessive flux residues should be removed by generously flushing the repair area with a suitable solvent such as isopropyl alcohol (IPA), followed by clean water. Be sure that the spaces under sockets, ICs, and large components are thoroughly clean.

3.7 TROUBLESHOOTING TIPS

If intermittent or no readings exist...

Be sure that ac power has been applied to System One and the front panel switch is on! The control software can function in the absence of hardware giving the appearance of partial functionality.

Check the installation of the Audio Precision interface board (PCI) in the host computer. Be sure that all expansion cards are fully seated in their respective sockets. In portable computers vibration can cause an expansion card to work loose.

Check the condition of the digital interface cable and connectors. Particularly inspect the male 25-pin connectors for bent or missing pins.

Check Power Supplies

As a general guideline, the +5V and +15V/-15V supplies should measure within 2% of their nominal values, and the +22V/-22V supplies within 5%. Low frequency ripple should be almost undetectable if a regulated supply is functioning properly, however some high frequency noise is quite normal.

Do not adjust the supplies unless absolutely necessary. Having exact nominal supply voltages is not critical, and will not improve instrument performance. If a supply is repaired or adjusted, the entire instrument must be completely re-calibrated.

Use Performance Check Procedures

The performance check procedures included on the software diskettes provide good starting points in diagnosing a problem. Run SYSCHEK.PRO first to determine if the basic system elements are functioning properly. The other performance check procedures provide more specific testing of the various options or modules.

Beware that some symptoms can result from a problem in many possible locations. For example, an amplitude reading error could be caused by a generator leveler, output amplifier, or attenuator problem; or by a malfunction in the analyzer input, ranging amplifier, filter, or detector stages. Careful analysis of any performance check failures, combined with a good understanding of the instrument architecture will usually narrow the search to several specific circuits. Additional tests can be devised to investigate specific performance characteristics using the standard System One software.

Residual Distortion Problems

Problems with high residual distortion readings are among the most difficult to troubleshoot. The first priority is to determine whether the generator or analyzer is at fault. The use of an independent analyzer is essential to avoid an incorrect diagnosis. Examining distortion behavior versus amplitude or frequency will also provide strong clues to the problem source.

High residual THD+N or IMD readings can also be caused by excessive noise. Observe the Reading Monitor output signal with an oscilloscope to determine whether the problem is related to distortion or noise. Certain op-amps (especially the LF353) can occasionally develop a significant increase in their input noise characteristic.

3.8 ADJUSTMENT LOCATION FIGURES

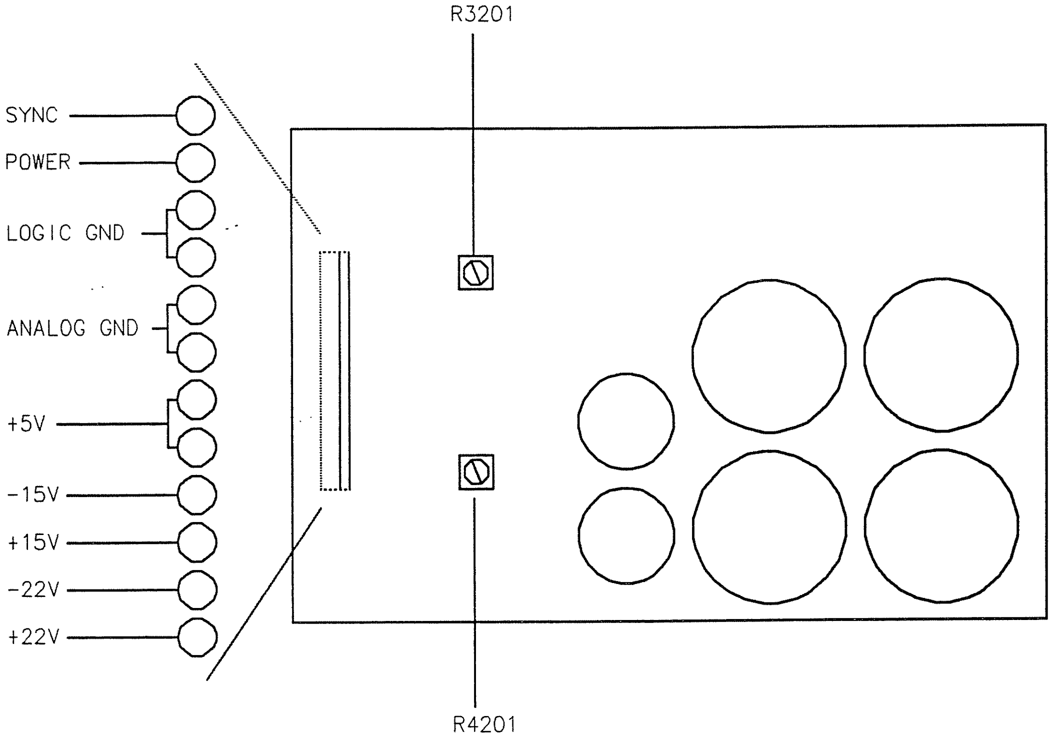


Figure 3.8.1 PSA-1 TEST AND ADJUSTMENT POINTS

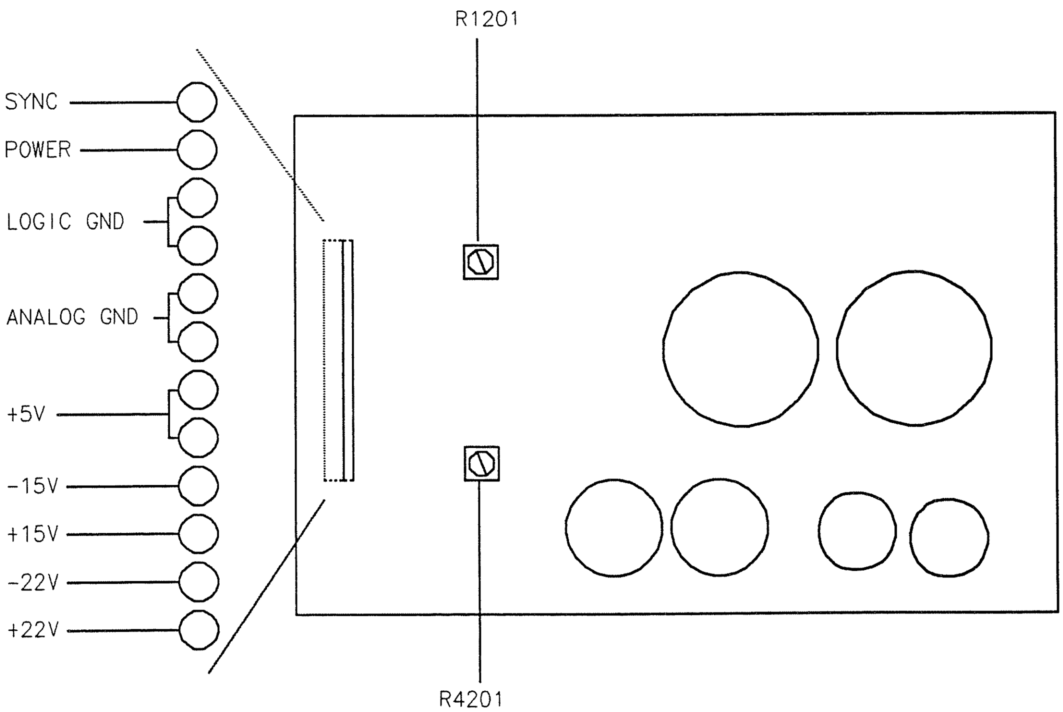


Figure 3.8.2 PSA-2 TEST AND ADJUSTMENT POINTS

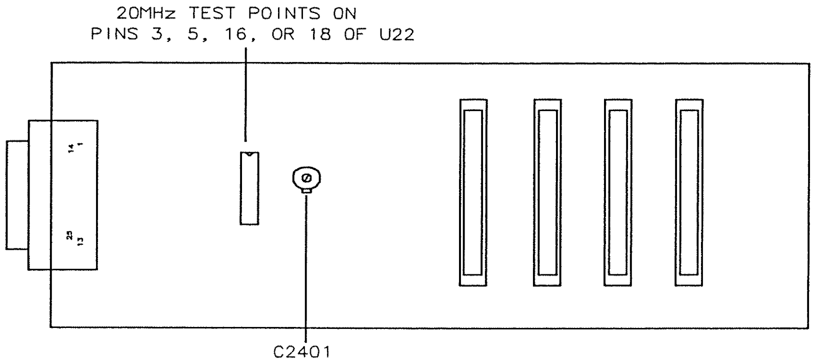


Figure 3.8.3 MFI-1 TEST AND ADJUSTMENT POINTS

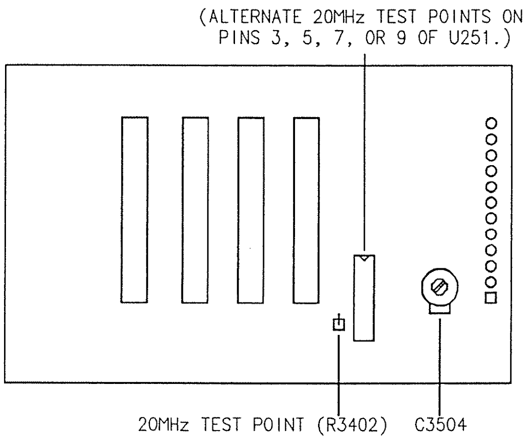


Figure 3.8.4 MFI-2 TEST AND ADJUSTMENT POINTS

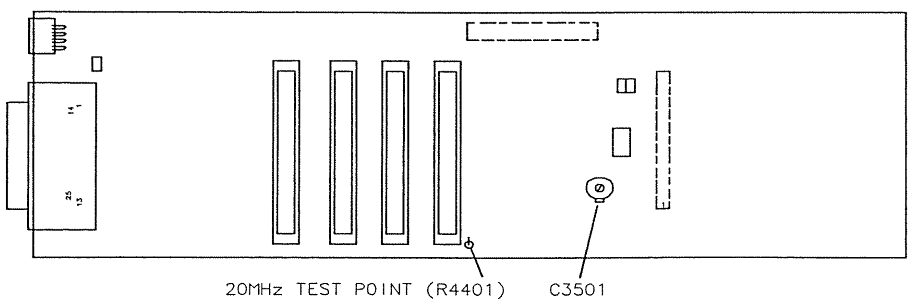


Figure 3.8.5 MFI-3/MFI-4 TEST AND ADJUSTMENT POINTS

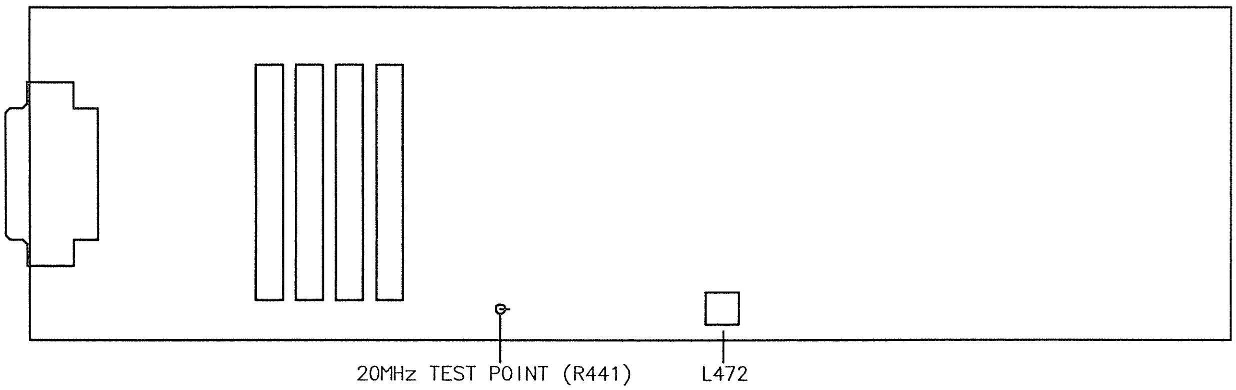


Figure 3.8.6 MFI-5 TEST AND ADJUSTMENT POINTS

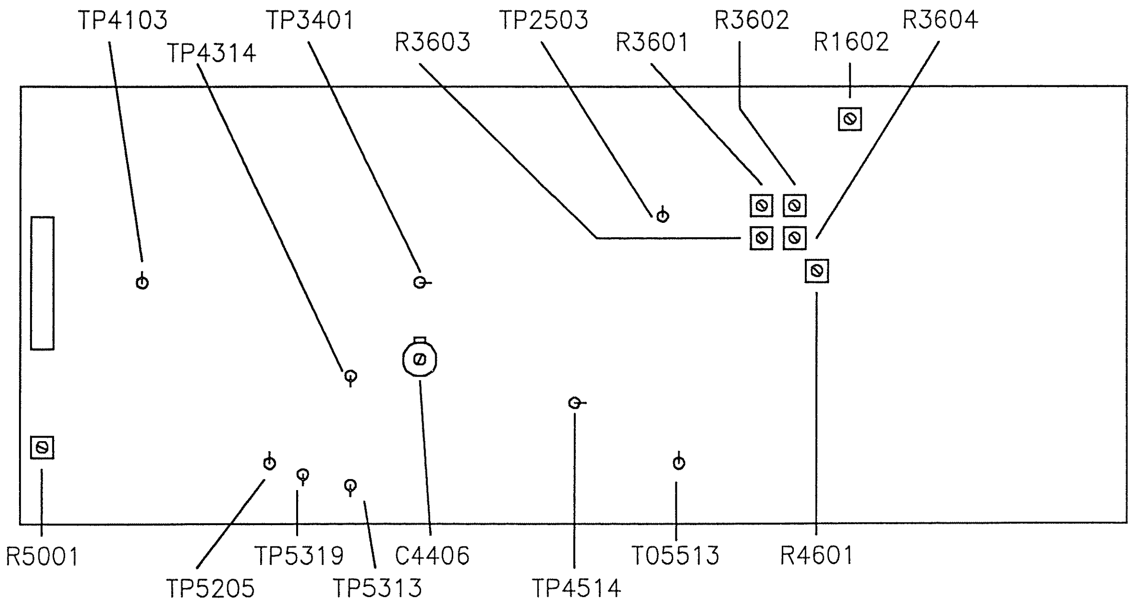


Figure 3.8.7 GEN-1 TEST AND ADJUSTMENT POINTS

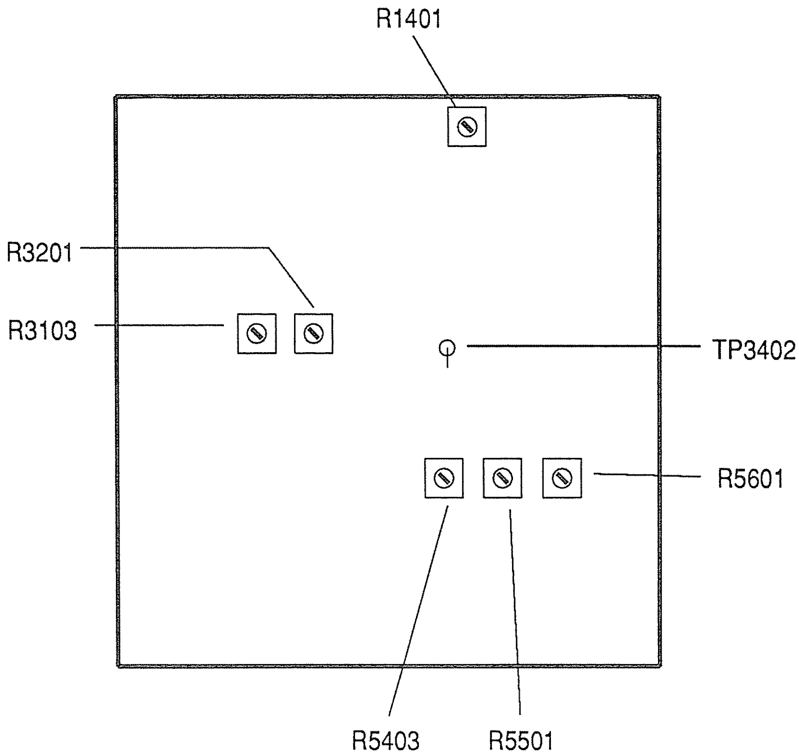


Figure 3.8.8 IMG-1 TEST AND ADJUSTMENT POINTS

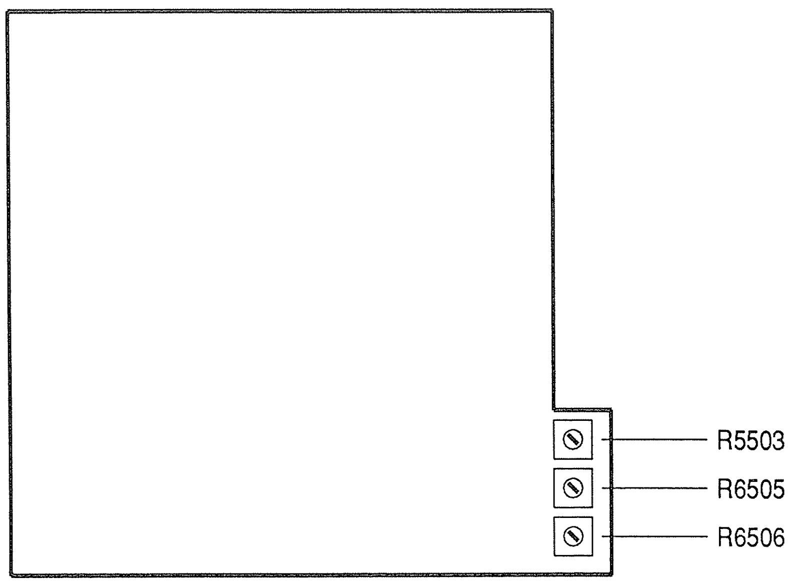


Figure 3.8.9 BUR-1 TEST AND ADJUSTMENT POINTS

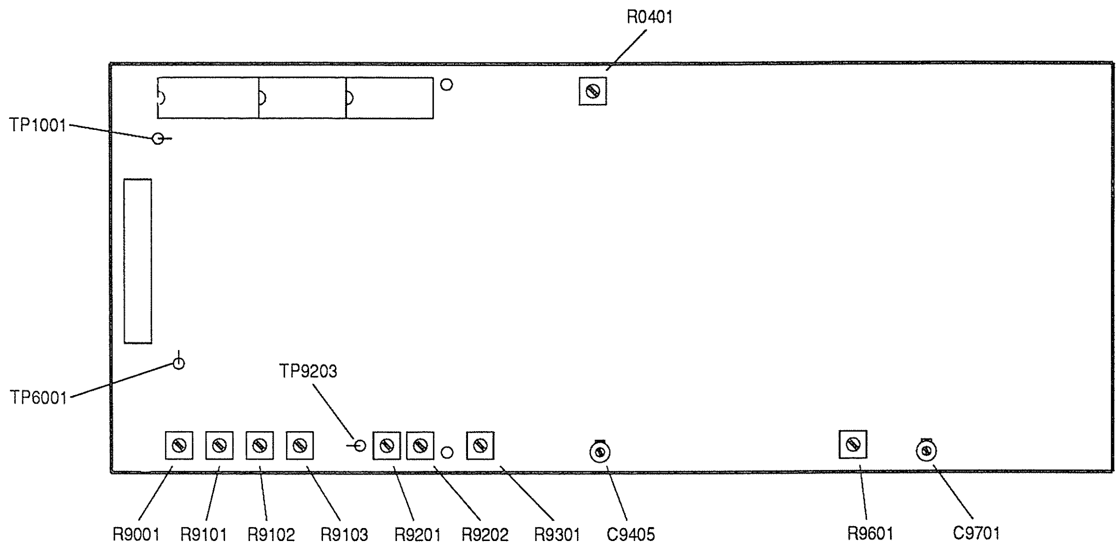


Figure 3.8.10 LVF-1/LVF-2 TEST AND ADJUSTMENT POINTS

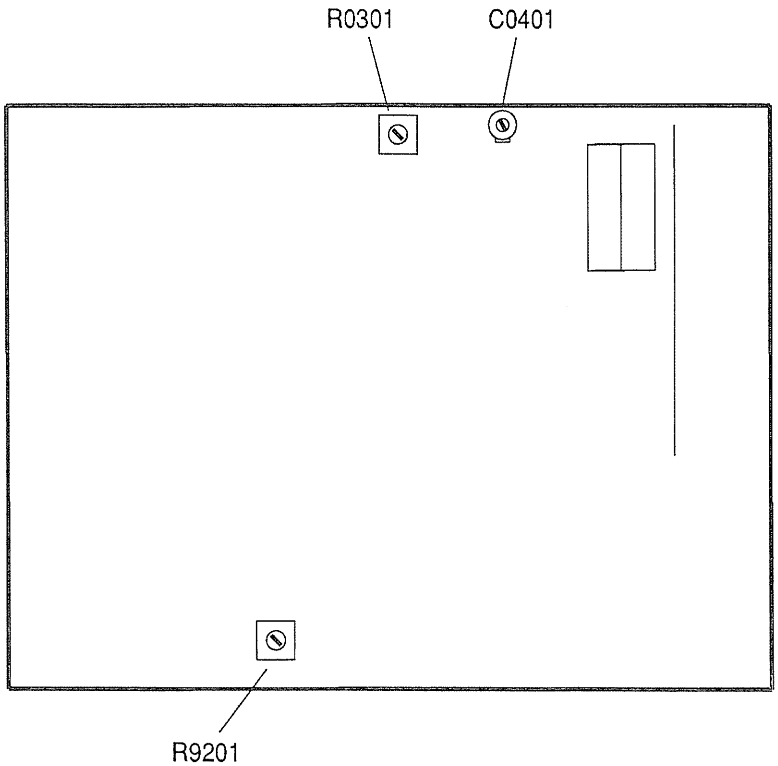


Figure 3.8.11 PHA-1/PHA-2 TEST AND ADJUSTMENT POINTS

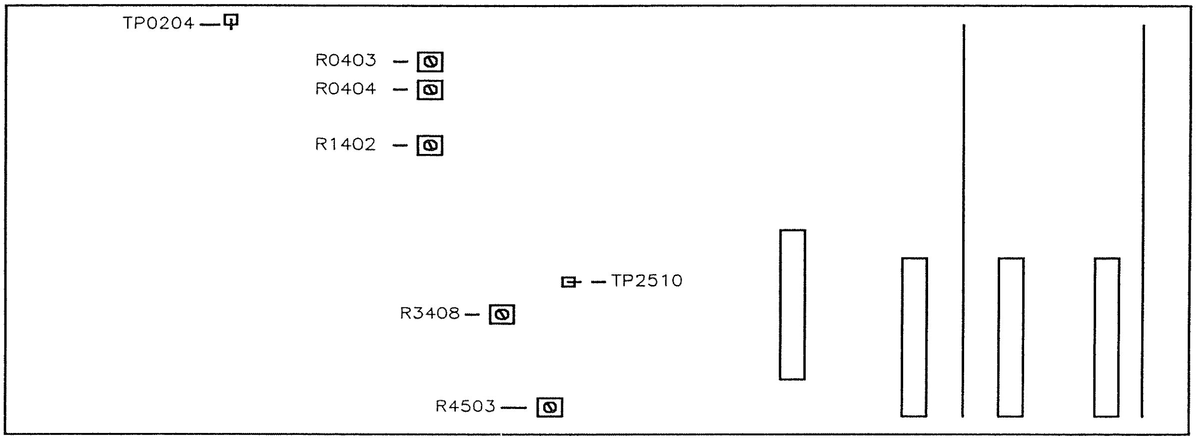


Figure 3.8.12 DIS-1 TEST AND ADJUSTMENT POINTS

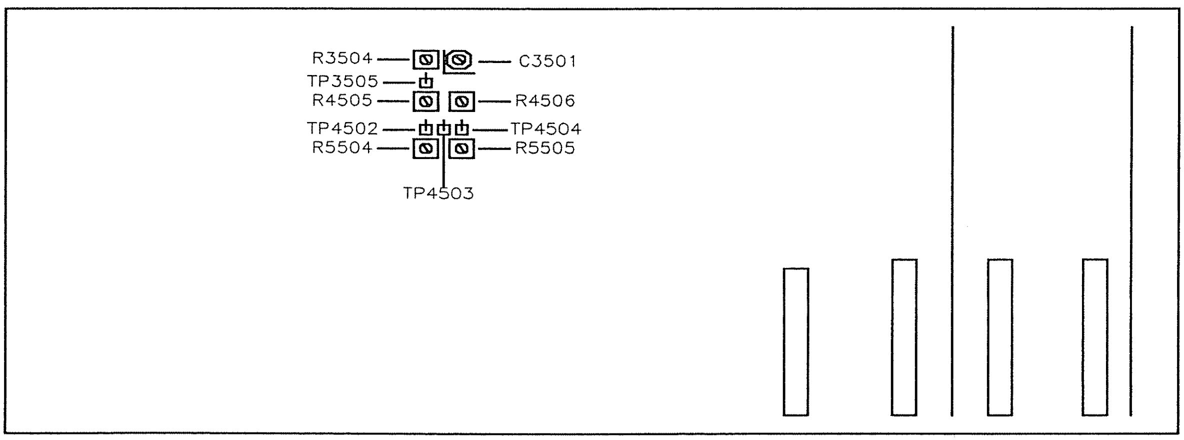


Figure 3.8.13 DIS-2 TEST AND ADJUSTMENT POINTS

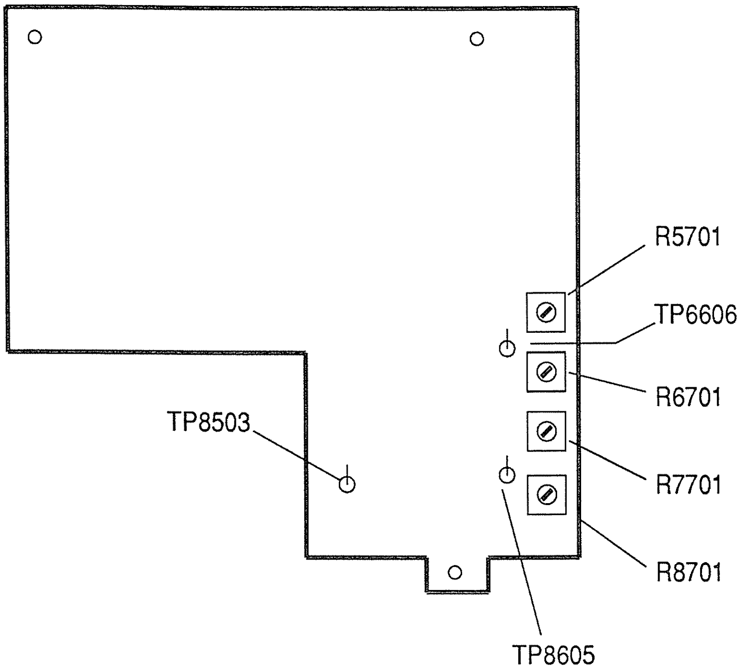


Figure 3.8.14 W&F-1 TEST AND ADJUSTMENT POINTS

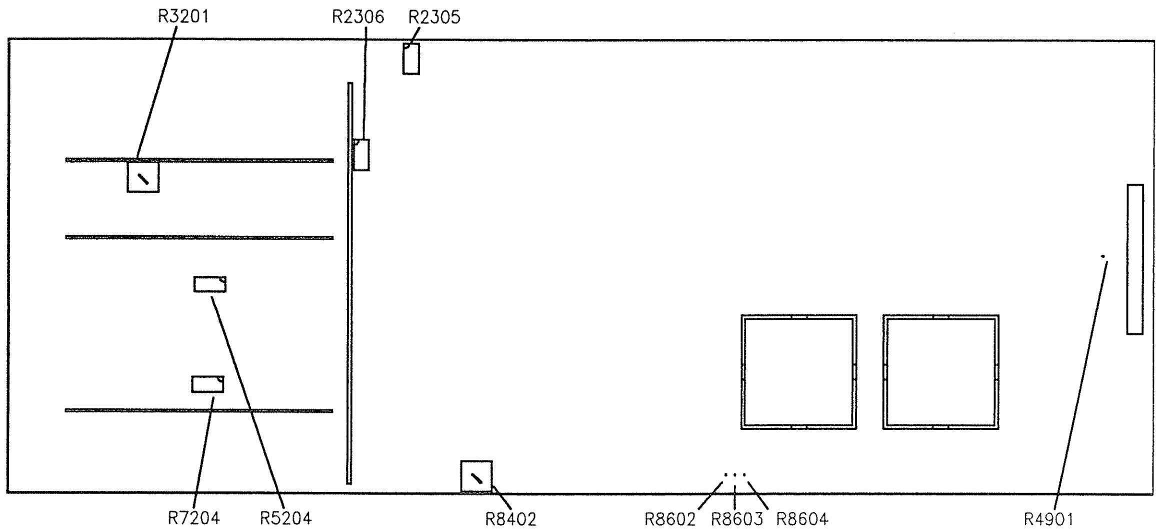


Figure 3.8.15 DSP-1 TEST AND ADJUSTMENT POINTS

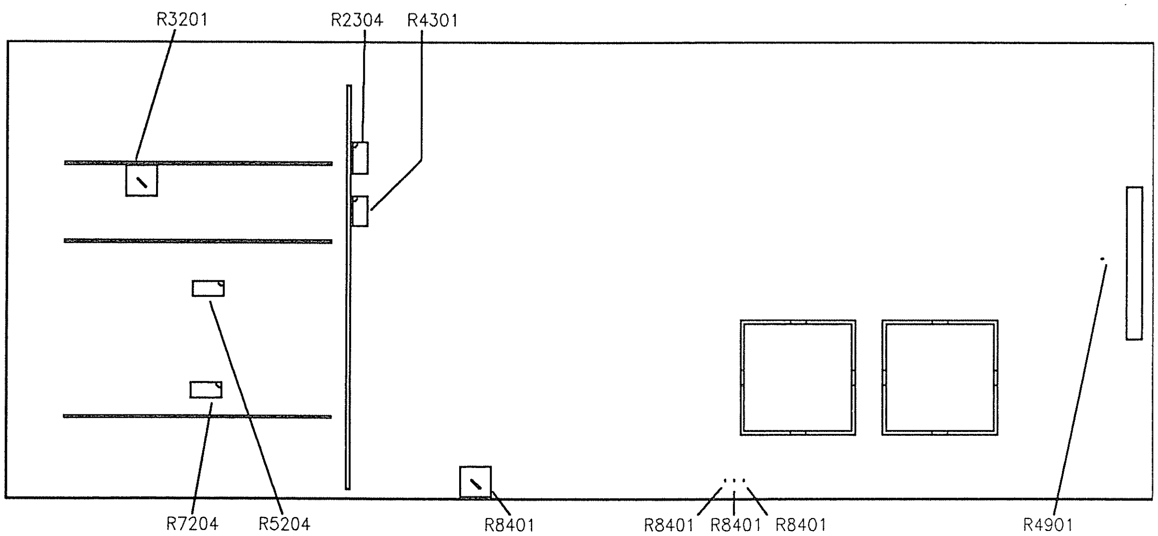


Figure 3.8.16 DSP-2 TEST AND ADJUSTMENT POINTS

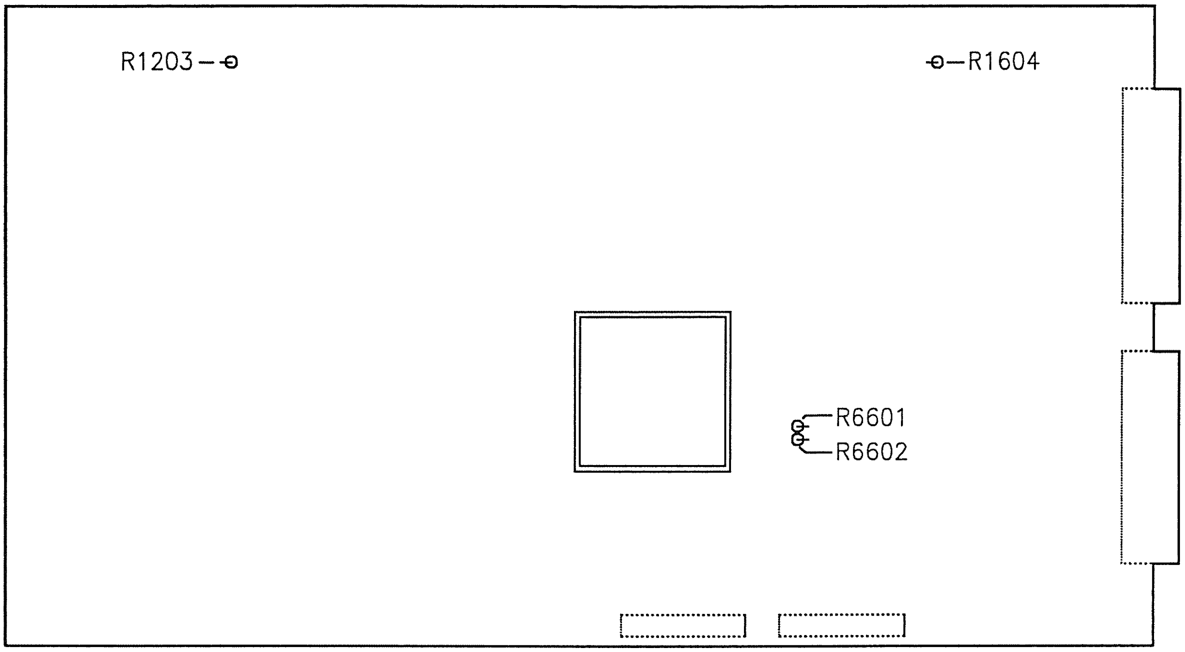


Figure 3.8.17 DIO-1 TEST AND ADJUSTMENT POINTS

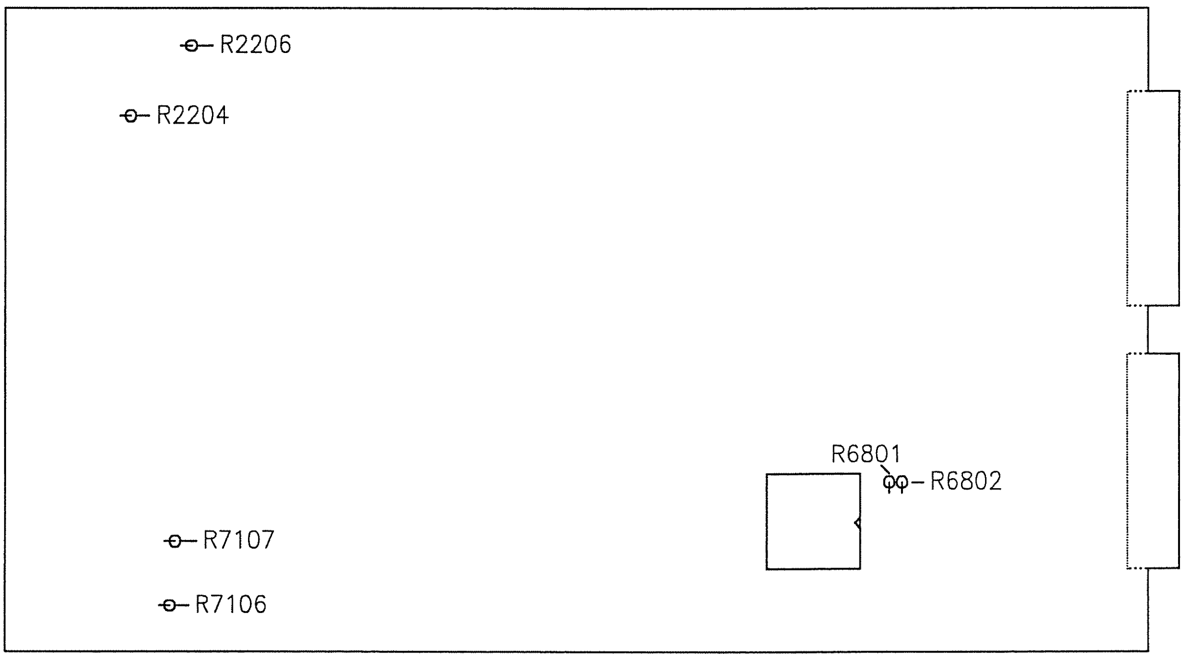


Figure 3.8.18 DIO-2 TEST AND ADJUSTMENT POINTS

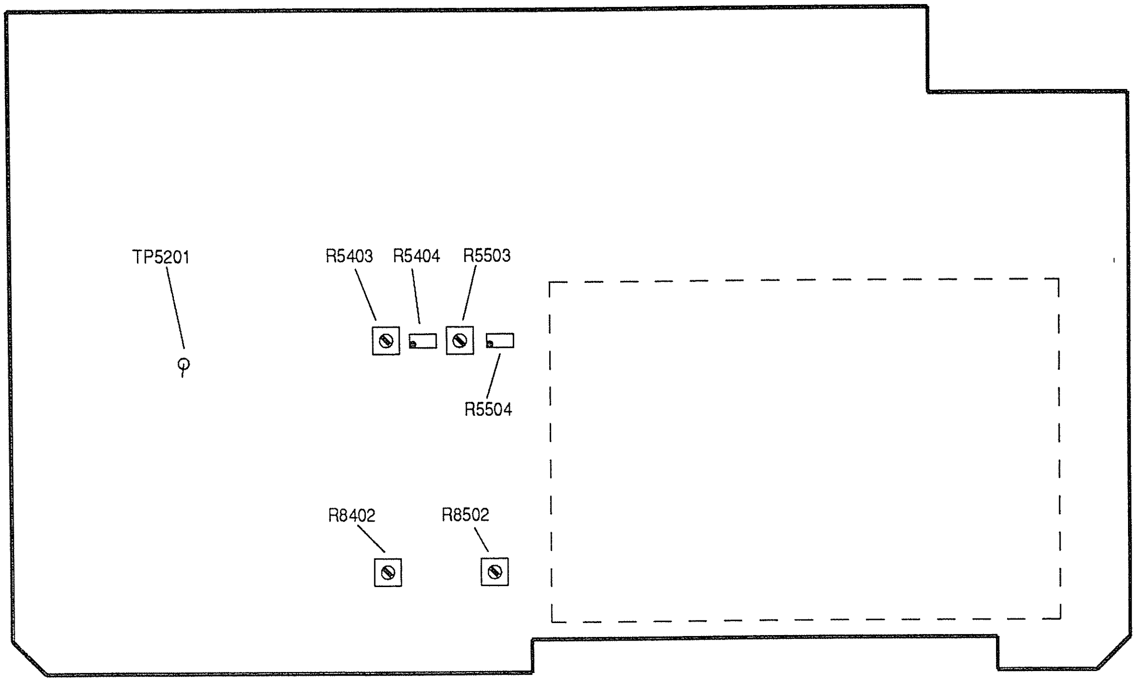


Figure 3.8.19 DCX-127 MAIN BOARD TEST AND ADJUSTMENT POINTS

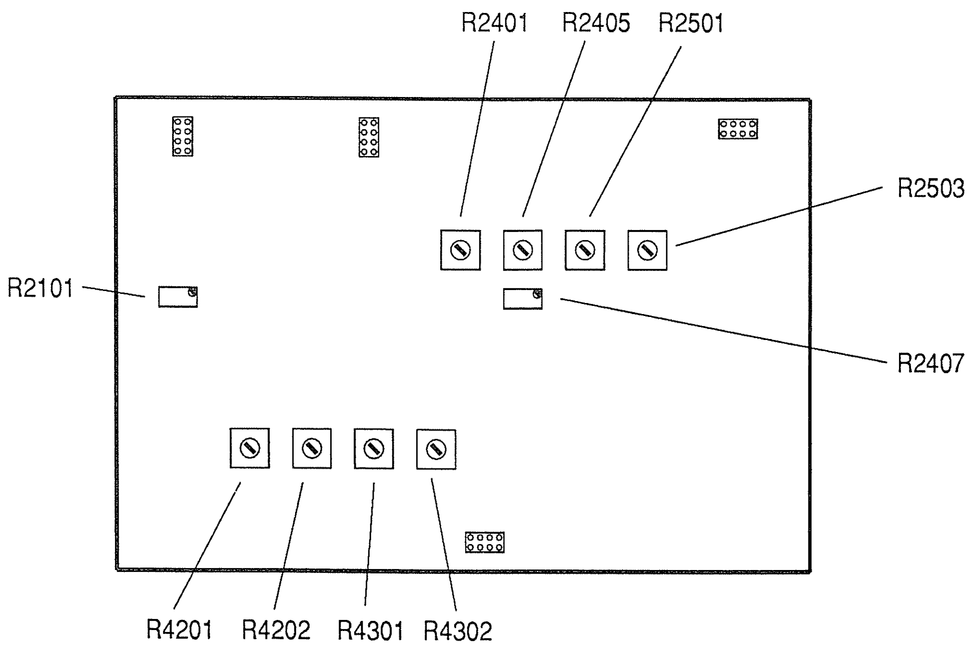


Figure 3.8.20 DCX-127 DMM BOARD TEST AND ADJUSTMENT POINTS

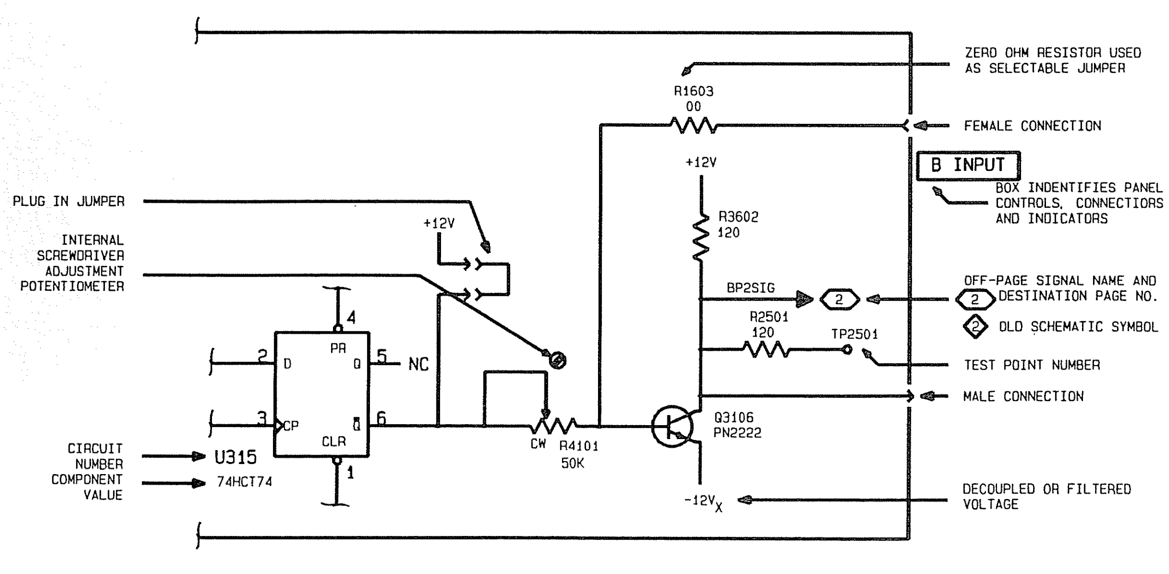
SECTION 4
SYSTEM ONE CIRCUIT DESCRIPTIONS, SCHEMATICS, & ELECTRICAL PARTS LISTS

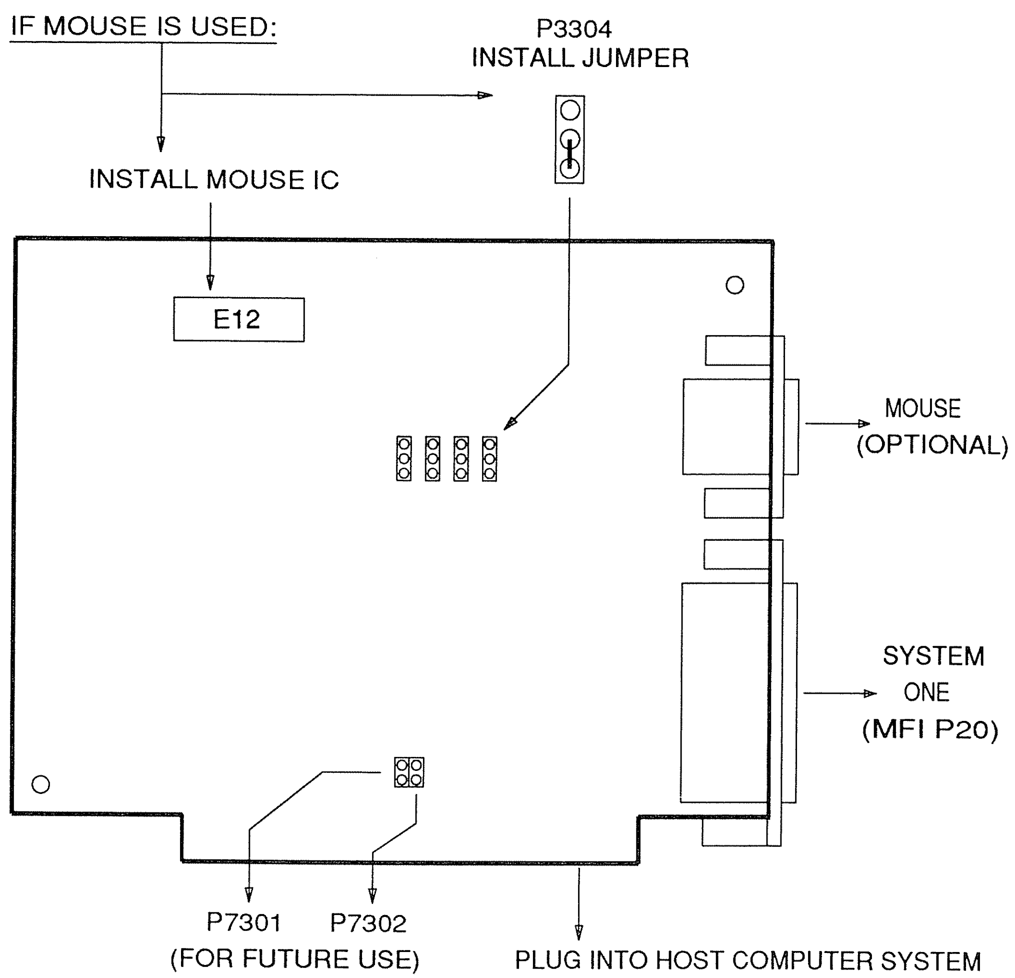
This section contains schematics, circuit descriptions, and electrical parts lists for the System One. All information is believed to be accurate as of the publication date, however Audio Precision reserves the right to make changes without prior notice. If a component value differs from that shown on the schematics use the value of the existing component for replacement purposes, or contact Audio Precision.

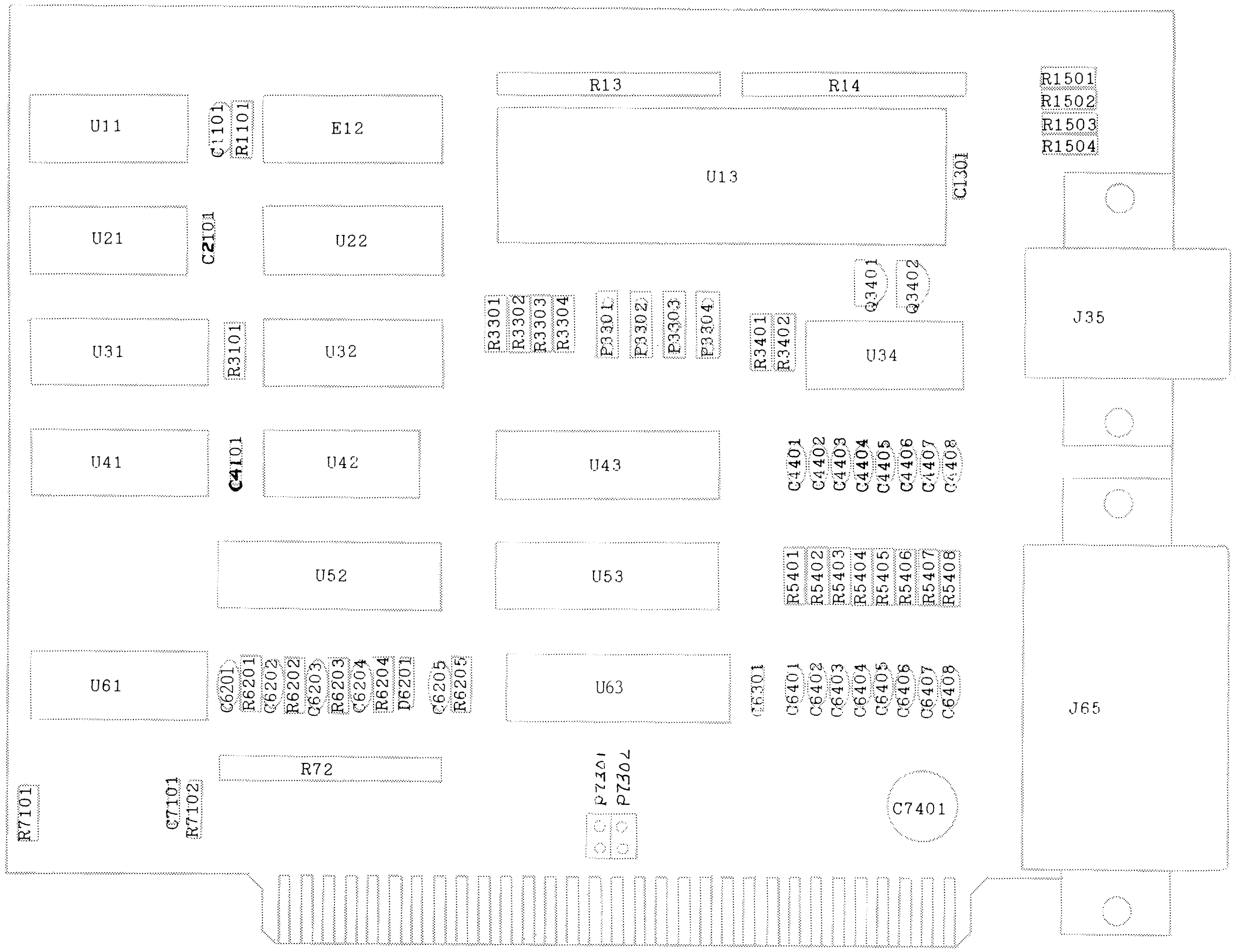
COMPONENT AND ASSEMBLY DESIGNATIONS

A	Assembly
BT	Battery
C	Capacitor, fixed or variable
D	Diode
E	Socket or mechanical part
F	Fuse
H	Heat sink or radiator
HS	Heatsink or mounting hardware
J	Connector, female
K	Relay
L	Inductor, fixed or variable
P	Connector, male
Q	Transistor, FET, or SCR
R	Resistor, fixed or variable
S	Switch or contact
TP	Test Point
U	Integrated Circuit
W	Wirestrap or Cable
X	Transformer
Y	Crystal

SPECIAL SCHEMATIC SYMBOLS




IF MOUSE IS USED:
P3304
INSTALL JUMPER
INSTALL MOUSE IC
E12
MOUSE
(OPTIONAL)
SYSTEM
ONE
(MFI P20)
P7301
P7302
(FOR FUTURE USE)
PLUG INTO HOST COMPUTER SYSTEM



COMPUTER INTERFACE (9PCI.1000)

PCI-1, COMPUTER INTERFACE CARD

NOTE: There are three possible versions of the Audio Precision digital interface board. The **PCI-1** *is a half-size IBM-PC card and contains a* *female* *9-pin connector for the original version Microsoft mouse. The* **PCI-2** *is very similar in appearance to the PCI-1 however it contains a 9-pin* *male* *connector for an auxiliary serial interface. The PCI-1 is obsolete but may still be found in use with older systems. The* **PCI-3** *is designed for the IBM PS/2 family of computers and differs significantly in size and shape.*

Introduction

The PCI-1 computer interface card is installed inside one of the expansion slots of the host computer and allows digital communications between the standard System One software and hardware package. The nature of the interface is unique to Audio Precision and is described in section 1.4.

Mouse Interface <1>

The mouse may be viewed as four switches, two for each axis of motion, which create quadrature pulses as the mouse is moved. Movement in one direction of an axis will cause one of the two switches to lead the other 90 degrees in phase. Reversal of direction will cause the other switch to lead by 90 degrees. By sensing which pulse leads and counting the number of pulses it is possible to track the mouse. This counting is taken care of by the custom IC U12. It contains a pair of 8-bit up/down counters, four 4-bit latches and appropriate decoding logic. The mouse pulses enter from the 9-pin D-subminiature connector and go directly to this IC. The 16 outputs of the 8-bit counters are latched by the 4-bit latches when the latch input transitions high. The data may then be read out four bits at a time from the D0-D3 pins. The control inputs H/L and Y/X are used to select which 4-bit latch is accessed. R1101 and C1101 are used to set the clock rate on a debounce circuit which filters noise from the incoming pulses.

Short Interval Timer <1>

The timer information is obtained by the 12-bit counter U32. The 15 microsecond refresh cycle pulses from the host computer are counted and the eight most significant bits are used. The resulting resolution of the timer is 0.48 msec. The counter will rollover at 122.88 msec. Bit 11 of the counter is also used to drive the host computer interrupt lines to force service of the mouse hardware. When the processor receives the interrupt it reads the 16 bits from the mouse IC and determines how far the mouse has moved since the last interrupt.

The bits to drive the control inputs and to read the data are obtained by an 8255 peripheral interface adaptor. The PIA is programmed by software to make port A, port B and the lower four bits of port C inputs. The upper four bits of port C are used as outputs to control the mouse IC and to enable the mouse interrupts. Port A bits 5, 6, and 7 are used to sense the button switches on the mouse. Provision is made for 3 buttons although the mouse only uses 2. The port B is used to read the short interval timer outputs. Isolation resistors R1501-R1504 and R3301-R3304 are used to guard against U13 port B accidently being programmed to be an output and creating a conflict with U32. Octal bus transceiver U53 is used to drive the bus since the 8255 outputs do not have sufficient current capability. Both the transceiver and U13 are enabled by the /MOUSE signal from <2>.

System One Interface <2>

The System One interface is a byte-wide multiplexed address and data bus. There are 256 addresses available in the System One from the eight bits of address information. The main functions of the interface are mapped into two I/O spaces of the host computer interface bus. One output byte from the host is used as the address byte. The other is used as the data byte. Two additional I/O spaces are used to read the status lines on the interface bus and to force a reset of the System One hardware if desired.

The host portion of the System One interface is shown in schematic <2>. The bus operates by stretching all read and write operations of the host microprocessor bus to approximately 2 usec. The timing circuitry in the lower right hand corner of the schematic generates the memory-not-ready pulses required to slow the microprocessor bus. The address decoding is in the lower left corner of the page and the data buffering is accomplished by the circuitry in the upper portion of the page.

All data going out of the host is buffered by octal bus transceiver U43. The output lines are filtered by C4401 through C4408 to reduce the rise time of the signals and reduce radiated EMI. Data being read from the System One is buffered by the transparent octal latch U63. Filter networks R5401/C6401 through R5408/C6408 reduce noise picked up in the lines. The latch action of U63 holds the data from the previous read operation for the first 0.5 usec of the read operation. For normal read operations which last 2 usec this latch behaves as a buffer, providing output current adequate to drive host interface bus. During DMA input operations the computer does not correctly follow the memory-not-ready protocol. Therefore, when DMA reads are performed the data held in the latch is captured by the computer, introducing a one read delay.

Address Decoding <2>

The address decoding for the mouse interface and the System One interface is performed by U61 and U41. The 1-of-8 selector U61 decodes five unused 32-address blocks in the host I/O space. The dual one of four decoder U41 decodes this further into blocks of four addresses. The available combinations of mouse and System One address locations are given in the accompanying table. When the selected address is accessed the corresponding output of U41 will go low.

The mouse select signal /MOUSE goes to schematic <1> to enable the bus buffer and the 8255. The System One select signal goes through U11B where it is combined with the DMA acknowledge signal. The NAND gate output drives U22 for the final stage of address decoding and U11A where it triggers the memory-not-ready pulse. Nand gate U11D output will go high when either /IOR or /IOW go low. When this occurs and the output of U11B is high there has been a read from or write to one of the addresses occupied by the System One interface.

Wait State Generator <2>

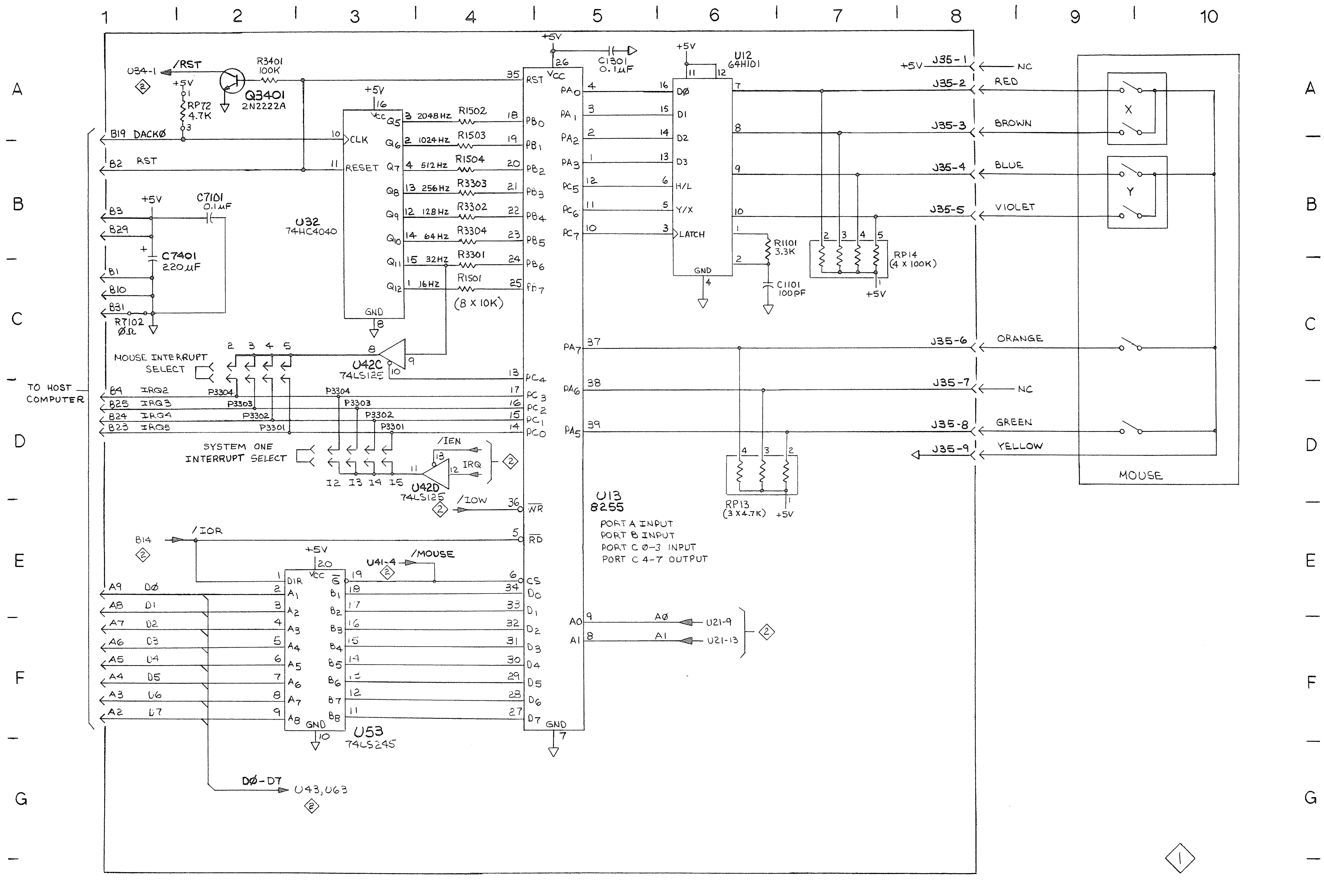
This drives the output of U11A low, turning on tri-state buffer U42B and releasing the counter U31 from reset. The counter is clocked from the 14 MHz master clock of the host computer, allowing repeatable timing of the wait states. The outputs start from the low state, forcing a low on the IOCHRDY line through U42B. This tells the host microprocessor to wait while the write or read cycle is completed. At the end of the 2 usec interval the QAb output of U31 will go high, releasing the processor from the wait state. An earlier output from the counter (at 1.5 usec) is used to force the write strobe line (EW) on the System One interface to finish its pulse before the host processor is released from the wait state. This guarantees that the data to be latched into the System One is still valid when the strobe pulse reaches the end of the cable.

Bus Drive <2>

The decoder U22 decodes the write and read operations to drive the appropriate strobe lines on the System One interface. The selected output of U22 will go low to implement the appropriate function. The 1Y3 output is enabled for data writes, driving the interface line EW high via inverter U52C. The 1Y2 output goes low for address writes driving the interface line EA high through U52B. The 1Y1 output is used to control the enabling of interrupts from the System One via U34A and to clear pending interrupts in U34B. The 1Y0 output drives the System One interface reset line through Q3402, allowing the line ERST to go high, resetting all hardware modules.

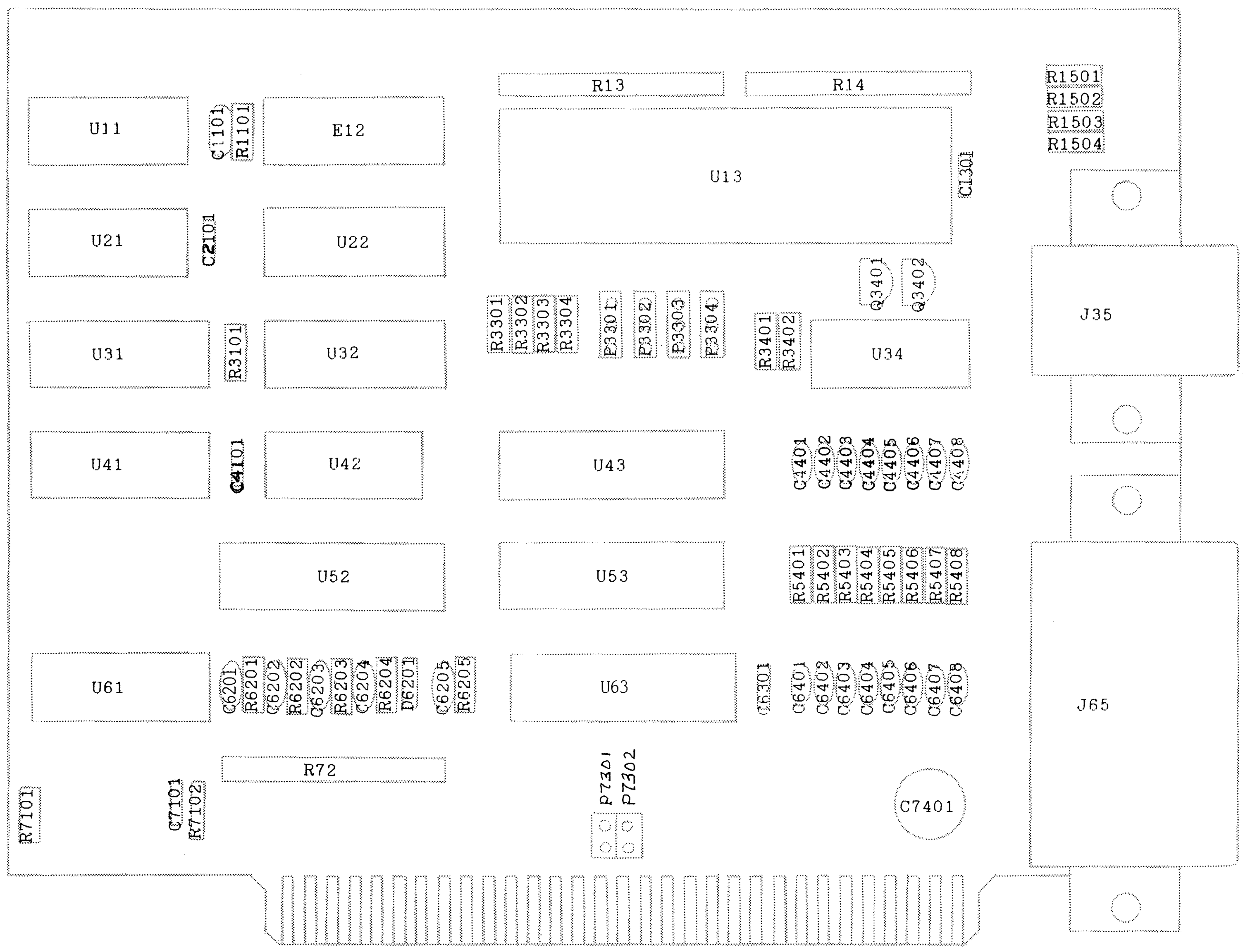
The 2Y3 output of U22 goes low for data reads from the System One. This enables the output of the tri-state latch U63 and places the stored data it contains onto the host computers bus. After a 0.5 usec delay introduced by R6204 and C6204 the output of U52D will go high. This places U63 into the transparent state and enables normal read operation. This output also drives the line ER on the System One interface, causing devices in the System One to place their data on the interface. The diode D6201 is used to charge C6204 quickly after a read operation so that another can be performed immediately afterward. The 2Y3 output of U22 drives the 4-bit tri-state buffer U52E and tri-state buffer U42A. The five buffer outputs drive the host bus allowing read of the three System One status lines, reading the state of the interrupt line and reading the state of flip-flop U34B which latches any occurrence of an interrupt.

During DMA transfers the /AEN line from the host bus will go high. This will shut down the address decoder U61 and force the address selection inputs of U22 high via U21C and U21D. This sets U22 for reads and writes from whatever System One address has previously been written to the hardware. During DMA transfers the /DACK1 or /DACK3 line will go low. This will drive the other input of U11B and initiate a read or write cycle as described above.

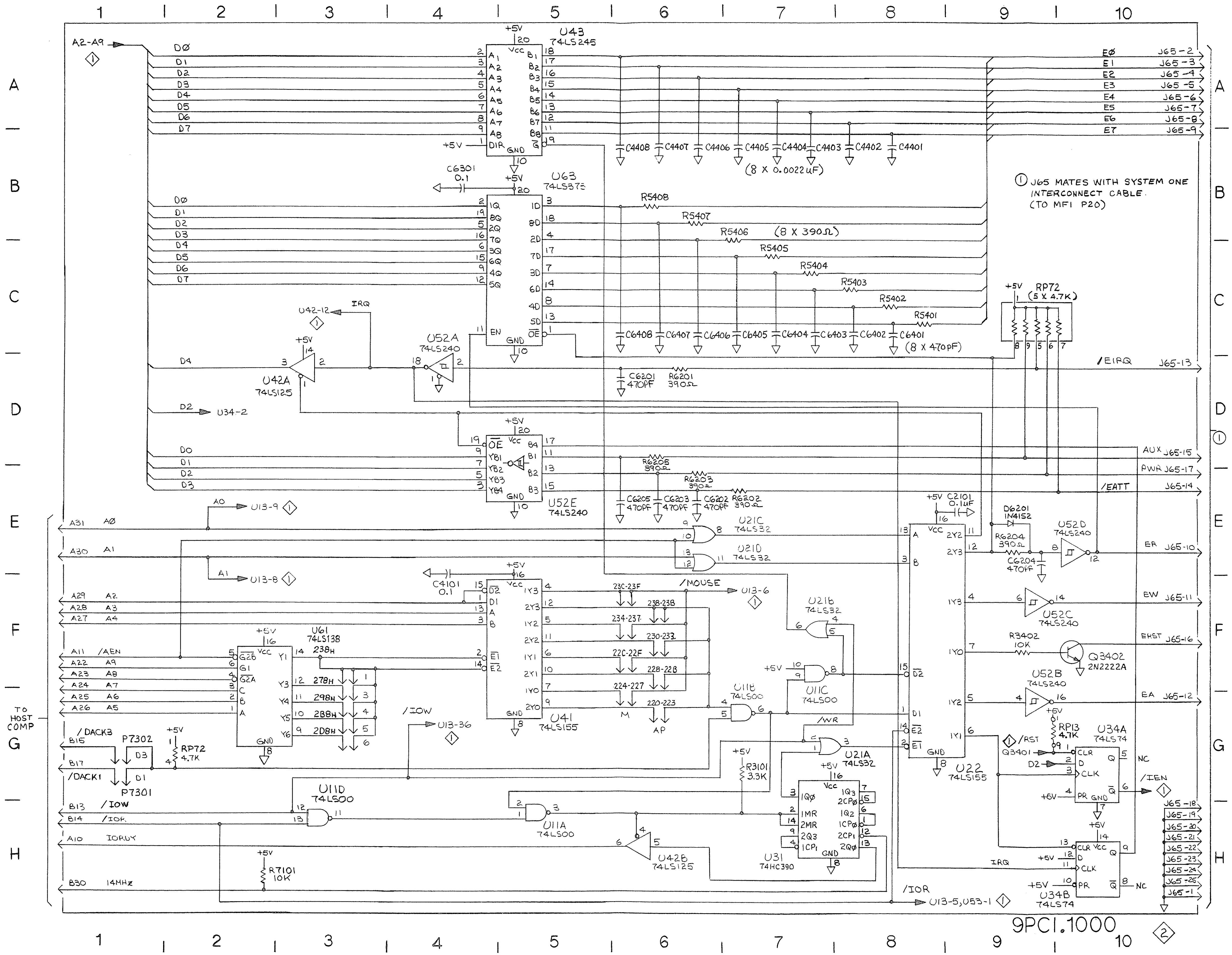


9PC1.1000
SHT 1 of 2

2-10-86 VGT
9-18-86 VGT



COMPUTER INTERFACE (9PCI.1000)



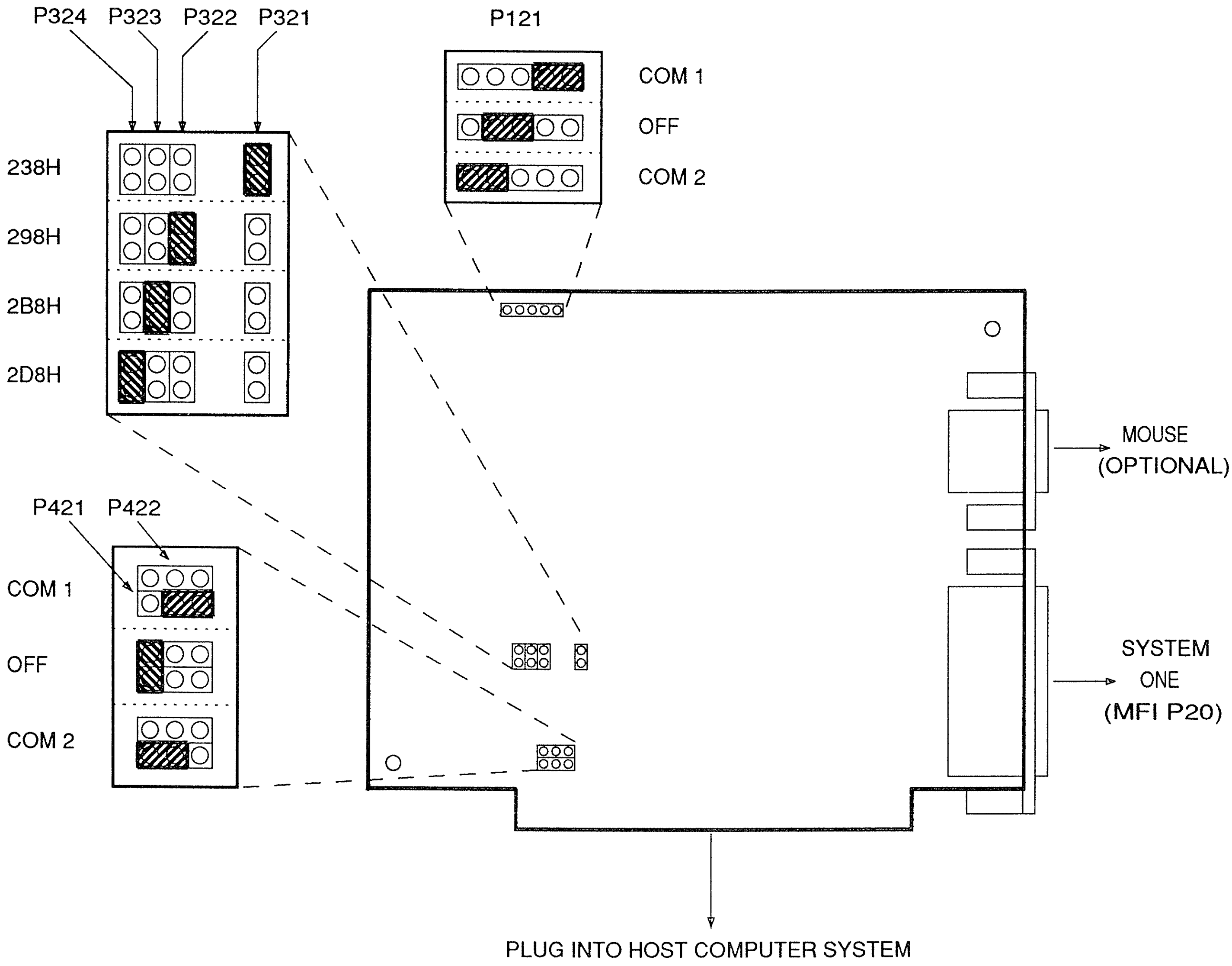
U43 74LS245
U63 74LS373
U42A 74LS125
U52A 74LS240
U52E 74LS240
U61 74LS138
U41 74LS155
U22 74LS155
U21A 74LS32
U21B 74LS32
U21C 74LS32
U21D 74LS32
U11A 74LS00
U11B 74LS00
U11C 74LS00
U11D 74LS00
U31 74HC390
U42B 74LS125
U34A 74LS74
U34B 74LS74
U52B 74LS240
U52C 74LS240
U52D 74LS240
Q3402 2N2222A
(8 X 0.0022uF)
(8 X 390Ω)
(8 X 470pF)
RP72 (5 X 4.7K)
① J65 MATES WITH SYSTEM ONE INTERCONNECT CABLE. (TO MFI P20)
TO HOST COMP
/MOUSE
/IOW
/IOR
IORDY
14MHz
/EIRQ
/EATT
/IEN

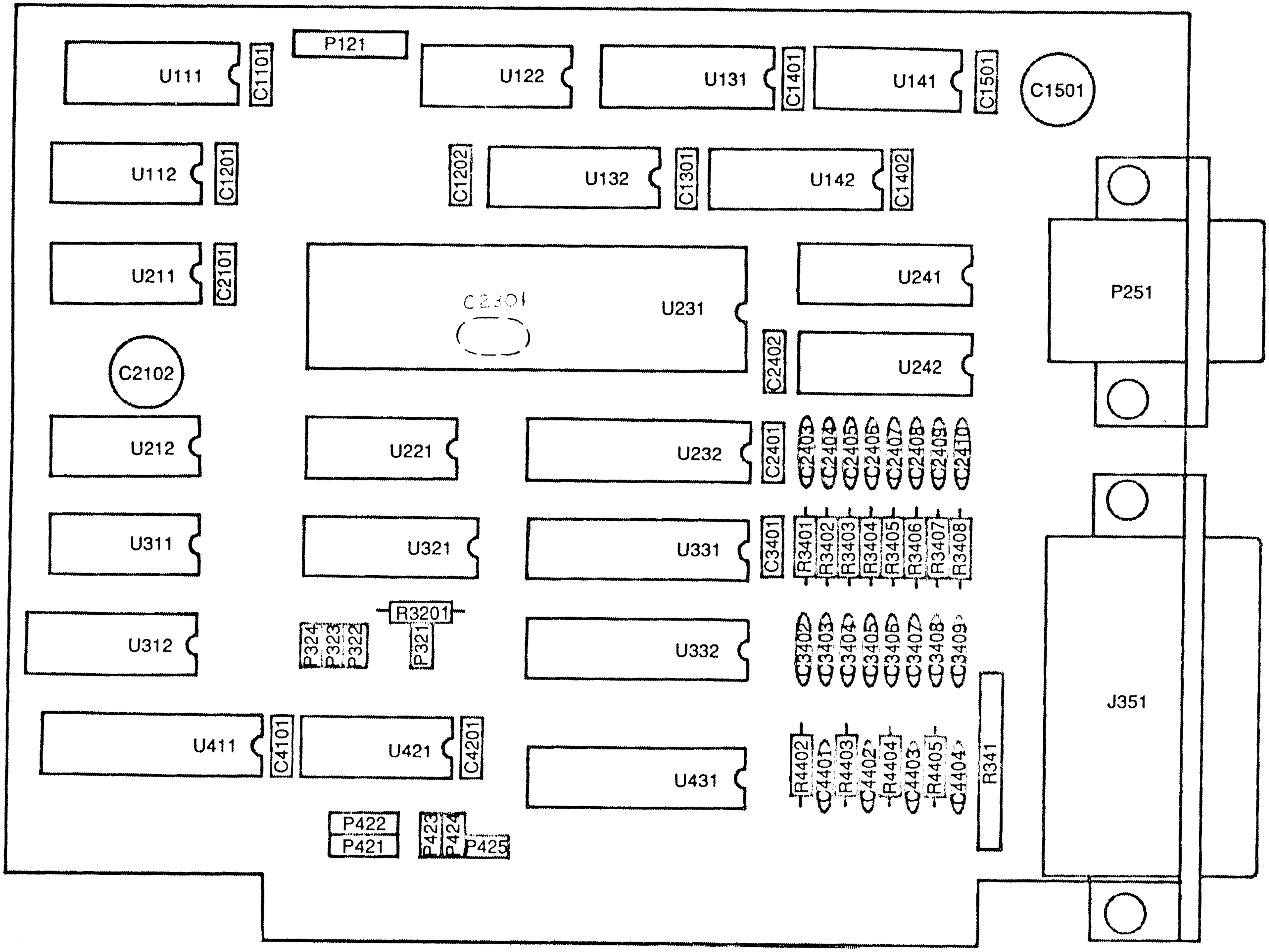
9PC1.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION		
C1101	1C6	2296.0101	CAP MICA 500V 1%		100pF
C1301	1A5	2172.0104	CAP CERAM 100V 20%		.1uF
C2101	2E9	2172.0104	CAP CERAM 100V 20%		.1uF
C4101	2E4	2172.0104	CAP CERAM 100V 20%		.1uF
C4401	2B8	2172.0222	CAP CERAM 100V 20%		.0022uF
C4402	2B8	2172.0222	CAP CERAM 100V 20%		.0022uF
C4403	2B7	2172.0222	CAP CERAM 100V 20%		.0022uF
C4404	2B7	2172.0222	CAP CERAM 100V 20%		.0022uF
C4405	2B7	2172.0222	CAP CERAM 100V 20%		.0022uF
C4406	2B6	2172.0222	CAP CERAM 100V 20%		.0022uF
C4407	2B6	2172.0222	CAP CERAM 100V 20%		.0022uF
C4408	2B6	2172.0222	CAP CERAM 100V 20%		.0022uF
C6201	2D6	2172.0471	CAP CERAM 100V 20%		470pF
C6202	2E6	2172.0471	CAP CERAM 100V 20%		470pF
C6203	2E6	2172.0471	CAP CERAM 100V 20%		470pF
C6204	2E9	2172.0471	CAP CERAM 100V 20%		470pF
C6205	2E6	2172.0471	CAP CERAM 100V 20%		470pF
C6301	2B4	2172.0104	CAP CERAM 100V 20%		.1uF
C6401	2C8	2172.0471	CAP CERAM 100V 20%		470pF
C6402	2C8	2172.0471	CAP CERAM 100V 20%		470pF
C6403	2C7	2172.0471	CAP CERAM 100V 20%		470pF
C6404	2C7	2172.0471	CAP CERAM 100V 20%		470pF
C6405	2C7	2172.0471	CAP CERAM 100V 20%		470pF
C6406	2C6	2172.0471	CAP CERAM 100V 20%		470pF
C6407	2C6	2172.0471	CAP CERAM 100V 20%		470pF
C6408	2C6	2172.0471	CAP CERAM 100V 20%		470pF
C7101	1B2	2172.0104	CAP CERAM 100V 20%		.1uF
C7401	1B1	2911.0227	CAP AL-EL 10V +80/-20%		220uF
D6201	2E9	3120.0000	DIODE SCHOTTKY		1SS97
J33		4220.1002	JACK MINI-JUMPER		2 PIN
J35	1A8	4225.0009	JACK D-SUB PC 90°		9 PIN
J65	2A10	4225.0025	JACK D-SUB PC 90°		25 PIN
P3301	1D2,1D3	4221.0036	PLUG PC	.1 X.43	36 PIN
P3302	1D2,1D3	4221.0036	PLUG PC	.1 X.43	36 PIN
P3303	1D2,1D3	4221.0036	PLUG PC	.1 X.43	36 PIN
P3304	1D2,1D3	4221.0036	PLUG PC	.1 X.43	36 PIN
Q3401	1A2	3211.2222	XSTR NPN TO92		PN2222A
Q3402	2F10	3211.2222	XSTR NPN TO92		PN2222A
R1101	1B6	1214.0332	RES 1/4W C FLM 5%		3.3K
R13	1D6,2G9	1984.9472	RES NET SIP 5%		9 X 4.7K
R14	1B7	1984.9104	RES NET SIP 5%		9 X 100K
R1501	1C4	1214.0103	RES 1/4W C FLM 5%		10K
R1502	1A4	1214.0103	RES 1/4W C FLM 5%		10K
R1503	1A4	1214.0103	RES 1/4W C FLM 5%		10K
R1504	1B4	1214.0103	RES 1/4W C FLM 5%		10K
R3101	2G7	1214.0332	RES 1/4W C FLM 5%		3.3K
R3301	1C4	1214.0103	RES 1/4W C FLM 5%		10K

Replaceable Electrical Parts List: 9PCI.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R3302	1B4	1214.0103	RES 1/4W C FLM 5%	10K
R3303	1B4	1214.0103	RES 1/4W C FLM 5%	10K
R3304	1B4	1214.0103	RES 1/4W C FLM 5%	10K
R3401	1A2	1214.0104	RES 1/4W/C/FLM 5%	100K
R3402	2F9	1214.0103	RES 1/4W C FLM 5%	10K
R3403	2F10	1214.0391	RES 1/4W C FLM 5%	390
R5401	2C8	1214.0391	RES 1/4W C FLM 5%	390
R5402	2C8	1214.0391	RES 1/4W C FLM 5%	390
R5403	2C8	1214.0391	RES 1/4W C FLM 5%	390
R5404	2C7	1214.0391	RES 1/4W C FLM 5%	390
R5405	2C7	1214.0391	RES 1/4W C FLM 5%	390
R5406	2C7	1214.0391	RES 1/4W C FLM 5%	390
R5407	2B6	1214.0391	RES 1/4W C FLM 5%	390
R5408	2B6	1214.0391	RES 1/4W C FLM 5%	390
R6201	2D6	1214.0391	RES 1/4W C FLM 5%	390
R6202	2E7	1214.0391	RES 1/4W C FLM 5%	390
R6203	2E6	1214.0391	RES 1/4W C FLM 5%	390
R6204	2E9	1214.0391	RES 1/4W C FLM 5%	390
R6205	2D6	1214.0391	RES 1/4W C FLM 5%	390
R7101	2H2	1214.0103	RES 1/4W C FLM 5%	10K
R7102	1C1	1214.0000	JUMPER .4 X.25	00
R72	1A2,2C9,2G2	1984.9472	RES NET SIP 5%	9 X 4.7K
U11	2F7,2G7,2H3,2H5	3313.0000	GATE 4 X 2-IN NAND	74LS00
U13	1D5	3332.8255	INTERFACE PERIPH PROG	8255
U21	2E6,2F7,2G7	3313.0032	GATE 4 X 2-IN OR	74LS32
U22	2E8	3313.0155	DECODER 2 X 2-LN/4-LN	74LS155
U31	2H7	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U32	1B3	3323.4040	COUNTER 12-STAGE	74HC4040
U34	2G10,2H10	3313.0074	FLIP-FLOP 2X J-K	74LS74
U41	2F5	3313.0155	DECODER 2 X 2-LN/4-LN	74LS155
U42	1C3,1D4,2D3,2H6	3313.0125	BUFFER 4X TRI-STATE	74LS125
U43	2A5	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U52	2D4,2D5,2E10,2F9,2G9	3313.0240	BUFFER 8X INV TRI-ST	74LS240
U53	1F3	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U61	2F2	3313.0138	DECODER 3-LINE/8-LINE	74LS138
U63	2C5	3313.0373	LATCH 8X D TRI-ST	74LS373


P324
P323
P322
P321
238H
298H
2B8H
2D8H
P121
COM 1
OFF
COM 2
P421
P422
COM 1
OFF
COM 2
MOUSE
(OPTIONAL)
SYSTEM
ONE
(MFI P20)
PLUG INTO HOST COMPUTER SYSTEM



COMPUTER INTERFACE 9PCI.2000 (6200.PCI2.5)

PCI-2, COMPUTER INTERFACE CARD

NOTE: There are three possible versions of the Audio Precision digital interface board. The **PCI-1** *is a half-size IBM-PC card and contains a* *female* *9-pin connector for the original version Microsoft mouse. The* **PCI-2** *is very similar in appearance to the PCI-1 however it contains a 9-pin* *male* *connector for an auxiliary serial interface. The PCI-1 is obsolete but may still be found in use with older systems. The* **PCI-3** *is designed for the IBM PS/2 family of computers and differs significantly in size and shape.*

Introduction

The PCI-2 computer interface card is installed inside one of the expansion slots of the host computer and allows digital communications between the standard System One software and hardware package. The nature of the interface is unique to Audio Precision and is described in section 1.4.

Address Decoding <2>

The address decoding for the PCI card is performed by U321 and U421. The 1-of-8 selector U321 and NAND gate U421D decode four unused blocks of 16 addresses in the host I/O space. They also decode the $2F8/$3F8 select signal required for the serial port. The two NAND gates U421B and U421C in combination with OR gate U221B decode this further into blocks of four addresses. The available System One base address locations are therefore $238, $298, $2B8 and $2D8. When the selected address is accessed the output of U221B will go low.

The original PCI-1 version of this card included a mouse interface and used one of the mouse ports as a timer. To retain compatibility with old software the timer port on the PCI-2 card is mapped into both old and new addresses. This is accomplished by U421A and the inverter U411.

Communications addresses in the host computer are located at either $2F8 or $3F8. All address bits except A0 through A2 and A8 are decoded by U321 which goes low when the appropriate address is received. Its output drives the active low chip select of U231 while A8 is used to drive the active high input of U231. Jumper P121 inverts the A8 address line to select between COM 1 ($3F8) and COM 2 ($2F8). Address lines A0 through A2 drive the NS16450 UART directly to decode registers internal to it.

Clock Generation <1>

Clocks for the serial port and the short interval timer on the PCI card are provided by dividing the 14.318 MHz host computer clock with U131. A 1.7898 MHz signal and a 55.93 kHz signal are combined by U141A and U122B to provide the 1.8458 MHz master clock for the serial interface. The 55.93 kHz signal is combined with a 27.96 kHz signal in U122B to obtain an 83.9 kHz clock for the short interval timer. This is divided by 20 in U242, resulting in a 4.195 kHz clock.

Short Interval Timer <1>

The 241 usec clock pulses are counted by 8-bit counter U241, giving a resolution of approximately 241 usec. This is read by the processor when the 2Y1 output of U312 pulses low. The low going edge of the read strobe is inverted by U122D to create a high going edge to latch the count into U241's output buffers. This timer data is present at the outputs of U241 when the enable input (pin 14) is low. Since the output current capability of U241 is insufficient to drive the bus, octal buffer U232 is used. AND gate U211C combines the enable signals from both the UART U231 and the timer U241.

Serial Interface <1>

The serial interface is implemented with an NS16450 universal asynchronous receiver/transmitter (UART). It provides the necessary parallel to serial conversion, baud rate generation and some address decoding. Eight of the RS232 interface signals are implemented; TX and RX (transmit and receive data), RTS (ready to send), DTR (data terminal ready), CTS (clear to send), DSR (data set ready), DCD (data carrier detect) and RI (ring indicator).

The UART U231 operates at TTL levels, interfacing to the ±12 volt levels of RS232 is accomplished by inverting buffers U132 and U142. Since the NS16450 outputs do not have sufficient current capability, octal bus transceiver U232 is used to drive the host computer bus. AND gate U211C combines the enable signals from both the UART U231 and the timer U241.

The interrupt output from U231 is combined with the read strobe signal by AND gate U211D. This is buffered by tri-state buffer U112A and drives the interrupt bus of the host computer. Jumper P421 selects between the IRQ 3 and IRQ 4 for RS 232 operation. IRQ 4 is used for COM 1 and IRQ 3 is used for COM 2.

System One Interface <2>

The System One interface is a byte-wide multiplexed address and data bus. There are 256 addresses available in the System One from the eight bits of address information. The main functions of the interface are mapped into two I/O spaces of the host computer interface bus. One output byte from the host is used as the address byte. The other is used as the data byte. Two additional I/O spaces are used to read the status lines on the interface bus and to force a reset of the System One hardware if desired.

The bus operates by stretching all read and write operations of the host microprocessor bus to approximately 2 usec. The timing circuitry, consisting of U111 and U112B generates the memory-not-ready pulses required to slow the microprocessor bus.

All data going out of the host is buffered by octal bus transceiver U332. The output lines are filtered by C3402 through C3409 to reduce the rise time of the signals and reduce radiated EMI. Data being read from the System One is buffered by the transparent octal latch U331. Filter networks R3401/C2403 through R3408/C2410 reduce noise picked up in the lines. The latch action of U331 holds the data from the previous read operation for the first 0.5 usec of a new read operation. For normal read operations which last 2 usec this latch behaves as a buffer, providing output current adequate to the drive host interface bus. During DMA input operations the computer does not correctly follow the memory-not-ready protocol. Therefore, when DMA reads are performed the data held in the latch is captured by the computer, introducing a one read delay.

Wait State Generator <2>

The System One select signal goes through U211A where it is combined with the DMA acknowledge signal. The AND gate output enables decoder U312 and drives U221B where it triggers the memory-not-ready pulse. AND gate U211D output will go low when either /IOR or /IOW go low. When this occurs and the output of U211A is low there has been a read from or write to one of the addresses occupied by the System One interface. This drives the output of U221B low, turning on tri-state buffer U112D and releasing the counter U111 from reset.

The counter is clocked from the 14 MHz master clock of the host computer, allowing repeatable timing of the wait states. The outputs start from the low state, forcing a low on the IOCHRDY line through U112B. This tells the host microprocessor to wait while the write or read cycle is completed. At the end of the approximately 2 usec interval the QAb output of U111 will go high, releasing the processor from the wait state. An earlier output from the counter (at 1.5 usec) is used to force the write strobe line (EW) on the System One interface to finish its pulse before the host processor is released from the wait state. This guarantees that the data to be latched into the System One is still valid when the strobe pulse reaches the end of the cable.

Bus Drive <2>

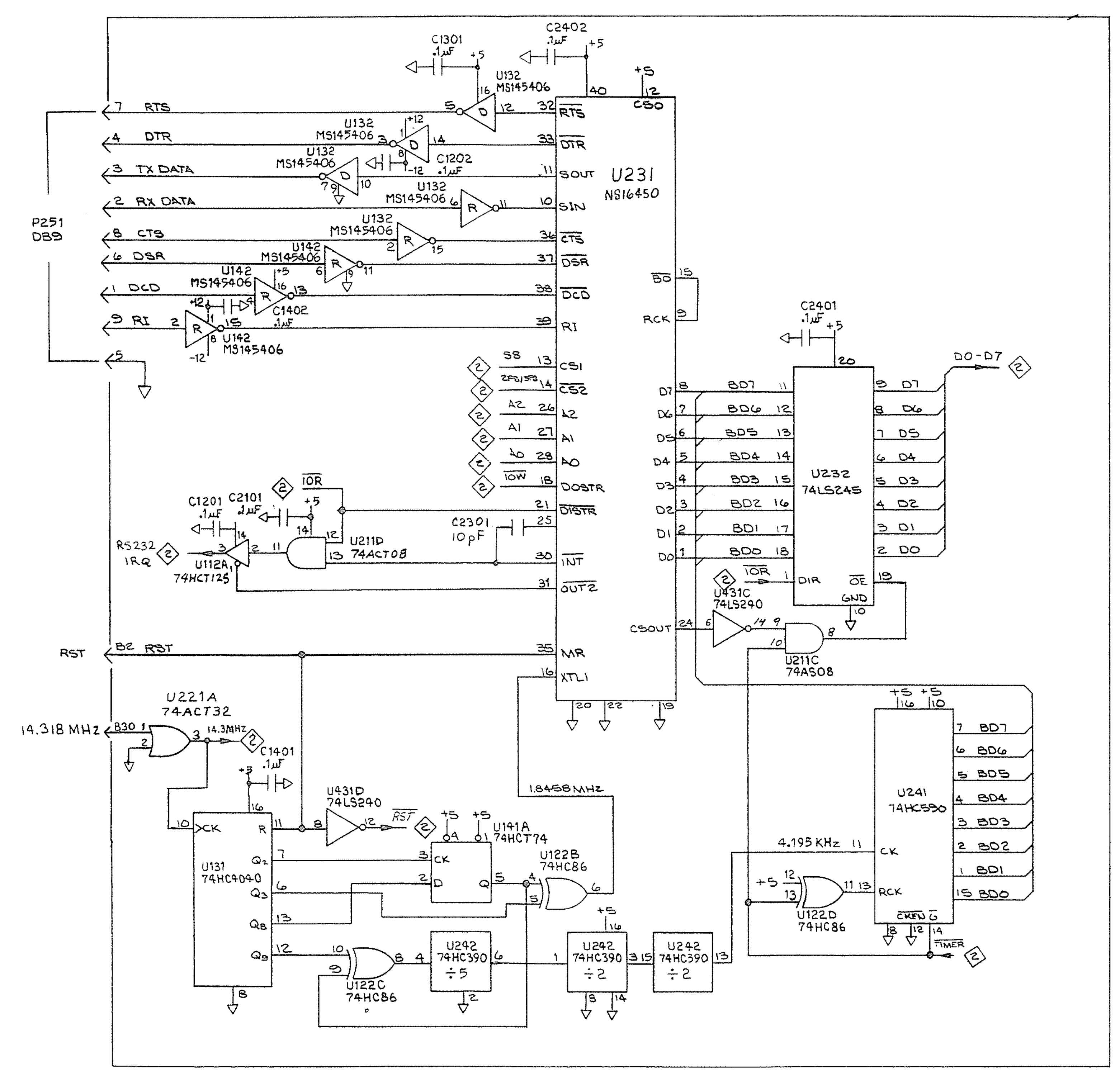
The decoder U312 decodes the write and read operations to drive the appropriate strobe lines on the System One interface. The selected output of U312 will go low to implement the appropriate function. The 1Y3 output is enabled for data writes, driving the interface EW line high via inverter U411D. The 1Y2 output goes low for address writes driving the interface EA line high through U411C. The 1Y1 output is used to control the enabling of interrupts from the System One via U212A and to clear pending interrupts in U212B. The 1Y0 output drives the System One interface reset line through U411D, forcing the ERST line high and resetting all hardware modules.

The 2Y3 output of U312 goes low for data reads from the System One. This enables the output of the tri-state latch U331 and places the stored data it contains onto the host computer's bus. Following a 0.5 usec delay introduced by U141B and U411H the /Q output of U141B will go high. This places U331 into the transparent state and enables normal read operation. The Q output drives the ER line on the System One interface through U411A, causing devices in the System One to place their data on the interface. The U411H is used to preset U141B after a read operation so that another can be performed immediately afterward. The 2Y3 output of U312 drives the 4-bit tri-state buffer U431E-H and tri-state buffer U112D. The five buffer outputs drive the host bus allowing read of the three System One status lines, reading the state of the interrupt line and reading the state of flip-flop U212B which latches any occurrence of an interrupt.

During DMA transfers the /AEN line from the host bus will go high. This will shut down the address decoder U321 and force the address selection inputs of U312 high via U311C and U311D. This sets U312 for reads and writes from whatever System One address has previously been written to the hardware. During DMA transfers the /DACK1 or /DACK3 line will go low. This will drive the input of U211B and initiate a read or write cycle as described above.

PCI-2 Interface Addressing

The addresses occupied by the Audio Precision Interface may be selected by jumpers on the circuit card. The card is shipped with the jumpers set to place the System One ports at 238 to 23B hex. Please refer to the Users Manual if it is necessary to move the hardware port locations.

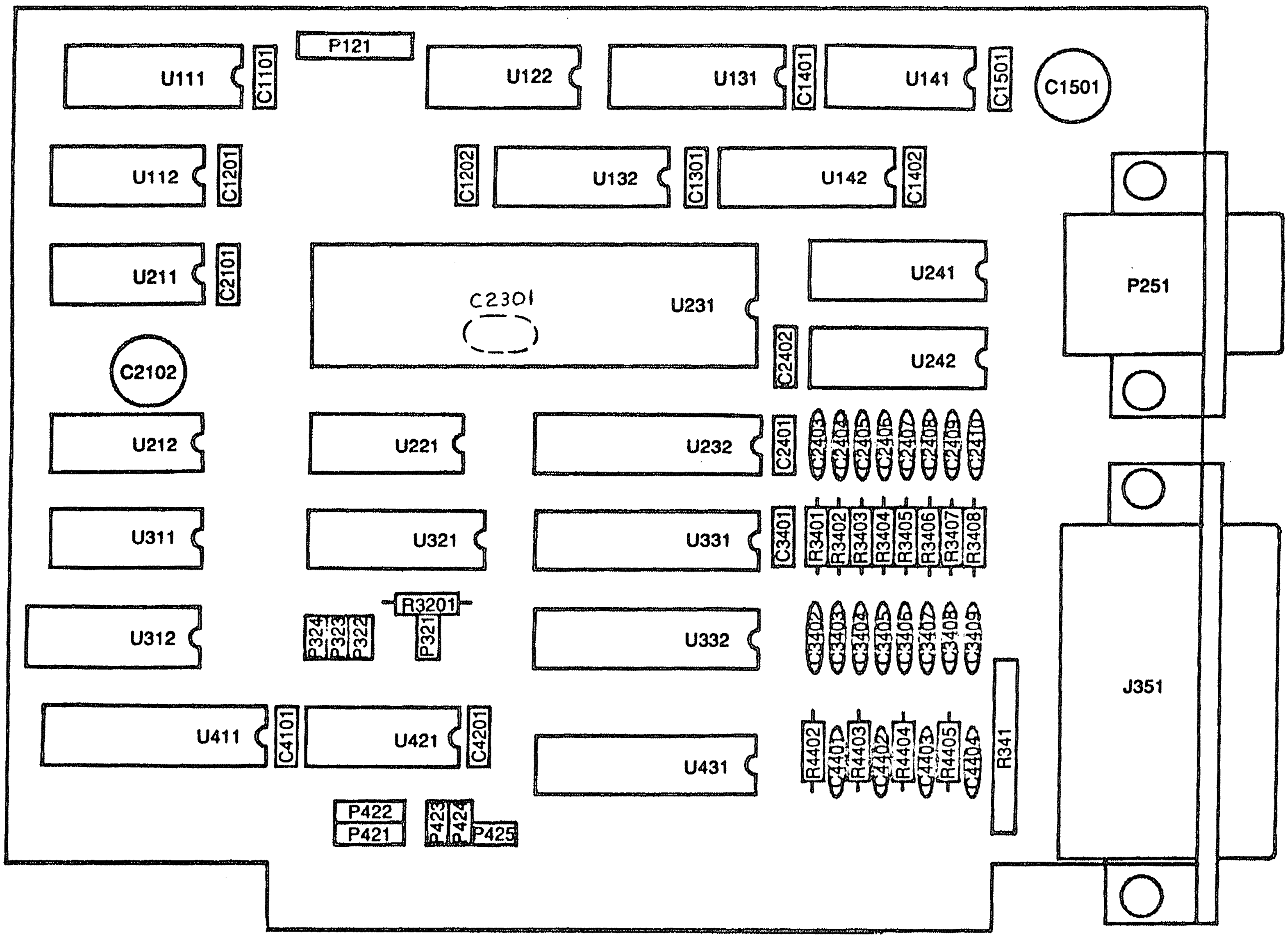


DATE 5-20-92

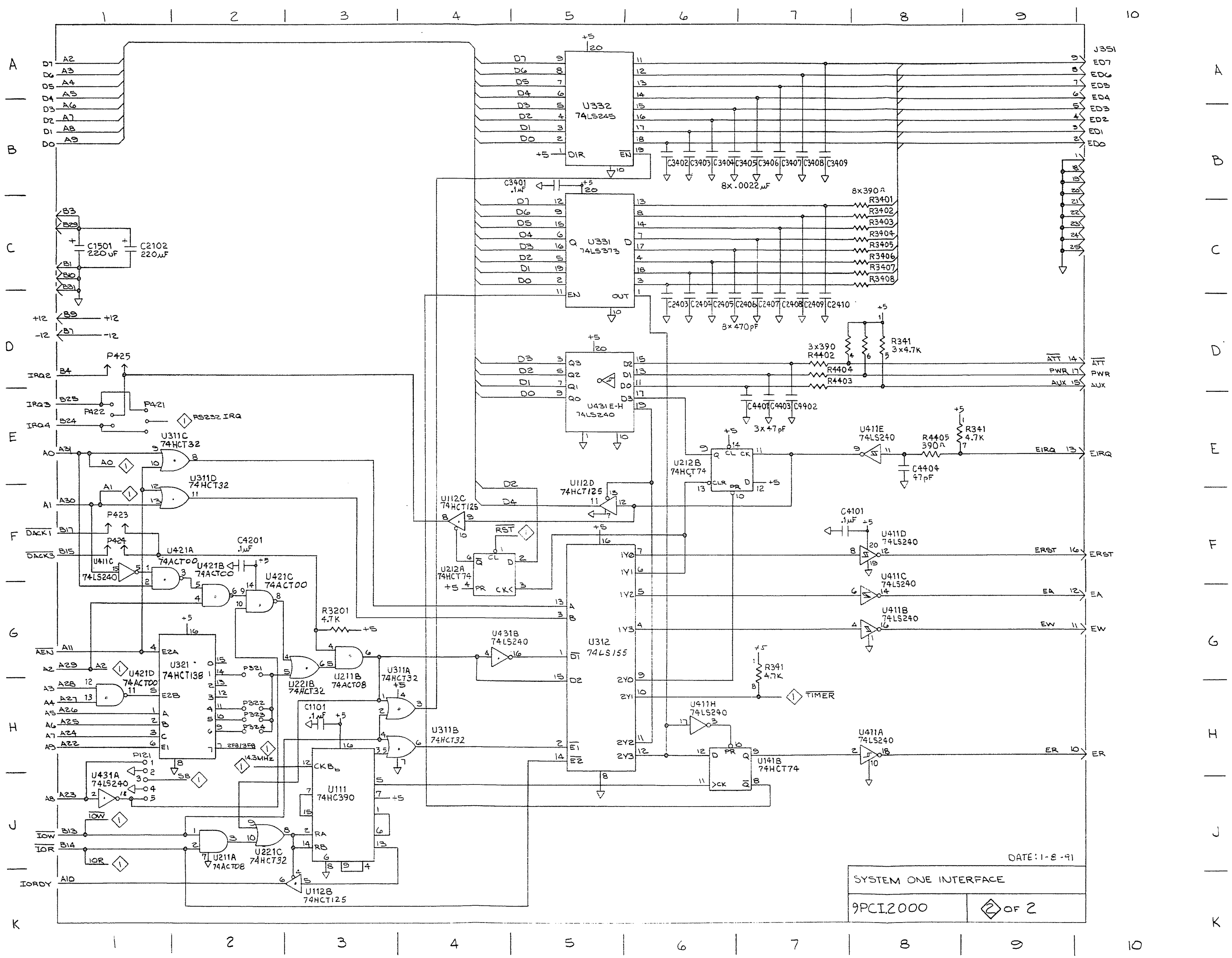
LAST ECO #91-031

RS232 COMMUNICATIONS

9PCI.2000 | 1 OF 2



COMPUTER INTERFACE 9PCI.2000 (6200.PCI2.5)

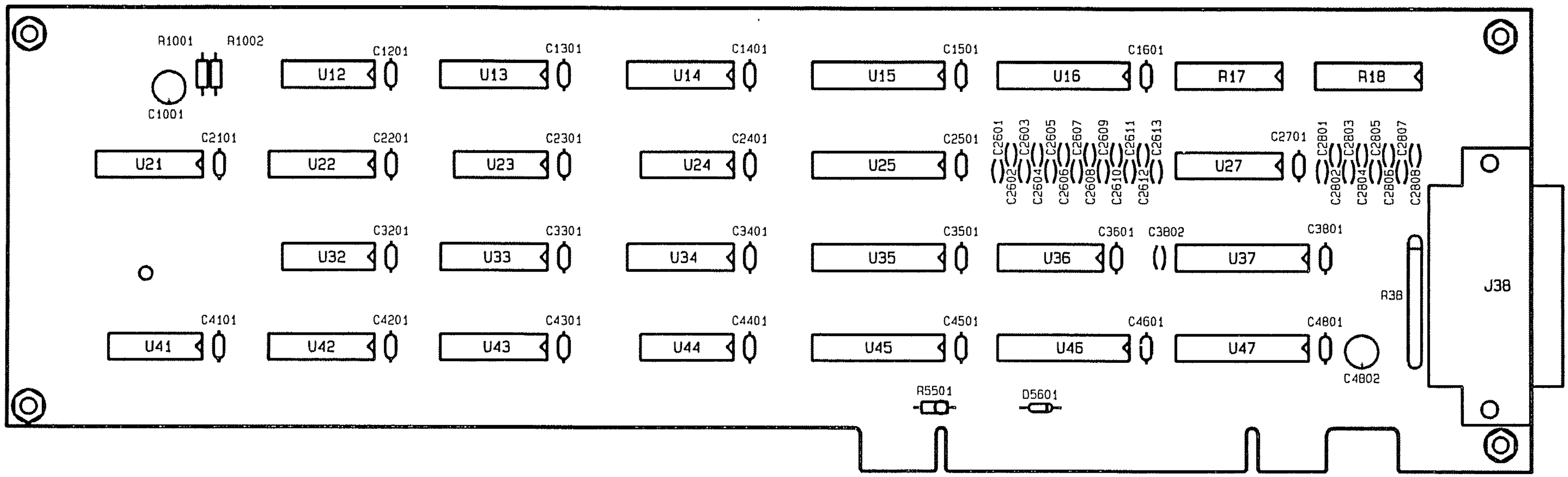

DATE: 1-8-91
SYSTEM ONE INTERFACE
9PCI.2000
2 OF 2
U332 74LS245
U331 74LS373
U431E-H 74LS240
U312 74LS155
U321 74HCT138
U111 74HC390
J351

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	2H3	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	1E2	2172.0104	CAP CERAM 100V 20%	.1uF
C1202	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C1301	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C1401	1G3	2172.0104	CAP CERAM 100V 20%	.1uF
C1402	1C3	2172.0104	CAP CERAM 100V 20%	.1uF
C1501	2C1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1502	1E3	2172.0104	CAP CERAM 100V 20%	.1uF
C2101	2C1	2172.0104	CAP CERAM 100V 20%	.1uF
C2102	1D6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2301	1E4	2172.0100	CAP CERAM 100V 20%	10pF
C2401	1B5	2172.0104	CAP CERAM 100V 20%	.1uF
C2402	2C6	2172.0104	CAP CERAM 100V 20%	.1uF
C2403	2C6	2172.0470	CAP CERAM 100V 20%	47pF
C2404	2C6	2172.0470	CAP CERAM 100V 20%	47pF
C2405	2C7	2172.0470	CAP CERAM 100V 20%	47pF
C2406	2C7	2172.0470	CAP CERAM 100V 20%	47pF
C2407	2C7	2172.0470	CAP CERAM 100V 20%	47pF
C2408	2C7	2172.0470	CAP CERAM 100V 20%	47pF
C2409	2C7	2172.0470	CAP CERAM 100V 20%	47pF
C2410	2C7	2172.0470	CAP CERAM 100V 20%	47pF
C3401	1B5	2172.0104	CAP CERAM 100V 20%	.1uF
C3402	2B6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3403	2B6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3404	2B7	2172.0222	CAP CERAM 100V 20%	.0022uF
C3405	2B7	2172.0222	CAP CERAM 100V 20%	.0022uF
C3406	2B7	2172.0222	CAP CERAM 100V 20%	.0022uF
C3407	2B7	2172.0222	CAP CERAM 100V 20%	.0022uF
C3408	2B7	2172.0222	CAP CERAM 100V 20%	.0022uF
C3409	2B7	2172.0222	CAP CERAM 100V 20%	.0022uF
C4101	2F7	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	2F3	2172.0104	CAP CERAM 100V 20%	.1uF
C4401	2D7	2172.0470	CAP CERAM 100V 20%	47pF
C4402	2D7	2172.0470	CAP CERAM 100V 20%	47pF
C4403	2D7	2172.0470	CAP CERAM 100V 20%	47pF
C4404	2E8	2172.0470	CAP CERAM 100V 20%	47pF
J351	2A10,2B10,2C10,2D10,2E10	4225.0025	JACK D-SUB PC 90'	25 PIN
P121	1H1	4221.0036	PLUG PC .1 X.43	36 PIN
P251	1B1,1C1,1D1	4225.0109	PLUG D-SUB PC 90'	9 PIN
P321	1G2	4221.0036	PLUG PC .1 X.43	36 PIN
P322	1H2	4221.0036	PLUG PC .1 X.43	36 PIN
P323	1H2	4221.0036	PLUG PC .1 X.43	36 PIN
P324	1H2	4221.0036	PLUG PC .1 X.43	36 PIN
P421	2E2	4221.0036	PLUG PC .1 X.43	36 PIN
P422	2E1	4221.0036	PLUG PC .1 X.43	36 PIN
P423	2F1	4221.0036	PLUG PC .1 X.43	36 PIN
P424	2F1	4221.0036	PLUG PC .1 X.43	36 PIN
P425	2E1	4221.0036	PLUG PC .1 X.43	36 PIN
R3201	2G3	1214.0472	RES 1/4W C FLM 5%	4.7K

REPLACEABLE ELECTRICAL PARTS LIST: 9PC1.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R3401	2C7	1214.0391	RES 1/4W C FLM 5%	390
R3402	2C7	1214.0391	RES 1/4W C FLM 5%	390
R3403	2C7	1214.0391	RES 1/4W C FLM 5%	390
R3404	2C7	1214.0391	RES 1/4W C FLM 5%	390
R3405	2C7	1214.0391	RES 1/4W C FLM 5%	390
R3406	2C7	1214.0391	RES 1/4W C FLM 5%	390
R3407	2C7	1214.0391	RES 1/4W C FLM 5%	390
R3408	2C7	1214.0391	RES 1/4W C FLM 5%	390
R341	2E8,2G6,2D8	1984.9102	RES NET SIP 5% B	9 X 1K
R4402	2D7	1214.0391	RES 1/4W C FLM 5%	390
R4403	2D7	1214.0391	RES 1/4W C FLM 5%	390
R4404	2D7	1214.0391	RES 1/4W C FLM 5%	390
R4405	2E8	1214.0391	RES 1/4W C FLM 5%	390
U111	2H3	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U112	1E3,2K3,2F4,2E5	3324.0125	BUFFER 4X TRI-ST	74HCT125
U122	1H3,1H5,1H6	3323.0086	GATE 4-IN EXCL OR	74HC86
U131	1G2	3323.4040	COUNTER 12-STAGE	74HC4040
U132	1B3,1B4,1C3,1C4	3333.5406	RS232 DRIVER/RCVR	MC145406
U141	1H4,2H7	3324.0074	FLIP-FLOP 2X D	74HCT74
U142	1C3,1C2,1D2	3333.5406	RS232 DRIVER/RCVR	MC145406
U211	1E3,1F6,2G3,2J2	3326.0008	GATE 4 X 2-IN AND	74ACT08
U212	2E6	3324.0074	FLIP-FLOP 2X D	74HCT74
U221	1G3,1J2,2J2	3324.0032	GATE 4 X 2-IN OR	74HCT32
U231	1C5	3332.16450	ASYNCH COMM ELEMENT	NS16450
U232	1D6	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U241	1G7	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U242	1H4,1H5	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U311	1E1,1F1,2H4	3324.0032	GATE 4 X 2-IN OR	74HCT32
U312	2G5	3324.0155	DECODER 2 X 2-LN/4-LN	74HCT155
U321	2G2	3324.0138	DECODER 3LINE/8LINE	74HCT138
U331	2C5	3313.0373	LATCH 8X D TRI-ST	74LS373
U332	2A5	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U411	2F1,2H6,2H8,2G8,2F8,2E8	3313.0240	BUFFER 8X INV TRI-ST	74LS240
U421	2F1,2G2,2H1	3326.0000	GATE 4 X 2-IN NAND	74ACT00
U431	1F5,1G3,2J1,2D5	3313.0240	BUFFER 8X INV TRI-ST	74LS240

PCI-3 **COMPUTER INTERFACE**



COMPUTER INTERFACE 9PCI.3000 (6200.PCI3.3)

PCI-3, COMPUTER INTERFACE CARD

NOTE: There are three possible versions of the Audio Precision digital interface board. The **PCI-1** *is a half-size IBM-PC card and contains a* female *9-pin connector for the original version Microsoft mouse. The* **PCI-2** *is very similar in appearance to the PCI-1 however it contains a 9-pin* male *connector for an auxiliary serial interface. The PCI-1 is obsolete but may still be found in use with older systems. The* **PCI-3** *is designed for the IBM PS/2 family of computers and differs significantly in size and shape.*

Introduction

The PCI-3 computer interface card is installed inside one of the expansion slots of the host computer and allows digital communications between the standard System One software and hardware package. The nature of the interface is unique to Audio Precision and is described in section 1.4.

Address Decoding <1>

The address decoding for the PCI card is performed by U33, U34 and U47. The 1-of-8 multiplexer U33 selects one of the four decoded outputs from U34. These go low for each of three different blocks of I/O space. Address selection bits ADR1 and ADR0 are used to select the appropriate decoded state for the desired address. The other four inputs of the multiplexer are tied high, allowing the card to be de-selected when CDEN into U33 is low.

Address comparator U47 checks the remaining bits for the correct pattern of high and low levels to uniquely determine the desired address. P0-P3 set the required number of high and low levels at the address inputs. When P0-P2 are low and P3 is high U47 will require inputs A1-A8 (of the chip) to be low and A9-A12 (of the chip) to be high. These are connected to the appropriate address lines of the computer to decode the desired address. If P3 is low and P0-P2 are high U47 will require inputs A1-A7 (of the chip) to be low and A8-A12 (of the chip) to be high. Input A8 of U47 thus changes from active low to active high based on the level of ADR0.

The available System One base address locations are therefore $238, $298, $2B8 and $2D8. The output of U47 goes low when the appropriate address is received. Its output drives the active low chip select of U22 and U36 (through U46). This also enables one section of tri-state buffer U44, driving /CDSFDBK low, and indicating the presence of the PCI card at that address.

The original PCI-1 version of this card included a mouse interface and used one of the mouse ports as a timer. To retain compatibility with old software the timer port on the PCI-3 card is mapped into both old and new addresses. This is accomplished by not decoding A2 in the System One interface circuitry. This causes the four I/O addresses used by the interface to alias into the four addresses directly above those normally used.

System One Interface <1>

The System One interface is a byte-wide multiplexed address and data bus. There are 256 addresses available in the System One from the eight bits of address information. The main functions of the interface are mapped into two I/O spaces of the host computer interface bus. One output byte from the host is used as the address byte. The other is used as the data byte. Two additional I/O spaces are used to read the status lines on the interface bus and to force a reset of the System One hardware if desired.

The bus operates by stretching all read and write operations of the host microprocessor bus to approximately 2 usec. The timing circuitry, consisting of U22A, U13 and U12A generates the memory-not-ready pulses required to slow the microprocessor bus.

All data going out of the host is buffered by octal bus transceiver U15. The output lines are filtered by C2801 through C2808 to reduce the rise time of the signals and reduce radiated EMI. Data being read from the System One is buffered by octal bus transceiver U25. Filter networks R18/C2606 through R18/C2613 reduce noise picked up in the lines.

Wait State Generator <1>

The System One select signal from U46 enables decoding of the PS2 mode control lines (S0-S2) by U36. This decoder creates read and write strobes. Unlike PC/AT systems, the PS/2 interface has no read or write lines. U22 decodes the start of I/O read or write operations without needing to wait for the address latch signal. The read and write lines are combined in AND gate U32 and used to preset flip-flop U12. This clears the reset from counter U13 which begins a wait state pulse on CD_CHRDY.

The wait state counter is clocked from the 14 MHz master clock of the host computer, allowing repeatable timing of the wait states. The outputs start from the low state, forcing a low on the IOCHRDY line through U31B. This tells the host microprocessor to wait while the write or read cycle is completed. The counter output starts low and goes high after a 2 usec delay. OR gate U31 combines the wait state counter output with the output of the enabling flip-flop. When a wait state is begun the flip-flop output goes low and the counter output is already low. This passes through the OR gate and asserts a low on the ready line. At the end of the approximately 2 usec interval the output of U13 will go high, releasing the processor from the wait state.

An earlier output from the counter (at 1.5 usec) is used to force the write strobe line (EW) on the System One interface to finish its pulse before the host processor is released from the wait state. This guarantees that the data to be latched into the System One is still valid when the strobe pulse reaches the end of the cable.

Bus Drive <1>

The decoder U27 decodes the write and read operations to drive the appropriate strobe lines on the System One interface. The selected output of U27 will go low to implement the appropriate function. The 2Y3 output is enabled for data writes, driving the interface EW line high via inverter U37D. The 2Y2 output goes low for address writes driving the interface EA line high through U37C. The 2Y1 output is used to control the enabling of interrupts from the System One via U12B and to clear pending interrupts in U23B. The 2Y0 output drives the System One interface reset line through U37B, forcing the ERST line high and resetting all hardware modules.

The 1Y3 output of U27 goes low for data reads from the System One. This enables the output of buffer U25 onto the bus of the host computer. The 1Y3 output also drives the ER line on the System One interface through U37E, causing devices in the System One to place their data on the interface. The 1Y3 output of U27 drives the buffer U16. The five buffer outputs drive the host bus allowing read of the three System One status lines, reading the state of the interrupt line and reading the state of flip-flop U23B which latches any occurrence of an interrupt.

PCI-3 Interface Addressing

The addresses occupied by the Audio Precision Interface are selected by the power on setup (POS) feature of the IBM PS2 computer. A disk containing the adapter description file is packaged with the PCI-3 card from Audio Precision. This file is copied onto the boot disk of the computer. The default address selected by the automatic setup is 238-23B hex. This will automatically be changed if the computer senses an address conflict during the automatic setup. It will then pick one of the alternate addresses to avoid this conflict. The choices may be viewed by the change configuration utility supplied with the computer.

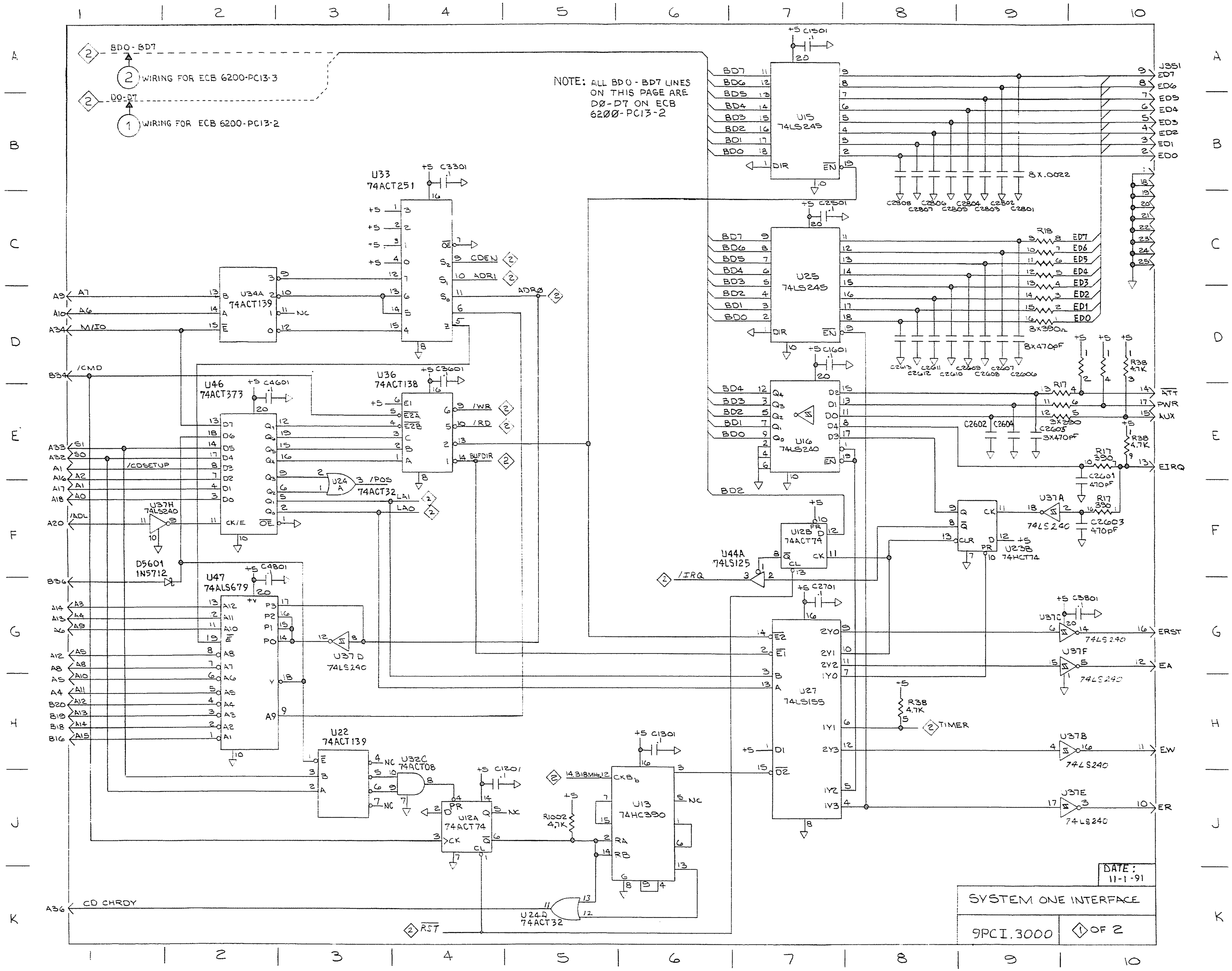
Power On Setup (POS) <2>

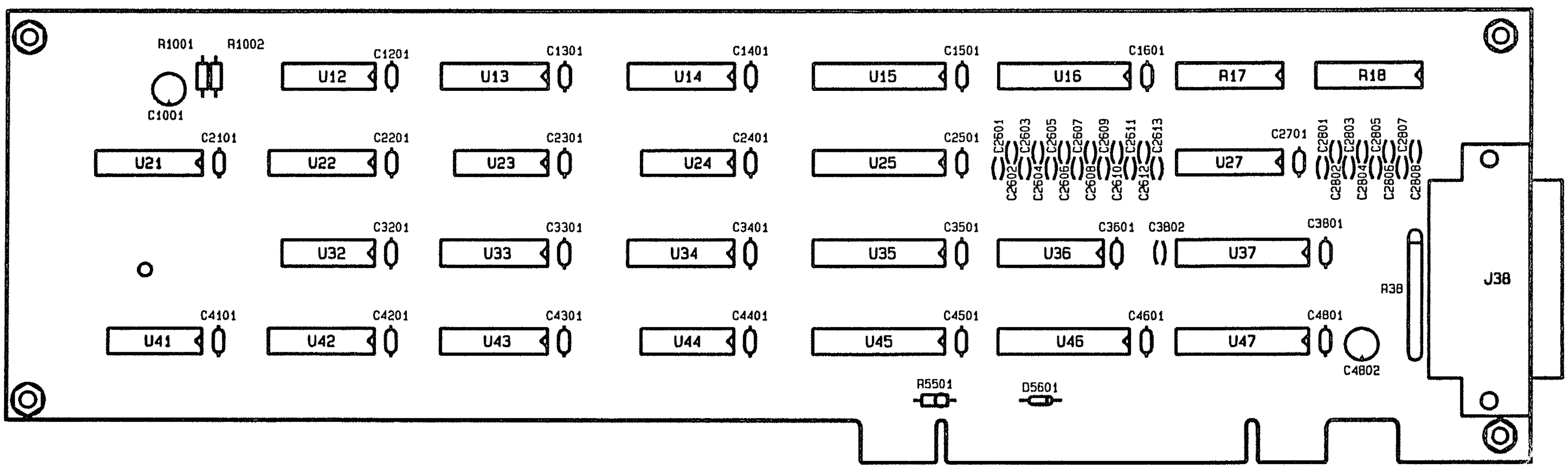
U14, U22 and U25 perform the power on setup required for the IBM PS2 system. On power up the card is de-selected and is set up by the computers BIOS routines. Latch U14 stores the bits required to select the address (ADR1, ADR0), the IRQ channel (IRQS1, IRQS0) and to enable the card (CDEN). The power on reset signal from the computer clears the latch, driving all of its outputs low. Using a dedicated enable signal to each card (/CDSETUP) the computer can program this latch to the appropriate pattern for the desired address and IRQ. To determine what the card in any given expansion slot is, the computer can read a 16-bit word from the card. A unique number is assigned to each manufacturer of expansion cards. This number is the same as that in the name of the adapter description file. For the Audio Precision System One interface card the number is 6064 hex. U22 decodes the two read addresses for the upper and lower bytes of the word. This word is supplied by U35 which reads as either 60 hex or 64 hex, depending on the address from which it is read.

Short Interval Timer <2>

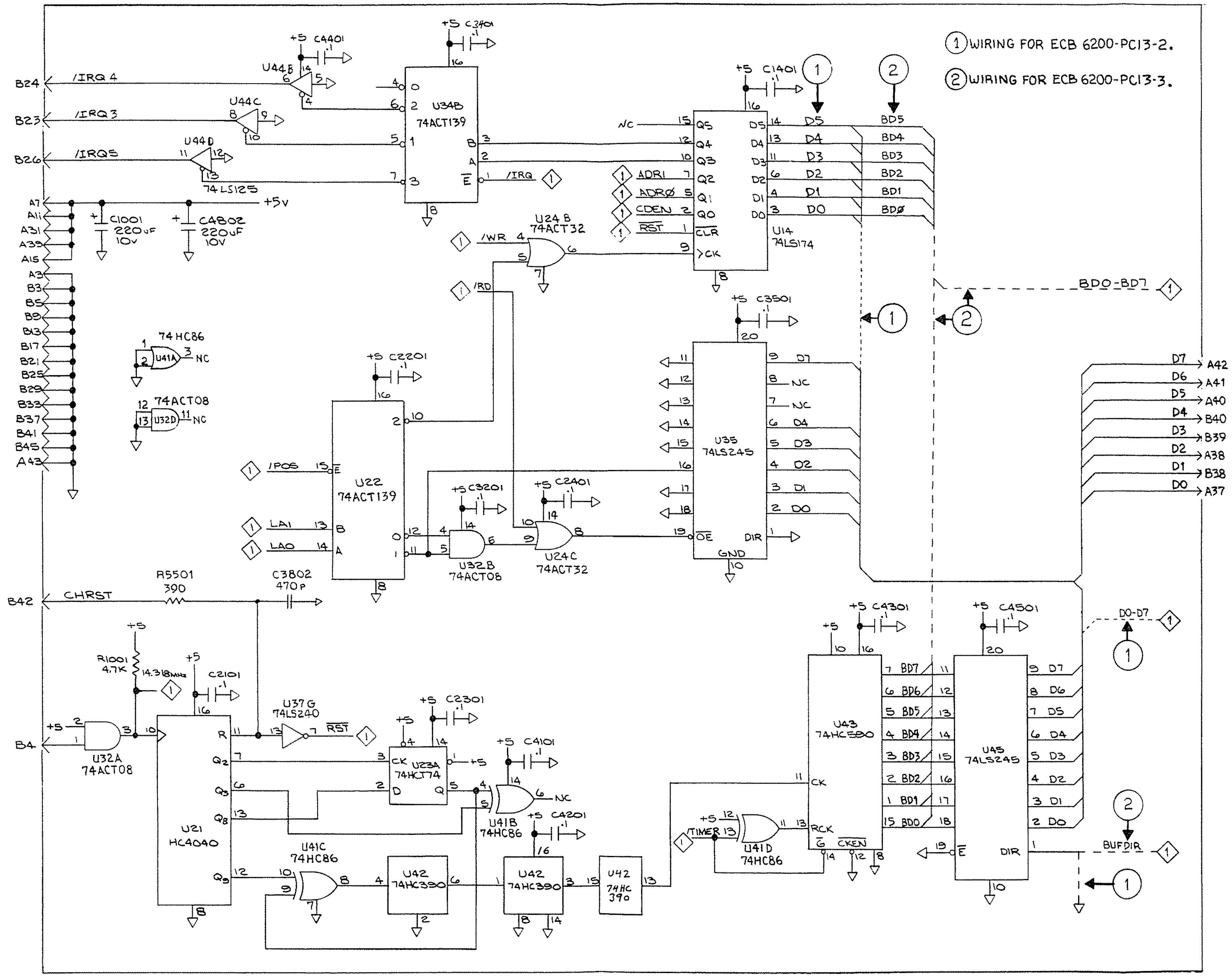
The clock for the short interval timer is provided by dividing the 14.318 MHz host computer clock with U21. A 55.93 kHz signal is combined with a 27.96 kHz signal in U41B to obtain a 83.9 kHz clock for the short interval timer. This is divided by 20 in U42, resulting in a 4.195 kHz clock.

The 241 usec clock pulses are counted by 8-bit counter U43, giving a resolution of approximately 241 usec. This is read by the processor when the 1Y1 output of U27 pulses low. The low going edge of the read strobe is inverted by U41D to create a high going edge to latch the count into U43's output buffers. Since the output current capability of U43 is insufficient to drive the bus, octal buffer U45 is used.


NOTE: ALL BD0 - BD7 LINES ON THIS PAGE ARE D0-D7 ON ECB 6200-PC13-2
BD0-BD7
WIRING FOR ECB 6200-PC13-3
D0-D7
WIRING FOR ECB 6200-PC13-2
U15 74LS245
U25 74LS245
U16 74LS240
U33 74ACT251
U34A 74ACT139
U46 74ACT373
U36 74ACT138
U24 A 74ACT32
U37H 74LS240
D5601 1N5712
U47 74ALS679
U37D 74LS240
U22 74ACT139
U32C 74ACT08
U12A 74ACT74
U13 74HC390
U24D 74ACT32
U12B 74ACT74
U44A 74LS125
U27 74LS155
U37A 74LS240
U23B 74HCT74
U37C 74LS240
U37F 74LS240
U37B 74LS240
U37E 74LS240
J351
8X.0022
8X470pF
3X390Ω
3X470PF
R18 8X390Ω
R17 390
R38 4.7K
R1002 4.7K
C2601 470pF
C2603 470pF
14.318MHz
CDEN
ADR1
ADR0
/WR
/RD
BUFDIR
/POS
LA1
LA0
/CMD
/CDSETUP
/ADL
/IRQ
TIMER
CD CHRDY
RST
ATT
PWR
AUX
EIRQ
ERST
EA
EW
ER
ED0 ED1 ED2 ED3 ED4 ED5 ED6 ED7
DATE: 11-1-91
SYSTEM ONE INTERFACE
9PCI.3000
1 OF 2



COMPUTER INTERFACE 9PCI.3000 (6200.PCI3.3)



POS AND TIMER

DATE: 11-1-91

9PCI.3000

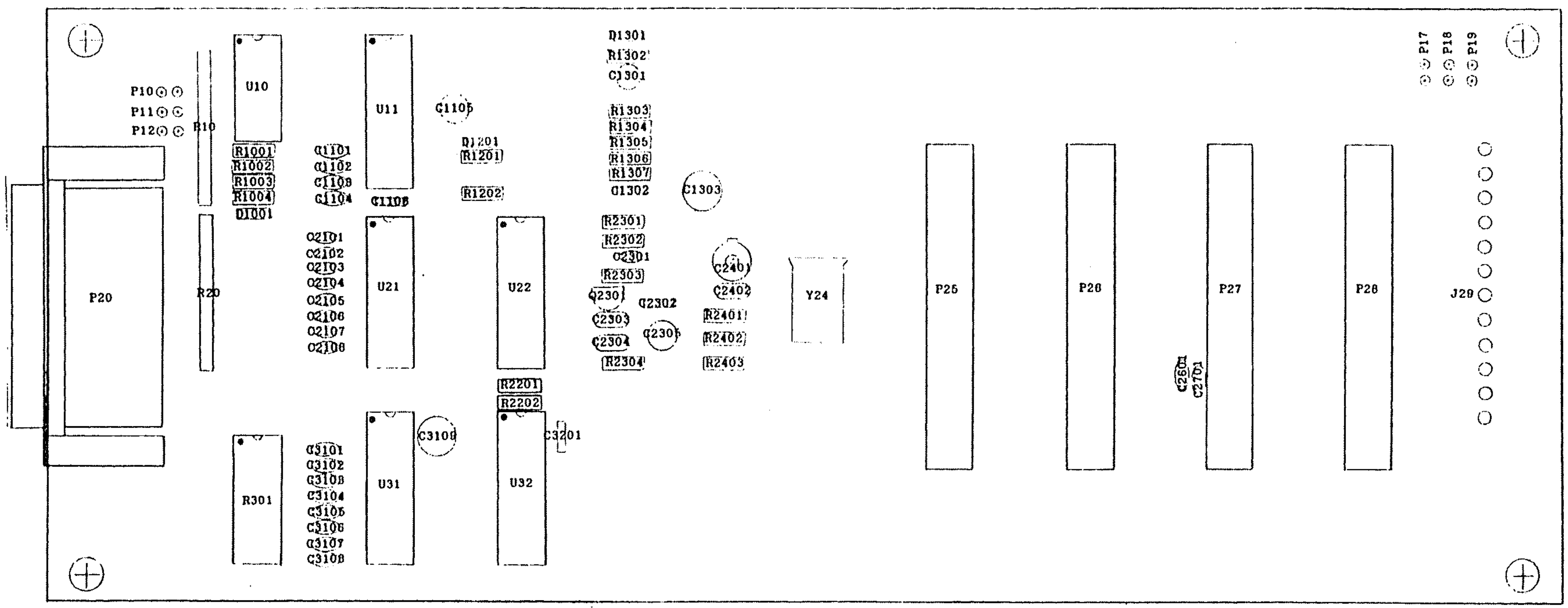
2 OF 2

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1001	2C2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1201	1J4	2172.0104	CAP CERAM 100V 20%	.1uF
C1301	1H6	2172.0104	CAP CERAM 100V 20%	.1uF
C1401	2B7	2172.0104	CAP CERAM 100V 20%	.1uF
C1501	1B7	2172.0104	CAP CERAM 100V 20%	.1uF
C1601	1D7	2172.0104	CAP CERAM 100V 20%	.1uF
C2101	2G3	2172.0104	CAP CERAM 100V 20%	.1uF
C2201	2D4	2172.0104	CAP CERAM 100V 20%	.1uF
C2301	2G4	2172.0104	CAP CERAM 100V 20%	.1uF
C2401	2E5	2172.0104	CAP CERAM 100V 20%	.1uF
C2501	1C7	2172.0104	CAP CERAM 100V 20%	.1uF
C2601	1F10	2172.0471	CAP CERAM 100V 20%	470pF
C2602	1F10	2172.0471	CAP CERAM 100V 20%	470pF
C2603	1E9	2172.0471	CAP CERAM 100V 20%	470pF
C2604	1E9	2172.0471	CAP CERAM 100V 20%	470pF
C2605	1E9	2172.0471	CAP CERAM 100V 20%	470pF
C2606	1D9	2172.0471	CAP CERAM 100V 20%	470pF
C2607	1D9	2172.0471	CAP CERAM 100V 20%	470pF
C2608	1D9	2172.0471	CAP CERAM 100V 20%	470pF
C2609	1D9	2172.0471	CAP CERAM 100V 20%	470pF
C2610	1D8	2172.0471	CAP CERAM 100V 20%	470pF
C2611	1D8	2172.0471	CAP CERAM 100V 20%	470pF
C2612	1D8	2172.0471	CAP CERAM 100V 20%	470pF
C2613	1D8	2172.0471	CAP CERAM 100V 20%	470pF
C2701	1G7	2172.0104	CAP CERAM 100V 20%	.1uF
C2801	1B9	2172.0222	CAP CERAM 100V 20%	.0022uF
C2802	1B9	2172.0222	CAP CERAM 100V 20%	.0022uF
C2803	1B9	2172.0222	CAP CERAM 100V 20%	.0022uF
C2804	1B9	2172.0222	CAP CERAM 100V 20%	.0022uF
C2805	1B8	2172.0222	CAP CERAM 100V 20%	.0022uF
C2806	1B8	2172.0222	CAP CERAM 100V 20%	.0022uF
C2807	1B8	2172.0222	CAP CERAM 100V 20%	.0022uF
C2808	1B8	2172.0222	CAP CERAM 100V 20%	.0022uF
C3101	1K5	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	2E5	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C3401	2B4	2172.0104	CAP CERAM 100V 20%	.1uF
C3501	2D6	2172.0104	CAP CERAM 100V 20%	.1uF
C3601	1D4	2172.0104	CAP CERAM 100V 20%	.1uF
C3801	1G10	2172.0104	CAP CERAM 100V 20%	.1uF
C3802	2F3	2172.0471	CAP CERAM 100V 20%	470pF
C4101	2G5	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	2H5	2172.0104	CAP CERAM 100V 20%	.1uF
C4301	2F7	2172.0104	CAP CERAM 100V 20%	.1uF
C4401	2B3	2172.0104	CAP CERAM 100V 20%	.1uF
C4501	2F8	2172.0104	CAP CERAM 100V 20%	.1uF
C4601	1E2	2172.0104	CAP CERAM 100V 20%	.1uF
C4801	1G2	2172.0104	CAP CERAM 100V 20%	.1uF
C4802	2C3	2911.0227	CAP AL-EL 10V +80/-20%	220uF
D5601	1G1	3120.0000	DIODE SIGNAL	5712

REPLACEABLE ELECTRICAL PARTS LIST: 9PCI.3000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
J38	1B10,1C10,1E10,1G10,1H10,1J10	4225.0025	JACK D-SUB PC 90'	25 PIN
R1001	2G2	1214.0472	RES 1/4W C FLM 5%	4.7K
R1002	1J5	1214.0472	RES 1/4W C FLM 5%	4.7K
R17	1E9,1F9	1994.8391	RES NET DIP 5%	8 X 390
R18	1C9,1D9	1994.8391	RES NET DIP 5%	8 X 390
R38	1D10,1E10,1H8	1984.9102	RES NET SIP 5% B	9 X 1K
R5501	2F2	1214.0391	RES 1/4W C FLM 5%	390
U12	1F7,1J4	3326.0074	FLIP-FLOP 2X D	74ACT74
U13	1J6	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U14	1C6	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U15	1B7	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U16	1E7	3313.0240	BUFFER 8X INV TRI-ST	74LS240
U21	2H3	3323.4040	COUNTER 12-STAGE	74HC4040
U22	2E4,1J3	3326.0139	DECODER 2 X 2-LN/4-LN	74ACT139
U23	1F9,2H4	3324.0074	FLIP-FLOP 2X D	74HCT74
U24	2C5,2F5,1F7,1F3	3326.0032	GATE 4 X 2-IN OR	74ACT32
U25	1D7	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U27	1H7	3313.0155	DECODER 2 X 2-LN/4-LN	74LS155
U32	1J4,2G2,2F4	3326.0008	GATE 4 X 2-IN AND	74ACT08
U33	1C4	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U34	2B4,1D2	3326.0139	DECODER 2 X 2-LN/4-LN	74ACT139
U35	2E6	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U36	1E4	3326.0138	DECODER 3-LN/8-LN	74ACT138
U37	1F1,1F9,1G9,1H9,1J9,1G3,2G3	3313.0240	BUFFER 8X INV TRI-ST	74LS240
U41	2H3,2H5,2H6	3323.0086	GATE 4-IN EXCL OR	74HC86
U42	2H4,2H5	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U43	2H7	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U44	2C3,2B3,1F7	3313.0125	BUFFER 4X TRI-STATE	74LS125
U45	2H8	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U46	1E2	3326.0373	LATCH 8X D TRI-ST	74ACT373
U47	1H2	3315.0679	ADDRESS COMP 12-BIT	74ALS679

MFI-1 MAINFRAME INTERFACE



SYSTEM ONE MAINFRAME INTERFACE (9MFI.1000)

MFI-1, MAINFRAME INTERFACE ASSEMBLY

NOTE: There are five possible versions of the mainframe interface assembly depending upon the digital interface option (see Section 1.3), system configuration, and age. The MFI version can be determined from the identification decal attached to the rear panel digital connector. The code number will have the format "MFIx-yyyyy-zz" where "x" is the MFI version.

Introduction

The MFI-1 mainframe interface board provides four basic functions: master clock generation, digital interface decoding and buffering, power on reset generation, and signal distribution to the four module compartments in the System One mainframe. The digital interface information from the computer enters the board through connector P20 at the left edge of the schematic. The four connectors for the cables to the modules are P25, P26, P27 and P28. Power supply connections enter through J29.

Master Clock Circuit

The master clock for System One functions is provided by a 20 MHz oscillator. Q2301 operates as a Colpitts oscillator with Y24 as the frequency reference element. C2401 pads the impedance of the crystal to allow some adjustment of frequency. R2403, C2302 and C2305 filter the +15V supply to eliminate noise coupling into the oscillator. C2301, R2301 and R2302 shift the signal from the oscillator to TTL logic levels for buffering by U22A-U22D. Each of the four buffers drives a separate module to eliminate interaction between the cards and maximize signal amplitude. Resistors R1304 through R1307 reduce ringing on the clock lines and provide a controlled rise time.

Reset Circuit

Buffers U22F, U22G and U10D, inverters U11B and U11D and associated components form the reset circuit. Reset can be initiated by either the host computer or by power cycling of the System One mainframe. Tri-state buffer U10D is used as an OR gate to combine these two reset signals. Its output goes high to reset, forcing the output of U11B low and providing the /RESET signal to each of the modules.

The reset signal from the host computer enters the System One via pin 16 of P20, the digital interface connector. A high level on this line forces reset. Because of the pull up resistor R10, disconnecting the cable will also cause a reset. This line is filtered to remove noise and buffered by the Schmitt trigger buffer U22G.

The power on reset is generated by sensing the presence of voltage on pin 11 from the power supply. This voltage is stored on C1301. This is attenuated by D1301 and R1302 to make it compatible with the logic levels. The threshold is set to +2 V by comparator action in U22F. R1202 serves to increase the hysteresis of the buffer. A high going pulse representing power present will be delayed by R1201 and C1105 until the supplies have had a chance to stabilize. A low going pulse representing power failure will bypass the delay network by the action of D1201. This reset pulse is buffered and inverted by U11D so that a high level forces reset.

Digital Interface

The data and address information from the host computer share the same 8-bit bus to the System One. The interface also contains three strobe lines to indicate which type of information is carried on the bus at the time. These are described in the accompanying interface description.

Data entering the System One mainframe is filtered by the eight RC networks R301A/C3101 through R301B/C3108 and buffered by the octal bus transceiver U31. This data drives the address latch and the four module connectors P25, P26, P27 and P28. The address information is latched by U32 and drives an additional eight lines on the module connectors. Data leaving the System One is buffered by the octal buffer U21. Capacitors C2101 through C2108 limit the rise time of the data edges to reduce EMI generation. Resistor network R20 pulls the bus lines high when they are tri-stated to prevent oscillations of the bus buffers when the lines assume voltages near TTL threshold.

When the host computer places address information on the bus it strobes the EA line high. This is filtered by R1001 and C1101 to remove noise and buffered by inverter U11E. This produces a low going pulse which is used to strobe the address latch U32. This address information is held until the next address write operation by the host.

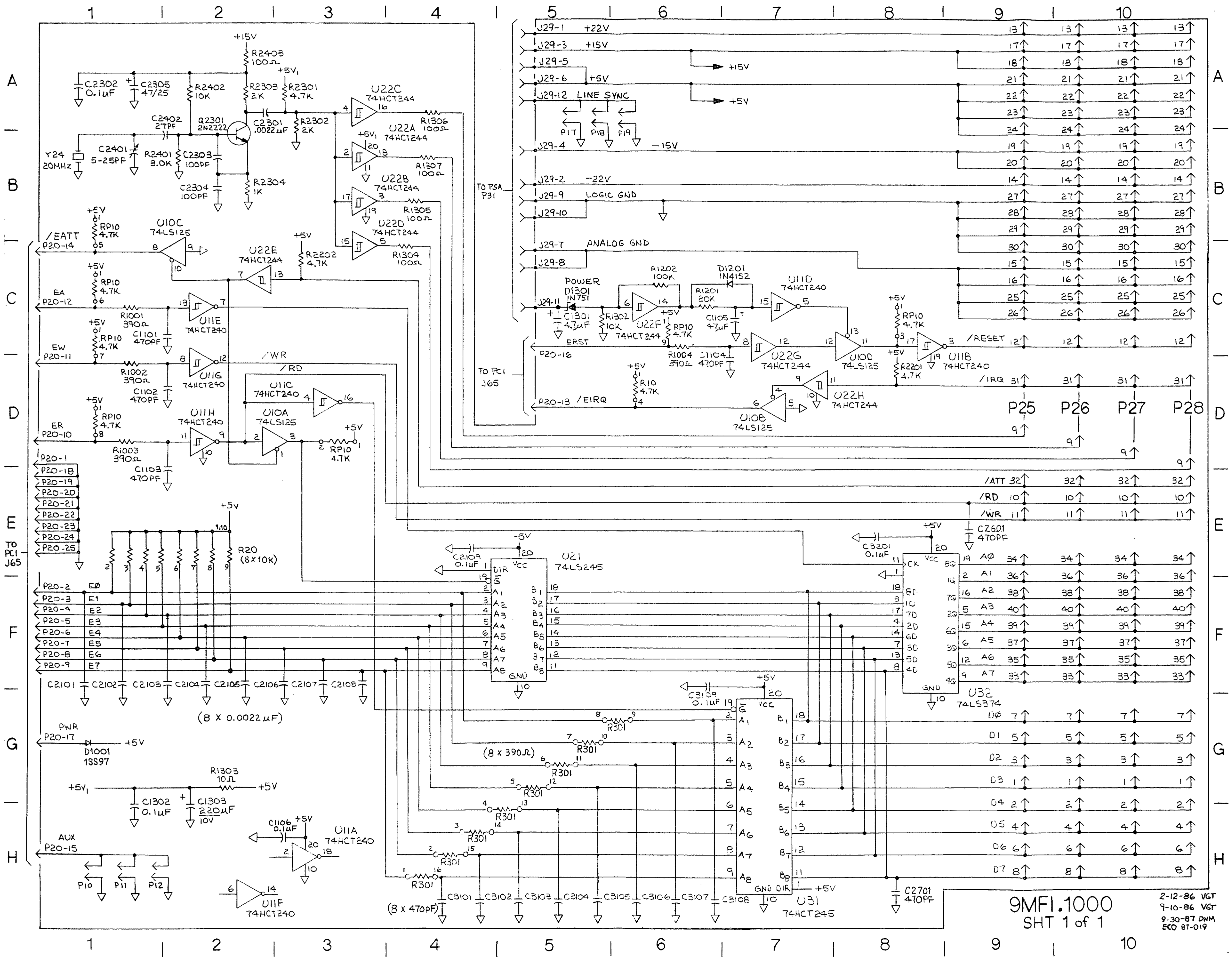
When data is written from the host computer to the System One the EW line is pulled high. This is filtered by R1002 and C1102 and buffered by inverter U11G. The output of this gate is the /WR line which strobes low to write data into any module in the System One.

When data is read from the System One into the host computer the ER line is pulled high. This is filtered by R1003 and C1103 and buffered by inverter U11H. The output of this gate is the /RD line which strobes low to read data from any module in the System One. The /ER line is also buffered by tri-state buffer U10A and used to enable the output bus buffer U21 and inverted by U11C and used to disable the input buffer U31. This prevents any bus contention by multiple buffers being active at one time. The purpose of the tri-state gate U10A is explained below.

When any module in the box senses its address on the address bus it pulls the /ATT line low. This serves two purposes. This information is passed to the host computer on the /EATT line so that the host may determine if a particular module is present. It is also used to disable the read buffer U21 if there are no modules in the enclosure at that address. This allows multiple System One enclosures to be present on the external bus at the same time if only one module at each address is used. The /ATT line is buffered by U22E and drives the tri-state buffers U10A and U10C. The output of U10C is open collector, so that its signal is combined in a logic OR function with those from other enclosures. U10A disables the operation of U21 so that bus contention does not occur between multiple System One enclosures during read operations.

Miscellaneous Bus Operations

Diode D1001 is used to pull the PWR line low if the mainframe loses power. This may be sensed by the host to determine the failure. The /IRQ line is a wired OR signal from the modules which is used to signal the host that service is necessary. It is buffered by U22H and drives the external bus via tri-state buffer U10B. U10B allows this signal to be wire ORed among System One enclosures. The /AUX signal is available on the external bus to allow for communications tasks between future modules and the host. It is not currently used.



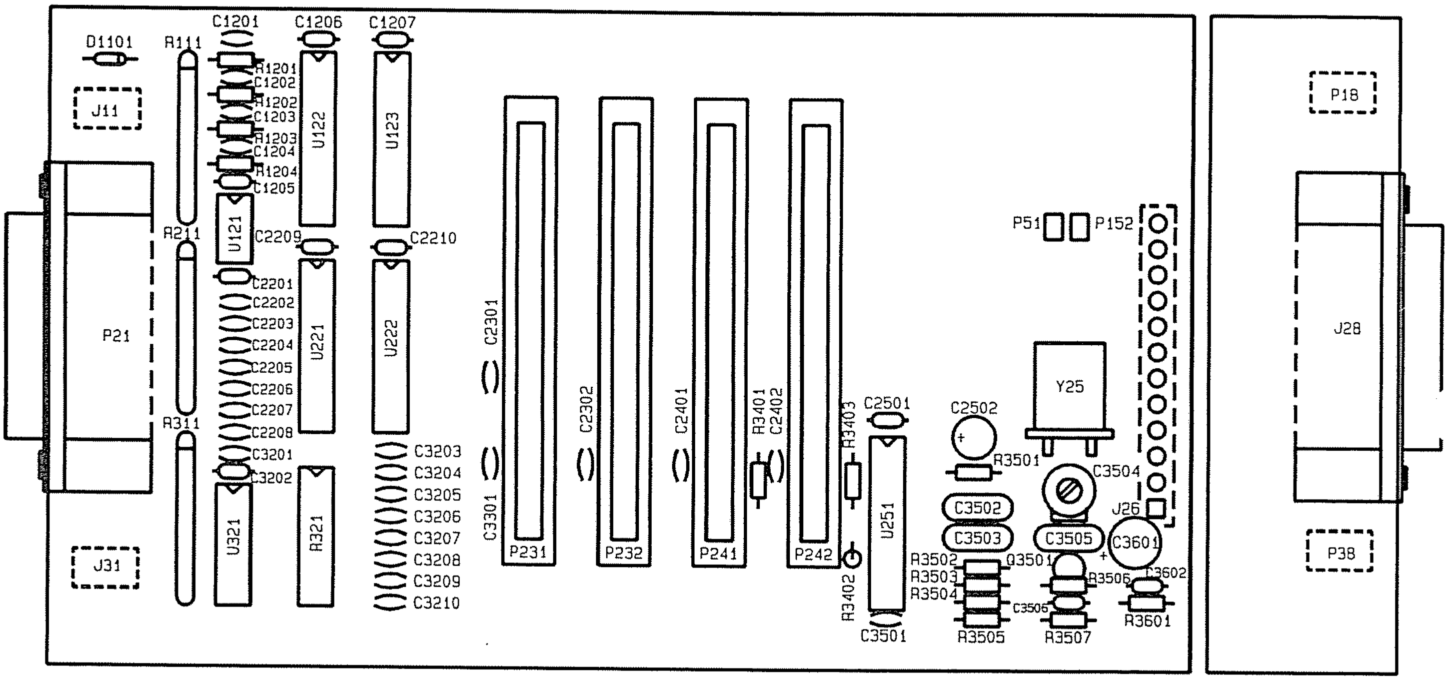
J29-1 +22V
J29-3 +15V
J29-5
J29-6 +5V
J29-12 LINE SYNC
J29-4 −15V
J29-2 −22V
J29-9 LOGIC GND
J29-10
J29-7 ANALOG GND
J29-8
J29-11
TO PSA P31
TO PCI J65
P25
P26
P27
P28
/EATT P20-14
EA P20-12
EW P20-11
ER P20-10
/RESET
/IRQ
/ATT
/RD
/WR
P20-16
P20-13 /EIRQ
ERST
POWER D1301 1N751
Y24 20MHz
Q2301 2N2222
U21 74LS245
U31 74HCT245
U32 74LS374
R20 (8 X 10K)
(8 X 0.0022µF)
(8 x 390Ω)
(8 x 470PF)
PWR P20-17
D1001 1SS97
AUX P20-15
R1303 10Ω
C1303 220µF 10V
9MFI.1000
SHT 1 of 1
2-12-86 VGT
9-10-86 VGT
9-30-87 DWM
ECO 87-019

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	1C2	2172.0471	CAP CERAM 100V 20%	470pF
C1102	1D2	2172.0471	CAP CERAM 100V 20%	470pF
C1103	1E2	2172.0471	CAP CERAM 100V 20%	470pF
C1104	1D7	2172.0471	CAP CERAM 100V 20%	470pF
C1105	1C7	2932.0476	CAP AL-EL 25V 20%	47uF
C1106	1H3	2172.0104	CAP CERAM 100V 20%	.1uF
C1301	1C5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C1302	1H1	2172.0104	CAP CERAM 100V 20%	.1uF
C1303	1H2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2101	1F1	2172.0222	CAP CERAM 100V 20%	.0022uF
C2102	1F1	2172.0222	CAP CERAM 100V 20%	.0022uF
C2103	1F2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2104	1F2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2105	1F2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2106	1F3	2172.0222	CAP CERAM 100V 20%	.0022uF
C2107	1F3	2172.0222	CAP CERAM 100V 20%	.0022uF
C2108	1F3	2172.0222	CAP CERAM 100V 20%	.0022uF
C2301	1A2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2302	1A1	2172.0104	CAP CERAM 100V 20%	.1uF
C2303	1B2	2296.0101	CAP MICA 500V 1%	100pF
C2304	1B2	2296.0101	CAP MICA 500V 1%	100pF
C2305	1A1	2932.0476	CAP AL-EL 25V 20%	47uF
C2401	1B1	4450.0250	VAR CAP PC	5-25pF
C2402	1B2	2294.0270	CAP MICA 500V 5%	27pF
C2601	1E9	2172.0471	CAP CERAM 100V 20%	470pF
C2701	1H8	2172.0471	CAP CERAM 100V 20%	470pF
C3101	1H4	2172.0471	CAP CERAM 100V 20%	470pF
C3102	1H4	2172.0471	CAP CERAM 100V 20%	470pF
C3103	1H5	2172.0471	CAP CERAM 100V 20%	470pF
C3104	1H5	2172.0471	CAP CERAM 100V 20%	470pF
C3105	1H5	2172.0471	CAP CERAM 100V 20%	470pF
C3106	1H6	2172.0471	CAP CERAM 100V 20%	470pF
C3107	1H6	2172.0471	CAP CERAM 100V 20%	470pF
C3108	1H6	2172.0471	CAP CERAM 100V 20%	470pF
C3109	1F6	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	1E8	2172.0104	CAP CERAM 100V 20%	.1uF
D1001	1G1	3120.0000	DIODE SCHOTTKY	1SS97
D1201	1C7	3110.4152	DIODE SIGNAL	4152
D1301	1C5	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
J29	1A5	4152.0012	CABLE ASSY .156	18Ga 12 COND
P10	1H1	4221.0036	PLUG PC .1 X.43	36 PIN
P11	1H1	4221.0036	PLUG PC .1 X.43	36 PIN
P12	1H1	4221.0036	PLUG PC .1 X.43	36 PIN
P17	1A5	4221.0036	PLUG PC .1 X.43	36 PIN
P18	1A5	4221.0036	PLUG PC .1 X.43	36 PIN
P19	1A6	4221.0036	PLUG PC .1 X.43	36 PIN
P20	1C1	4225.0125	PLUG D-SUB PC 90'	25 PIN
P25	1A9	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P26	1A10	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN

Replaceable Electrical Parts List: 9MFI.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
P27	1A10	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P28	1A10	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
Q2301	1B2	3211.2222	XSTR NPN TO92	PN2222A
R10	1B1,1C1,1C6,1C8,1D1,1D3,1D6	1984.9472	RES NET SIP 5%	9 X 4.7K
R1001	1C1	1214.0391	RES 1/4W C FLM 5%	390
R1002	1D1	1214.0391	RES 1/4W C FLM 5%	390
R1003	1D1	1214.0391	RES 1/4W C FLM 5%	390
R1004	1C6	1214.0391	RES 1/4W C FLM 5%	390
R1201	1C6	1214.0203	RES 1/4W C FLM 5%	20K
R1202	1C6	1214.0104	RES 1/4W/C/FLM 5%	100K
R1302	1C5	1214.0103	RES 1/4W C FLM 5%	10K
R1303	1G2	1214.0100	RES 1/4W C FLM 5%	10
R1304	1C4	1214.0101	RES 1/4W C FLM 5%	100
R1305	1B4	1214.0101	RES 1/4W C FLM 5%	100
R1306	1A4	1214.0101	RES 1/4W C FLM 5%	100
R1307	1B4	1214.0101	RES 1/4W C FLM 5%	100
R20		1984.9103	RES NET SIP 5%	9 X 10K
R2201	1D8	1214.0472	RES 1/4W C FLM 5%	4.7K
R2202	1C3	1214.0472	RES 1/4W C FLM 5%	4.7K
R2301	1A3	1214.0472	RES 1/4W C FLM 5%	4.7K
R2302	1A3	1214.0202	RES 1/4W C FLM 5%	2.0K
R2303	1A2	1214.0202	RES 1/4W C FLM 5%	2.0K
R2304	1B2	1214.0102	RES 1/4W C FLM 5%	1K
R2401	1B2	1214.0302	RES 1/4W C FLM 5%	3.0K
R2402	1A2	1214.0103	RES 1/4W C FLM 5%	10K
R2403	1A2	1214.0101	RES 1/4W C FLM 5%	100
R301	1G5,1G6,1H4,1H5	1994.8391	RES NET DIP 5%	8 X 390
U10	1C2,1D2,1D7	3313.0125	BUFFER 4X TRI-STATE	74LS125
U11	1C2,1C7,1D2,1D3,1H2,1H3	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U21	1F5	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U22	1A3,1B3,1C2,1C3,1C7,1D7	3324.0244	BUFFER 8X TRI-STATE	74HCT244
U31	1G7	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U32	1F8	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
Y24	1B1	3900.0020	CRYSTAL	20MHz

MFI-2 MAINFRAME INTERFACE



MAINFRAME INTERFACE 9MFI.2000 (6200.MFI2.4)

MFI-2, MAINFRAME INTERFACE ASSEMBLY

NOTE: There are five possible versions of the mainframe interface assembly depending upon the digital interface option (see Section 1.3), system configuration, and age. The MFI version can be determined from the identification decal attached to the rear panel digital connector. The code number will have the format "MFIx-yyyyy-zz" where "x" is the MFI version.

Introduction

The MFI-2 mainframe interface board provides four basic functions: master clock generation, digital interface decoding and buffering, power on reset generation, and signal distribution to the four module compartments in the System One mainframe. The digital interface information from the computer enters the board through connectors P21 and J28 at the left edge of the schematic. The four connectors for the cables to the modules are P231, P232, P241 and P242. Power supply connections enter through J26.

Master Clock Circuit

The master clock for System One functions is provided by a 20 MHz oscillator. Q3501 operates as a Colpitts oscillator with Y25 as the frequency reference element. C3504 pads the impedance of the crystal to allow some adjustment of frequency. R3504, C2502 and C5306 filter the +15V supply to eliminate noise coupling into the oscillator. C3501, R3507 and R3505 shift the signal from the oscillator to TTL logic levels for buffering by U251E. Each of the four buffers drives a separate module to eliminate interaction between the cards and maximize signal amplitude. Resistors R3401 and R3403 reduce ringing on the clock lines and provide a controlled rise time.

Reset Circuit

Resetting of the measurement hardware can be initiated by either the host computer or by power cycling of the System One mainframe. The power-on reset is generated by the +5V supply sensor IC U121. The sensor monitors when the supply voltage falls below 4.75 Volts and asserts the internal reset signal. The host computer reset signal enters the System One via pin 16 of P21, the digital interface connector. A high level on this line forces reset. Because of the pull up resistor R111, disconnecting the cable will also cause a reset. This line is filtered to remove noise and buffered by inverter U122A. Its output goes low, providing a /RESET signal to the supply sensor.

Digital Interface

The data and address information from the host computer share the same 8-bit bus to the System One. The interface also contains three strobe lines to indicate which type of information is carried on the bus at the time. These are described in the accompanying interface description.

Data entering the System One mainframe is filtered by the eight RC networks R321A/C3203 through R321H/C3210 and buffered by the octal bus transceiver U222. This data drives the address latch and the four module connectors P231, P232, P241 and P242. The address information is latched by U123 and drives an additional eight lines on the module connectors. Data leaving the System One is buffered by the octal buffer U221. Capacitors C2202 through C2208 and C3201 limit the rise time of the data edges to reduce EMI generation. Resistor network R211 pulls the bus lines high when they are tri-stated to prevent oscillations of the bus buffers when the lines assume voltages near TTL threshold.

When the host computer places address information on the bus it strobes the EA line high. This is filtered by R1204 and C1204 to remove noise and buffered by inverter U122D. This produces a low going pulse which is used to strobe the address latch U123. This address information is held until the next address write operation by the host.

When data is written from the host computer to the System One, the EW line is pulled high. This is filtered by R1203 and C1203 and buffered by inverter U122C. The output of this gate is the /WR line which strobes low to write data into any module in the System One.

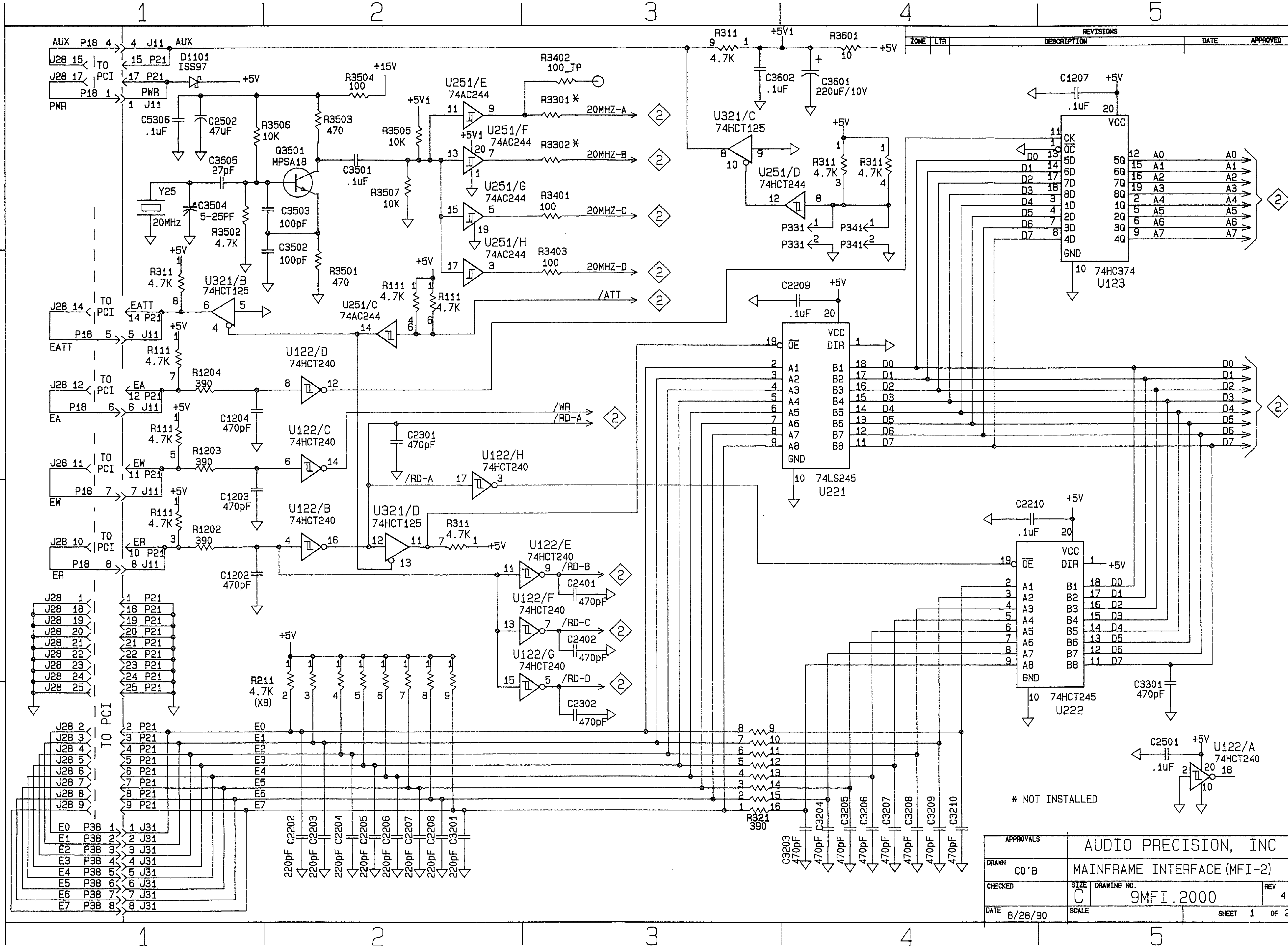
When data is read from the System One into the host computer the ER line is pulled high. This is filtered by

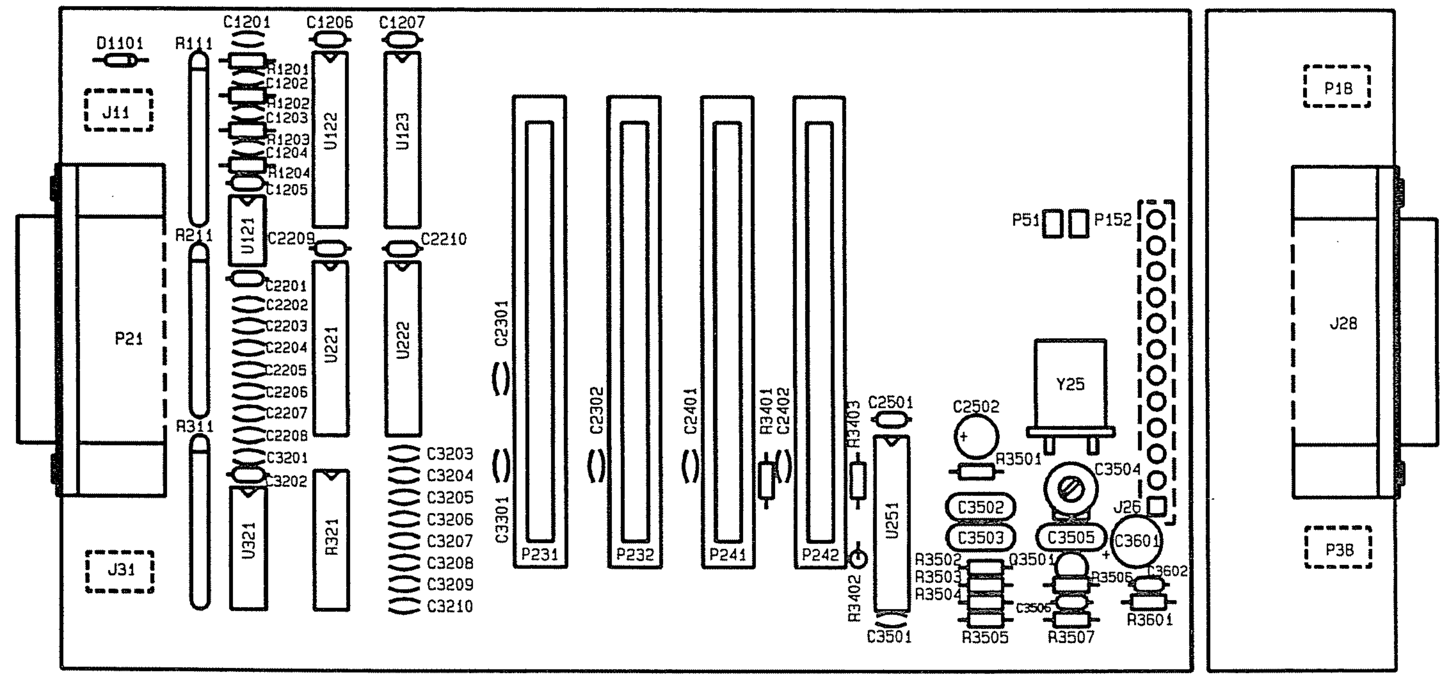
R1202 and C1202 and buffered by inverter U122B, U122E, U122F, and U122G. The outputs of these gates are the lines which strobe low to read data from any module in the System One. The /RD-A line is also buffered by tri-state buffer U321D and used to enable the output bus buffer U221 and inverted by U122H and used to disable the input buffer U222. This prevents any bus contention by multiple buffers being active at one time. The purpose of the tri-state gate U321D is explained below.

When any module in the box senses its address on the address bus it pulls the /ATT line low. This serves two purposes. This information is passed to the host computer on the /EATT line so that the host may determine if a particular module is present. It is also used to disable the read buffer U221 if there are no modules in the enclosure at that address. This allows multiple System One enclosures to be present on the external bus at the same time if only one module at each address is used. The /ATT line is buffered by U251C and drives the tri-state buffers U321B and U321D. The output of U321B is open collector, so that its signal is combined in a logic OR function with those from other enclosures. U321D disables the operation of U221 so that bus contention does not occur between multiple System One enclosures during read operations.

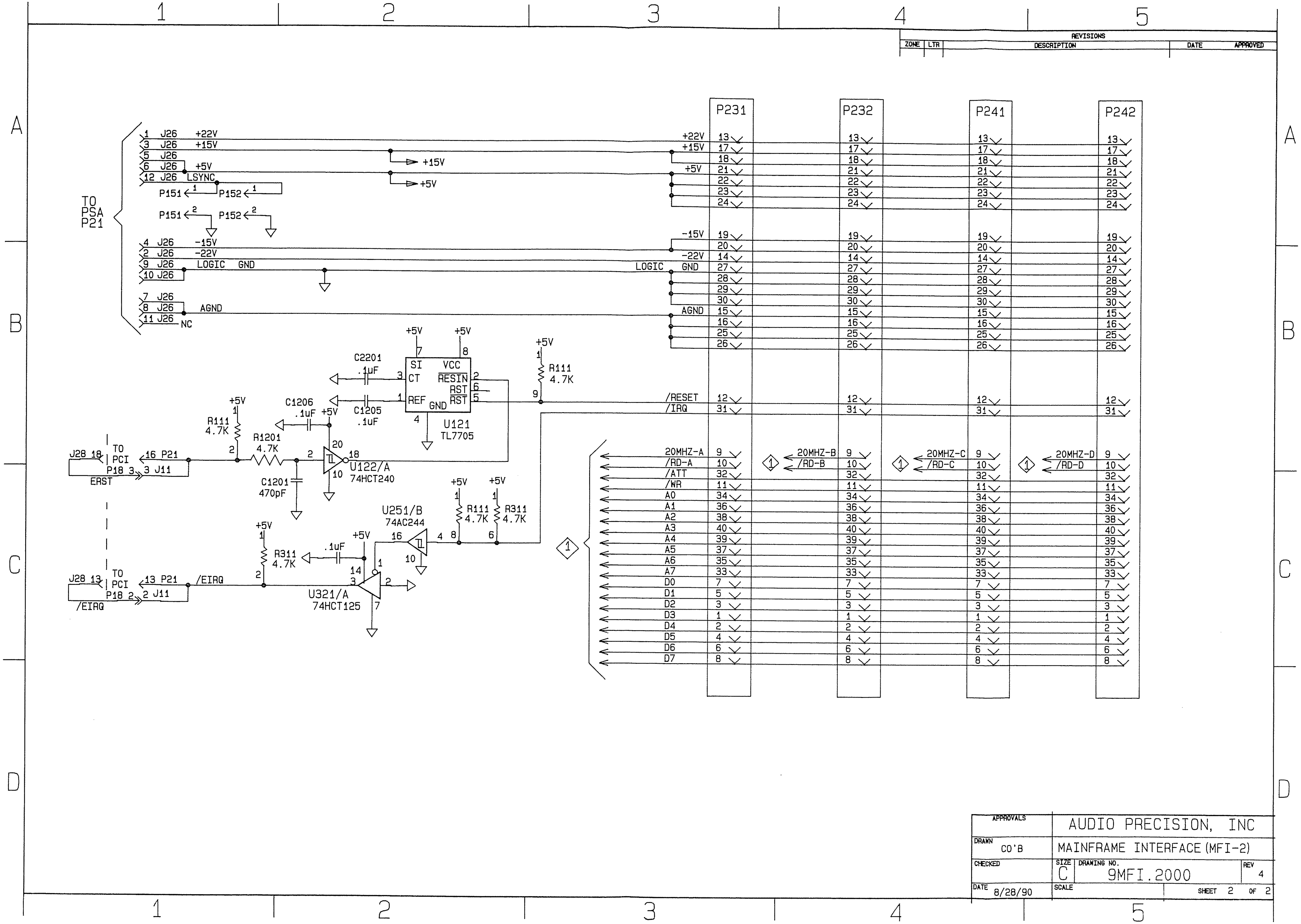
Miscellaneous Bus Operations

Diode D1101 is used to pull the PWR line low if the mainframe loses power. This may be sensed by the host to determine the failure. The /IRQ line is a wired OR signal from the modules which is used to signal the host that service is necessary. It is buffered by U251B and drives the external bus via tri-state buffer U321A. U321A allows this signal to be wire ORed among System One enclosures. The /AUX signal is available on the external bus to allow for communications tasks between the DSP module and the host.


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
* NOT INSTALLED
AUX
PWR
EATT
EA
EW
ER
TO PCI
20MHZ-A
20MHZ-B
20MHZ-C
20MHZ-D
/ATT
/WR
/RD-A
/RD-B
/RD-C
/RD-D
74AC244
74HCT125
74HCT240
74HCT244
74HC374
U123
74LS245
U221
74HCT245
U222
APPROVALS
AUDIO PRECISION, INC
DRAWN CO'B
MAINFRAME INTERFACE (MFI-2)
CHECKED
SIZE C
DRAWING NO. 9MFI.2000
REV 4
DATE 8/28/90
SCALE
SHEET 1 OF 2



MAINFRAME INTERFACE 9MFI.2000 (6200.MFI2.4)

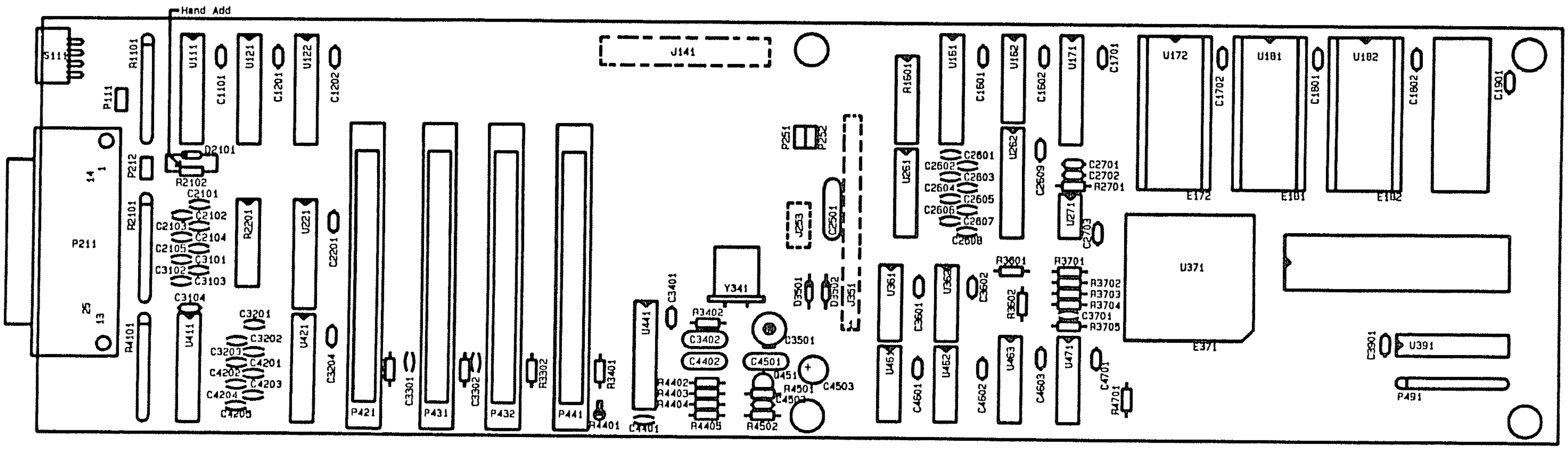

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
TO PSA P21
1 J26 +22V
3 J26 +15V
5 J26
6 J26 +5V
12 J26 LSYNC
P151 1
P152 1
P151 2
P152 2
+15V
+5V
4 J26 -15V
2 J26 -22V
9 J26 LOGIC GND
10 J26
7 J26
8 J26 AGND
11 J26 NC
P231
P232
P241
P242
+22V
+15V
+5V
-15V
-22V
LOGIC GND
AGND
/RESET
/IRQ
+5V
C2201 .1uF
C1205 .1uF
SI VCC CT RESIN REF RST RST GND
U121 TL7705
R111 4.7K
C1206 .1uF
R1201 4.7K
U122/A 74HCT240
C1201 470pF
J28 18
TO PCI P18 3
16 P21
3 J11
ERST
U251/B 74AC244
R311 4.7K
U321/A 74HCT125
J28 13
TO PCI P18 2
13 P21
2 J11
/EIRQ
20MHZ-A
/RD-A
/ATT
/WR
A0
A1
A2
A3
A4
A5
A6
A7
D0
D1
D2
D3
D4
D5
D6
D7
20MHZ-B
/RD-B
20MHZ-C
/RD-C
20MHZ-D
/RD-D
APPROVALS
DRAWN CO'B
CHECKED
DATE 8/28/90
AUDIO PRECISION, INC
MAINFRAME INTERFACE (MFI-2)
SIZE C
DRAWING NO. 9MFI.2000
REV 4
SCALE
SHEET 2 OF 2

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1201	2C2	2172.0471	CAP CERAM 100V 20%	470pF
C1202	1C1	2172.0471	CAP CERAM 100V 20%	470pF
C1203	1C1	2172.0471	CAP CERAM 100V 20%	470pF
C1204	1B1	2172.0471	CAP CERAM 100V 20%	470pF
C1205	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C1206	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C1207	1B5	2172.0104	CAP CERAM 100V 20%	.1uF
C2201	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C2202	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2203	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2204	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2205	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2206	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2207	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2208	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2209	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C2210	1C5	2172.0104	CAP CERAM 100V 20%	.1uF
C2301	1B2	2172.0471	CAP CERAM 100V 20%	470pF
C2302	1D3	2172.0471	CAP CERAM 100V 20%	470pF
C2401	1C3	2172.0471	CAP CERAM 100V 20%	470pF
C2402	1C3	2172.0471	CAP CERAM 100V 20%	470pF
C2501	1D5	2172.0104	CAP CERAM 100V 20%	.1uF
C2502	1A1	2932.0476	CAP AL-EL 25V 20%	47uF
C3201	1D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C3202	2C2	2172.0104	CAP CERAM 100V 20%	.1uF
C3203	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3204	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3205	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3206	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3207	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3208	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3209	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3210	1D4	2172.0471	CAP CERAM 100V 20%	470pF
C3301	1C5	2172.0471	CAP CERAM 100V 20%	470pF
C3501	1A2	2172.0104	CAP CERAM 100V 20%	.1uF
C3502	1A2	2296.0101	CAP MICA 500V 1%	100pF
C3503	1A2	2296.0101	CAP MICA 500V 1%	100pF
C3504	1A1	4450.0250	VAR CAP PC	5-25pF
C3505	1A1	2294.0270	CAP MICA 500V 5%	27pF
C3506	1A1	2172.0104	CAP CERAM 100V 20%	.1uF
C3601	1A4	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C3602	1A3	2172.0104	CAP CERAM 100V 20%	.1uF
D1101	1A1	3120.0000	DIODE SCHOTTKY	1SS97
J11	1A1,1B1,1C1,2C1	4221.1008	JACK PC 2 X .1	8 PIN
J26	2A1,2B1	4152.0012	CABLE ASSY .156 18Ga	12 COND
J28	1B1,1C1,1D1,2C1	4225.0025	JACK D-SUB PC 90'	25 PIN
J31	1D1	4221.1008	JACK PC 2 X .1	8 PIN
P151	2A1	4221.0036	PLUG PC .1 X.43	36 PIN
P152	2A1	4221.0036	PLUG PC .1 X.43	36 PIN

REPLACEABLE ELECTRICAL PARTS LIST: 9MFI.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
P18	1A-C1,2C1	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P21	1A-D1,2C1	4225.0125	PLUG D-SUB PC 90'	25 PIN
P231	2A3	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P232	2A4	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P241	2A4	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P242	2A5	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P331	1A4	4221.0036	PLUG PC .1 X.43	36 PIN
P341	1A4	4221.0036	PLUG PC .1 X.43	36 PIN
P38	1D1	4221.0072	PLUG PC 2X.1 X.43	72 PIN
Q3501	1A2	3211.0018	XSTR NPN TO92	MPSA18
R111	1B1,1B2,1C1,2B1,2B2,2C2	1984.9472	RES NET SIP 5% B	9 X 4.7K
R1201	2C1	1214.0391	RES 1/4W C FLM 5%	390
R1202	1C1	1214.0391	RES 1/4W C FLM 5%	390
R1203	1B1	1214.0391	RES 1/4W C FLM 5%	390
R1204	1B1	1214.0391	RES 1/4W C FLM 5%	390
R211	1C2	1984.9472	RES NET SIP 5% B	9 X 4.7K
R311	1A3,1A4,1B1,1C2,2C1,2C2	1984.9472	RES NET SIP 5% B	9 X 4.7K
R321	1D4	1994.8391	RES NET DIP 5%	8 X 390
R3301	1A3	1214.0101	RES 1/4W C FLM 5%	100
R3302	1A3	1214.0101	RES 1/4W C FLM 5%	100
R3401	1A3	1214.0101	RES 1/4W C FLM 5%	100
R3402	1A3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R3403	1B3	1214.0101	RES 1/4W C FLM 5%	100
R3501	1A2	1214.0471	RES 1/4W C FLM 5%	470
R3502	1A1	1214.0472	RES 1/4W C FLM 5%	4.7K
R3503	1A2	1214.0471	RES 1/4W C FLM 5%	470
R3504	1A2	1214.0101	RES 1/4W C FLM 5%	100
R3505	1A2	1214.0103	RES 1/4W C FLM 5%	10K
R3506	1A1	1214.0103	RES 1/4W C FLM 5%	10K
R3507	1A2	1214.0103	RES 1/4W C FLM 5%	10K
R3601	1A4	1214.0100	RES 1/4W C FLM 5%	10
U121	2B2	3450.7705	SUPPLY VOLT SENSOR	5V
U122	1B2,1C2,1C3,1D3,1D5,2B2	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U123	1B5	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U221	1B4	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U222	1C5	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U251	1A2,1A4,1B2,2C2	3325.0244	BUFFER 8X TRI-ST	74AC244
U321	1A4,1B1,1C2,2C2	3313.0125	BUFFER 4X TRI-STATE	74LS125
Y25	1A1	3900.0020	CRYSTAL	20MHz

MFI-3 MAINFRAME INTERFACE



MAINFRAME INTERFACE 9MFI.3000 (6400.MFI3.3)

MFI-3, MAINFRAME INTERFACE ASSEMBLY

NOTE: There are five possible versions of the mainframe interface assembly depending upon the digital interface option (see Section 1.3), system configuration, and age. The MFI version can be determined from the identification decal attached to the rear panel digital connector. The code number will have the format "MFIx-yyyyy-zz" where "x" is the MFI version.

Introduction

The MFI-3 mainframe interface board provides five basic functions: master clock generation, GPIB or RS232 interface decoding and buffering, Audio Precision Interface Bus decoding and buffering, power on reset generation, and signal distribution to the four module compartments in the System One mainframe. The selection of RS232 or GPIB interface is made via a daughter board, the OMI-3, which contains the appropriate interface logic.

The MFI-3 contains all of the circuitry for communicating with a personal computer over the "APIB" (Audio Precision Interface Bus) interface bus. In addition it contains a reduced capability version of a personal computer and personal computer interface (PCI) card. The internal computer can then translate commands received over the GPIB or RS232 interface and convert them to APIB commands. These commands will drive the hardware internal to the System and will also appear on the rear panel APIB connector. Other System One equipment such as a DCX-127 or SWR-122 modules may be connected to the APIB connector. The internal computer will then control these as well. If desired, the internal computer may be disabled via the rocker switches on the rear panel and the System One will operate over the APIB from an external personal computer. The processor reads these on power up to see if it should be in APIB or internal computer mode. If APIB mode is selected, the internal computer shuts down and will not restart without power cycling.

System One Interface

The System One interface is a byte-wide multiplexed address and data bus. There are 256 addresses available in the System One from the eight bits of address information. The main functions of the interface are mapped into two I/O spaces of the host computer interface bus. One output byte from the host is used as the address byte. The other is used as the data byte. Two additional I/O spaces are used to read the status lines on the interface bus and to force a reset of the System One hardware if desired.

Master Clock Circuit <1>

The master clock for System One functions is provided by a 20 MHz oscillator. Q451 operates as a Colpitts oscillator with Y341 as the frequency reference element. C3501 pads the impedance of the crystal to allow some adjustment of frequency. R4404, C4503 and C4502 filter the +15V supply to eliminate noise coupling into the oscillator. C4401, R4405 and R4502 shift the signal from the oscillator to TTL logic levels for buffering by U441. Each of the four buffers drives a separate module to eliminate interaction between the cards and maximize signal amplitude. Resistors R3401 and R3302 reduce ringing on the clock lines and provide a controlled rise time.

Microprocessor <1>

The control functions are provided by U371, an Intel 80C188 CMOS 16-bit microprocessor with an 8-bit interface bus. It is similar to the 8088 microprocessor used in IBM type personal computers except that the clock generation, DMA, memory decoding peripheral decoding are included on chip. It also includes three onboard counter timers. The microprocessor executes a program loop which receives commands over RS232 or GPIB, parses them, programs the hardware appropriately and returns readings from the hardware when requested.

The microprocessor runs from the 20 MHz master clock via jumper R4701. This is divided by 2 internally to form the bus clock. The microprocessor contains all necessary chip select logic for enabling ROMs and RAMs. Supply voltage sensor U271 resets the microprocessor U371 and the remaining hardware when the supply voltage drops below 4.75V. It also has an active high open collector output which holds the chip select high during this time to prevent accidental writes to the EEROMs when the microprocessor is going down.

Octal latch U391 and OR gate U461A display status information during the microprocessors startup sequence and is used for factory test of circuit boards.

Memory <2>

The 8-bit data bus is multiplexed with the lower 8 address lines from the microprocessor. These eight bidirectional bus lines are labeled D0 through D7. 8-bit latch U171 demultiplexes the lower address lines to produce a 16-bit address bus. The address bus is labeled A0 through A15, lines A16 through A19 are not used.

The microprocessor does not contain RAM. In the MFI-3 this is provided by 32k x 8 static RAM U172. Program memory for the MFI-3 is contained in ROMs U181, U182 and U191. U181 is enabled by the /UCS output and contains the boot code. The other two ROMs are enabled by /MCS2 and /MCS3.

Configuration Switches <3>

Tri-state buffer U111 and rocker switch S111 supply the bus address for GPIB applications or the baud rate selections for RS232 applications.

Short Interval Timer <3>

The timer information is obtained by the 8-bit counter U162. A 4 kHz signal derived from one of the 80C188 internal counter timers. The resulting resolution of the timer is 0.48 msec. The counter will rollover at 122.88 msec.

System One Interface Logic <3,4>

The data and address information from the APIB controller share the same 8-bit bus to the System One hardware. The interface also contains three strobe lines to indicate which type of information is carried on the bus at the time. These are described in the accompanying interface description. The bus timing is achieved by stretching all read and write operations of the host microprocessor bus to approximately 2 usec.

The Audio Precision Interface Bus connector is P211 at the right edge of the schematic. The four connectors for the cables to the modules are P421, P431, P432 and P441. Power supply connections enter through J351.

Wait State Generator <3>

The peripheral chip select signal from the 80C188 drives U261 and U161E for the final address decoding, U461D where it enables the bus driver U121 and U361B (through U161E) where it triggers the memory not ready pulse. The output of nand gate U361A will go high when either /IOR or /IOW are asserted. When this occurs, and the output of U161E is high there has been a read from or write to one of the addresses occupied by the System One interface. This drives the output of U361B low, turning on tri-state buffer U362C and releasing the counter U463 from reset. The counter is clocked from the 20 MHz master clock, allowing repeatable timing of the wait states. The outputs start from the low state, forcing a low on the IORDY line. This tells the micro-processor to wait while the write or read cycle is completed. At the end of the 2 usec interval the output of U463 will go high, releasing the processor from the wait state. An earlier output from the counter (at 1.5 usec) is used to force the write strobe line (EW) on the System One interface to finish its pulse before the host processor is released from the wait state. This guarantees that the data to be latched into the System One is still valid when the strobe pulse reaches the end of the cable.

Bus Drive <3>

The decoder U261 decodes the write and read operations to drive the appropriate strobe lines on the System One interface. The selected output of U261 will go low to implement the appropriate function. The 1Y3 output is enabled for data writes, driving the interface line EW high via inverter U262D. The 1Y2 output goes low for address writes driving the interface line EA high through U262C. The 1Y1 output is used to control the enabling of interrupts from the System One via U462B and to clear pending interrupts in U462A. The 1Y0 output drives the System One interface reset line through U262B, forcing ERST high, resetting all hardware modules.

The 2Y3 output of U261 goes low for data reads from the System One. This enables the output of the tri-state buffer U122 and places the data it onto the micro-processor bus. This output also drives the line ER on the System One interface, causing devices in the System One to place their data on the interface. The 2Y2 output of U261 drives the 4-bit tri-state buffer U161. The buffer outputs allow reads of the three System One status lines and the state of flip-flop U462A which latches any occurrence of an interrupt.

Bus Receive <3,4>

All data going out of the host is buffered by octal bus transceiver U121. The eight capacitors typified by C3103 limit the rise time of the data edges to reduce EMI generation. Data being read from the System One is buffered by the transparent octal latch U122. The eight RC networks, of which R221A/C3201 is typical, reduce noise picked up in the lines. Data entering the System One mainframe is filtered by the same networks and buffered by the octal bus transceiver U421. This data drives the address latch U221 and the four module connectors P421, P431, P432 and P441. The address information is latched and drives an additional eight lines on the module connectors. Data leaving the System One measurement hardware is buffered by octal buffer U411. Resistor network R2101 pulls the bus lines high when they are tri-stated to prevent oscillations of the bus buffers when the lines assume voltages near TTL threshold.

When the APIB controller places address information on the bus it strobes the EA line high. This is filtered by R1601 and C2607 to remove noise and buffered by inverter U262G. This produces a low going pulse which is used to strobe the address latch U221. This information is held until the next address write operation by the host.

When data is written from the APIB controller to the System One the EW line is pulled high. This is filtered by R1601 and C2608 and buffered by inverter U262H. The output of this gate is the /WR line which strobes low to write data into any module in the System One.

When data is read from the System One into the APIB controller the ER line is pulled high. This is filtered by R1601 and C2605 and buffered by inverter U262E. The output of this gate is the /SRD line which strobes low to read data from any module in the System One. The /SRD line is combined with the /ATT line to enable the output bus buffer U411 and inverted by U441H and used to disable the input buffer U421. This prevents any bus contention by multiple buffers being active at one time.

When any module in the System One mainframe senses its address on the address bus it pulls the /ATT line low. This serves two purposes. This information is passed to the microcomputer on the /EATT line so that the host may determine if a particular module is present. The outputs of U362A are open collector allowing the external bus to be wire ORed with other enclosures. The /ATT signal is also used to disable the read buffer U411 via U461 if there are no modules in the System One at that address. This allows multiple System One enclosures to be present on the external bus at the same time, if only one module at each address is used.

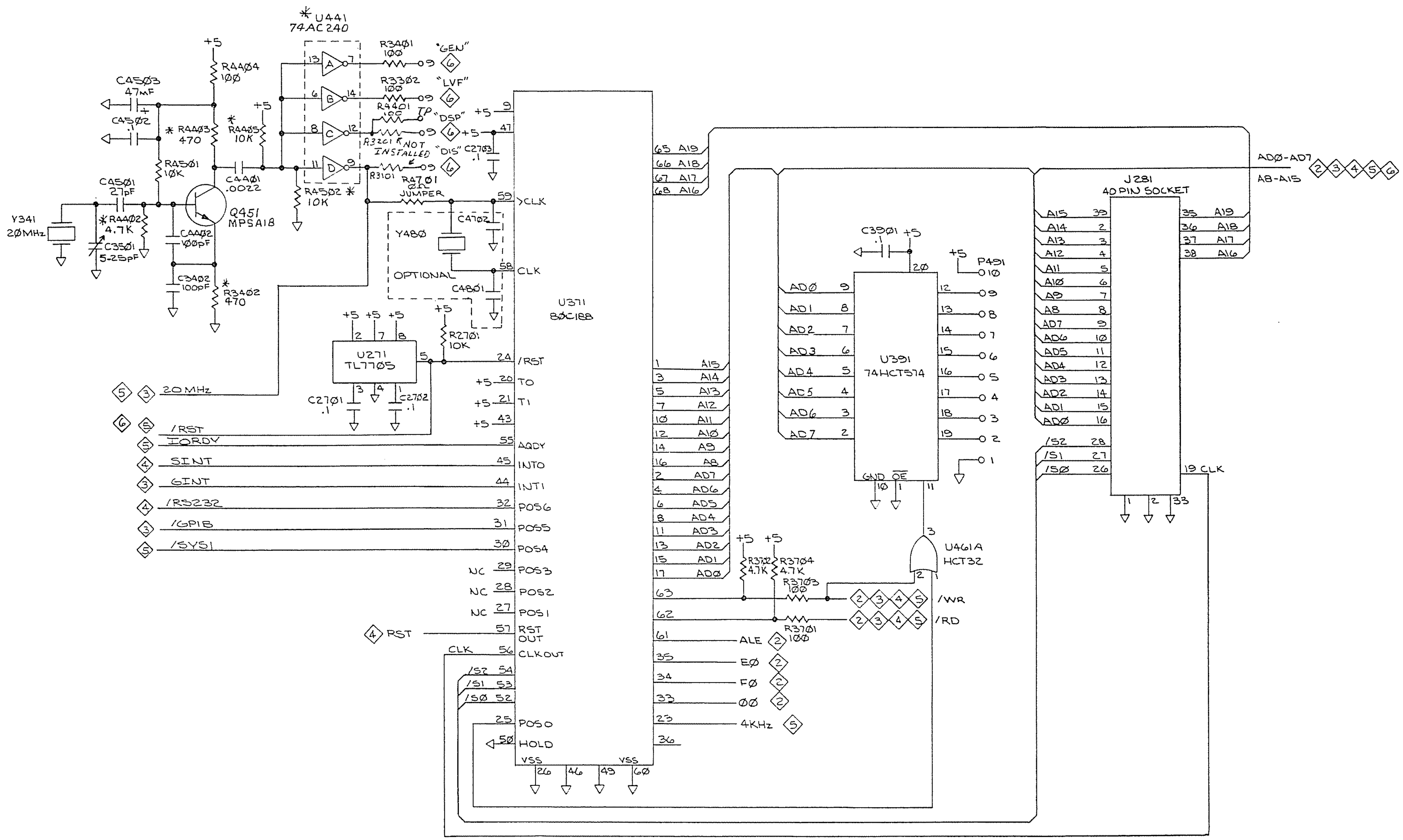
Reset Circuit <1,3,4>

Resetting of the measurement hardware can be initiated by either the host computer or by power cycling of the System One mainframe. The power-on reset is generated by the +5V supply sensor IC U271. The reset signal (ERST) from the host computer enters the System One via pin 16 of P211, the digital interface connector. A high level on this line forces reset. Because of the pull up resistor R4101, disconnecting the cable when the hardware is in the APIB mode will also cause a reset. This line is filtered to remove noise and buffered by one section of inverter U262. NAND gates U361C and U361D are used to combine these two reset signals. Its output goes low, providing the /RESET signal to each of the modules.

Miscellaneous Bus Operations

Diode D2101 is used to pull the PWR line low if the mainframe loses power. This may be sensed by the host to determine the failure. The /SIRQ line is a wired ORed signal from the modules which is used to signal the host that service is necessary. It is buffered by U362 and drives the external bus in an open collector fashion. This allows the /EIRQ signal to be wire ORed among multiple System One enclosures. IRQ assertions which happen internally or on the external APIB bus are buffered by U161E and latched in U462. The state of U462 is read by the microprocessor via tri-state buffer U161. The /AUX signal is used by the dsp to signal that a new reading is ready.

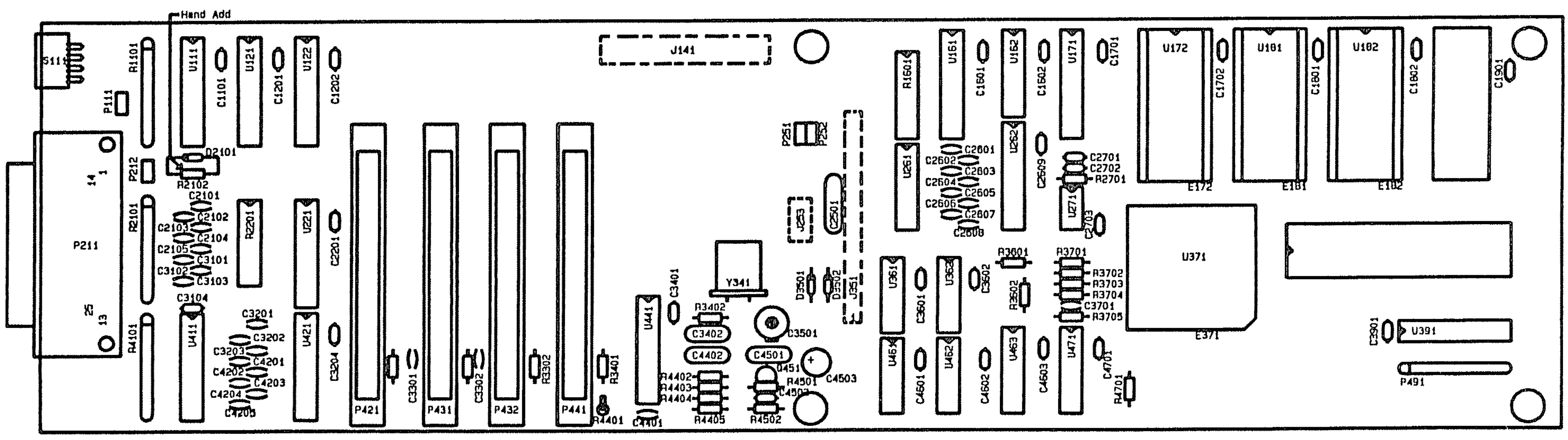
REV	DATE	ECO#	DESCRIPTION	
3	1-15-91	91-003	Add R2102 (SNS)	COS



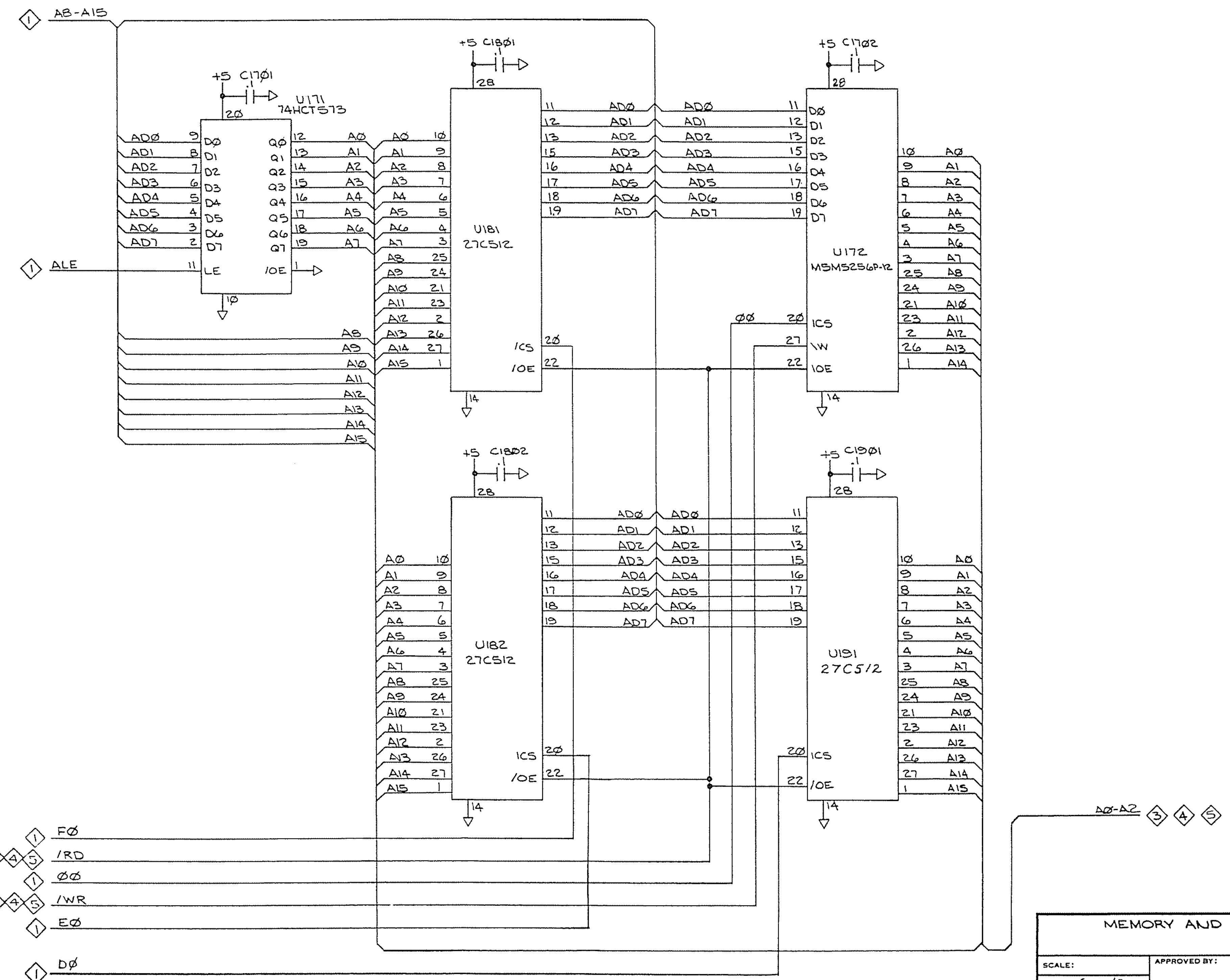
*EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.

CPU AND CLOCK		
SCALE:	APPROVED BY:	DRAWN BY COS
DATE: 8/13/90		REVISED 1-7-91
MAINFRAME INTERFACE (MFI-3)		
SHEET 1 of 4		DRAWING NUMBER 9MFI.3000

17 X 22 PRINTED ON NO. 1000H CLEARPRINT



MAINFRAME INTERFACE 9MFI.3000 (6400.MFI3.3)



MEMORY AND BUFFERS

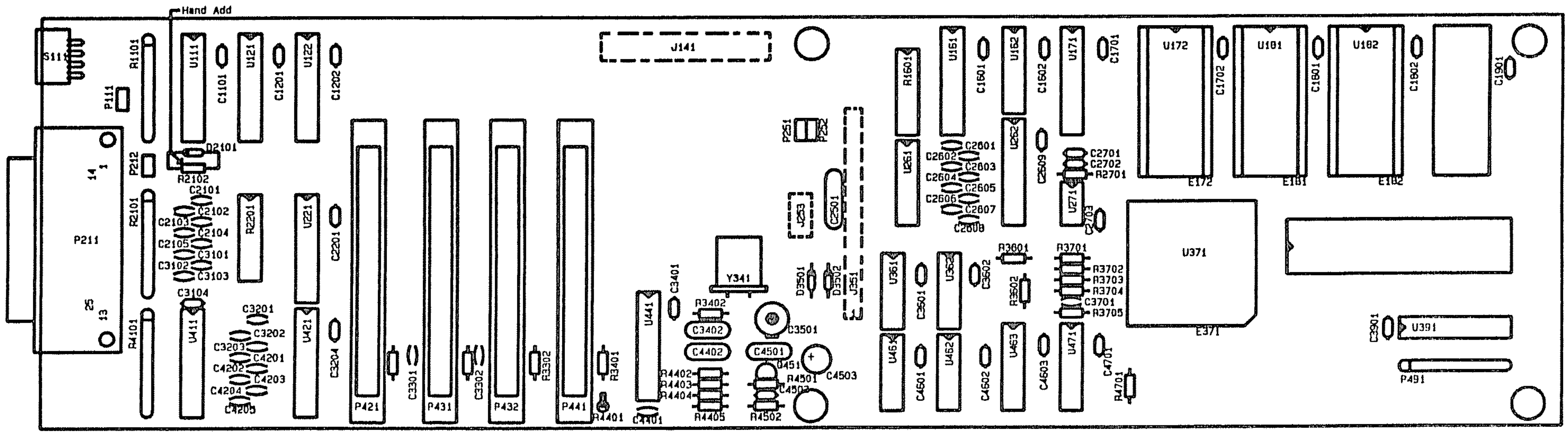
SCALE:	APPROVED BY:	DRAWN BY
DATE: 8/13/90		REVISED

MAINFRAME INTERFACE (MFI-3)

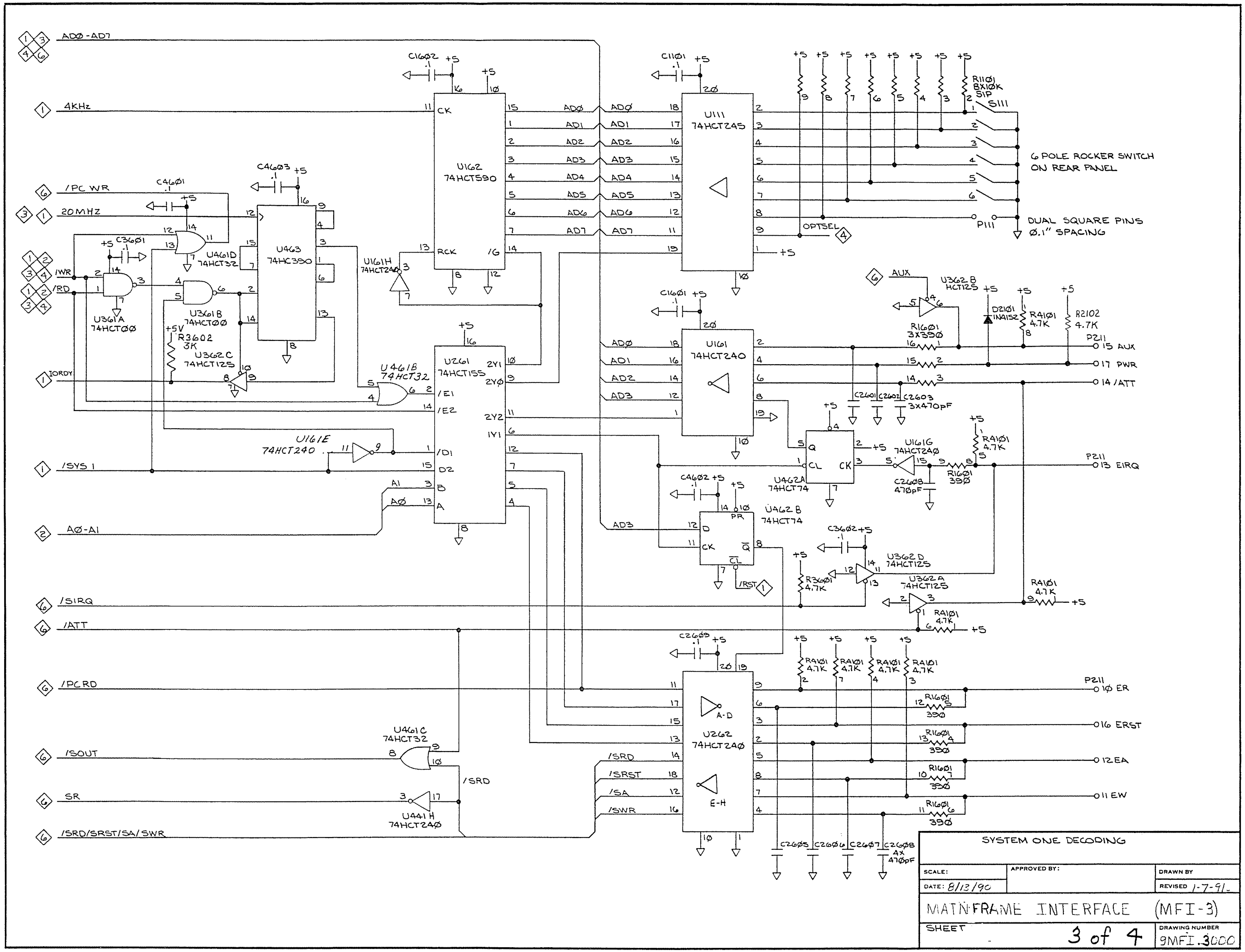
SHEET 2 of 4

DRAWING NUMBER 9MFI.3000

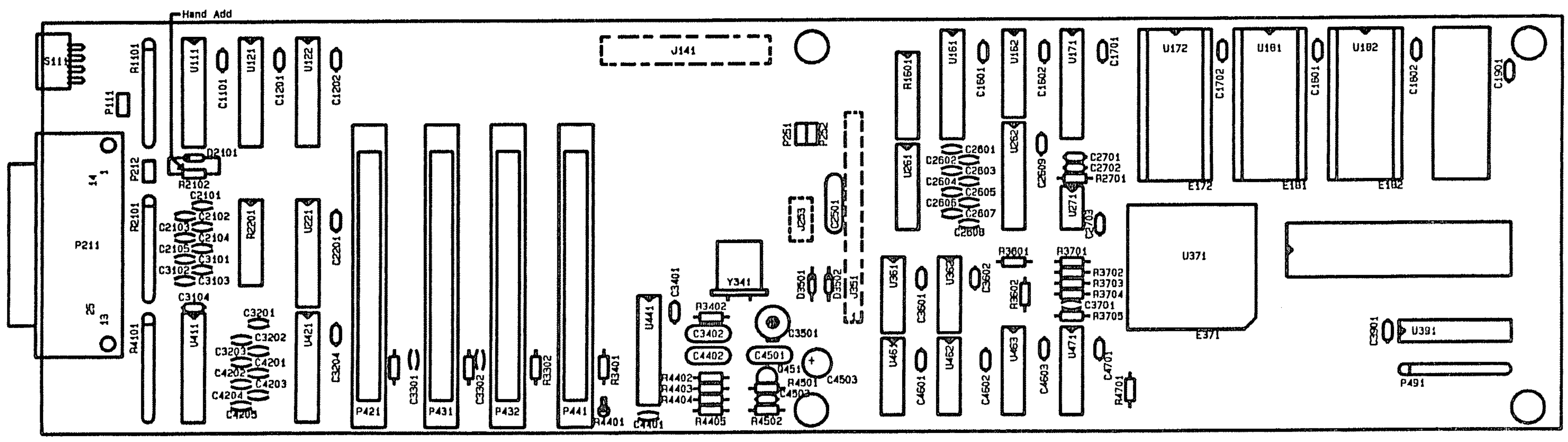
17 X 22 PRINTED ON NO. 1000H CLEARPRINT



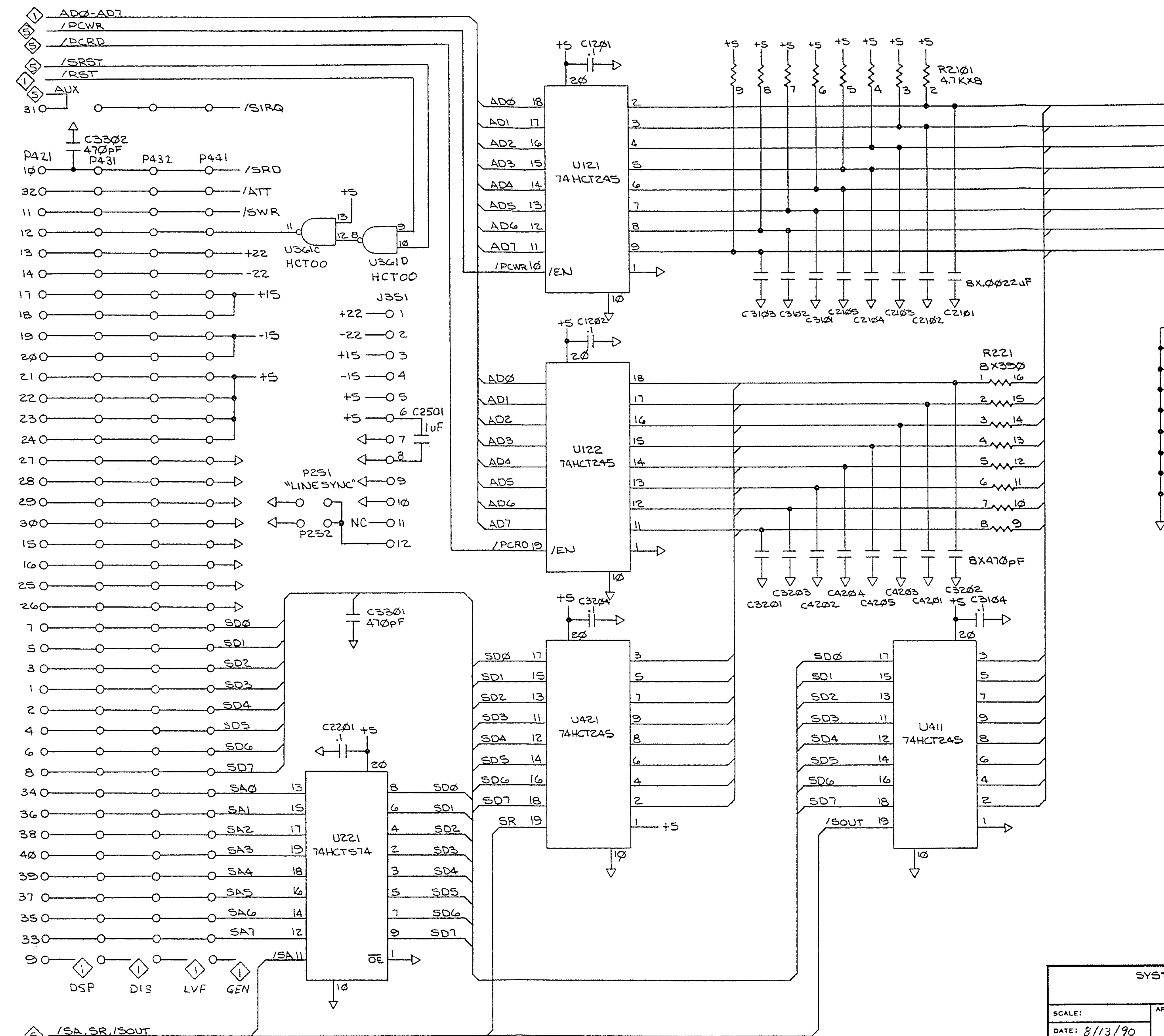
MAINFRAME INTERFACE 9MFI.3000 (6400.MFI3.3)



17 X 22 PRINTED ON NO. 1000H CLEARPRINT



MAINFRAME INTERFACE 9MFI.3000 (6400.MFI3.3)



SYSTEM ONE INTERFACE

SCALE:	APPROVED BY:	DRAWN BY
DATE: 8/13/90		REVISED

MAINFRAME INTERFACE (MFI-3)

SHEET 4 of 4

DRAWING NUMBER 9MFI.3000

17 X 22 PRINTED ON NO. 1000H CLEARPRINT

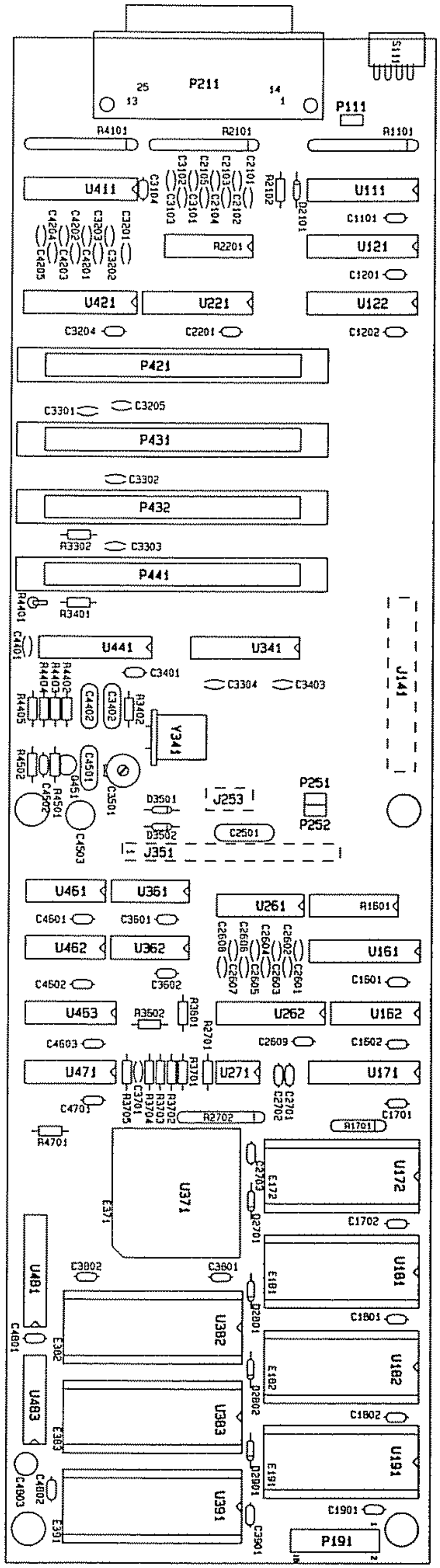
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	5A6	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	6A5	2172.0104	CAP CERAM 100V 20%	.1uF
C1202	6C5	2172.0104	CAP CERAM 100V 20%	.1uF
C1601	5C6	2172.0104	CAP CERAM 100V 20%	.1uF
C1602	5A4	2172.0104	CAP CERAM 100V 20%	.1uF
C1701	2B3	2172.0104	CAP CERAM 100V 20%	.1uF
C1702	2B6	2172.0104	CAP CERAM 100V 20%	.1uF
C1801	2B4	2172.0104	CAP CERAM 100V 20%	.1uF
C1802	2E4	2172.0104	CAP CERAM 100V 20%	.1uF
C1901	2E6	2172.0104	CAP CERAM 100V 20%	.1uF
C2101	6C7	2172.0222	CAP CERAM 100V 20%	.0022uF
C2102	6C7	2172.0222	CAP CERAM 100V 20%	.0022uF
C2103	6C7	2172.0222	CAP CERAM 100V 20%	.0022uF
C2104	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C2105	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C2201	6F3	2172.0104	CAP CERAM 100V 20%	.1uF
C2501	6D4	2454.0105	CAP POLYE 50V 5%	1uF
C2601	5D7	2172.0471	CAP CERAM 100V 20%	470pF
C2602	5D7	2172.0471	CAP CERAM 100V 20%	470pF
C2603	5D7	2172.0471	CAP CERAM 100V 20%	470pF
C2604	5E7	2172.0471	CAP CERAM 100V 20%	470pF
C2605	5H6	2172.0471	CAP CERAM 100V 20%	470pF
C2606	5H7	2172.0471	CAP CERAM 100V 20%	470pF
C2607	5H7	2172.0471	CAP CERAM 100V 20%	470pF
C2608	5H7	2172.0471	CAP CERAM 100V 20%	470pF
C2609	5F6	2172.0104	CAP CERAM 100V 20%	.1uF
C2701	1D3	2172.0104	CAP CERAM 100V 20%	.1uF
C2702	1D3	2172.0104	CAP CERAM 100V 20%	.1uF
C2703	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C3101	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3102	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3103	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3104	6E7	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C3202	6E7	2172.0471	CAP CERAM 100V 20%	470pF
C3203	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C3204	6E5	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	6F3	2172.0471	CAP CERAM 100V 20%	470pF
C3302	6B1	2172.0471	CAP CERAM 100V 20%	470pF
C3401	3F3	2172.0104	CAP CERAM 100V 20%	.1uF
C3402	1D2	2296.0101	CAP MICA 500V 1%	100pF
C3501	1C2	4450.0250	VAR CAP PC	5-25pF
C3601	5C2	2172.0104	CAP CERAM 100V 20%	.1uF
C3602	5E7	2172.0104	CAP CERAM 100V 20%	.1uF
C3701	3H3	2172.0470	CAP CERAM 100V 20%	47pF
C3901	1C7	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	6E7	2172.0471	CAP CERAM 100V 20%	470pF
C4202	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C4203	6E7	2172.0471	CAP CERAM 100V 20%	470pF
C4204	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C4205	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C4401	1C2	2172.0222	CAP CERAM 100V 20%	.0022uF

REPLACEABLE ELECTRICAL PARTS LIST: 9MFI.3000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C4402	1C2	2296.0101	CAP MICA 500V 1%	100pF
C4501	1C2	2294.0270	CAP MICA 500V 5%	27pF
C4502	1B2	2172.0104	CAP CERAM 100V 20%	.1uF
C4503	1B2	2932.0476	CAP AL-EL 25V 20%	47uF
C4601	5B2	2172.0104	CAP CERAM 100V 20%	.1uF
C4602	5E6	2172.0104	CAP CERAM 100V 20%	.1uF
C4603	5B3	2172.0104	CAP CERAM 100V 20%	.1uF
C4701	3G3	2172.0104	CAP CERAM 100V 20%	.1uF
D2101	5C8	3110.4152	DIODE SIGNAL	4152
D3501	4G3	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D3502	4G3	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
J141	3C4,4C3,4F3	4221.1024	JACK PC 2 X .1	24 PIN
J253	3G3,4G3	4221.1008	JACK PC 2 X .1	8 PIN
J281	1C8	4232.1040	SOCKET IC WIDE	40 PIN
J351	6C3	4152.0012	CABLE ASSY .156 18Ga	12 COND
P111	5C8	4221.0036	PLUG PC .1 X.43	36 PIN
P211	5D9,5E9,5G9,6B8	4225.0125	PLUG D-SUB PC 90'	25 PIN
P251	6D3	4221.0036	PLUG PC .1 X.43	36 PIN
P252	6D3	4221.0036	PLUG PC .1 X.43	36 PIN
P421	6H1	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P431	6H2	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P432	6H2	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P441	6H2	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P491	1D7	4221.0036	PLUG PC .1 X.43	36 PIN
Q451	1C2	3211.0018	XSTR NPN TO92	MPSA18
R1101	5A7,5A8	1984.9103	RES NET SIP 5% B	9 X 10K
R1601	5D7,5E8,5G8,5H8	1994.8391	RES NET DIP 5%	8 X 390
R2101	6A7	1984.9472	RES NET SIP 5% B	9 X 4.7K
R2201	6D7	1994.8391	RES NET DIP 5%	8 X 390
R2701	1D4	1214.0103	RES 1/4W C FLM 5%	10K
R3302	1B4	1214.0101	RES 1/4W C FLM 5%	100
R3401	1B4	1214.0101	RES 1/4W C FLM 5%	100
R3402	1D2	1214.0471	RES 1/4W C FLM 5%	470
R3601	5F7	1214.0472	RES 1/4W C FLM 5%	4.7K
R3602	5D2	1214.0302	RES 1/4W C FLM 5%	3.0K
R3701	1F6	1214.0101	RES 1/4W C FLM 5%	100
R3702	1F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R3703	1F6	1214.0101	RES 1/4W C FLM 5%	100
R3704	1F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R3705	3G3	1214.0471	RES 1/4W C FLM 5%	470
R4101	5C8,5D8,5F8,5F7	1984.9472	RES NET SIP 5% B	9 X 4.7K
R4401	2B3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4402	1C2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4403	1B2	1214.0471	RES 1/4W C FLM 5%	470
R4404	1B2	1214.0101	RES 1/4W C FLM 5%	100
R4405	1B3	1214.0103	RES 1/4W C FLM 5%	10K
R4501	1C2	1214.0103	RES 1/4W C FLM 5%	10K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4502	1C3	1214.0103	RES 1/4W C FLM 5%	10K
R4701	1C3	1214.0000	JUMPER .4 X.25	00
S111	5B8	4311.0006	SWITCH DIP 90'	6 POLE
U111	5B6	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U121	6B5	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U122	6D5	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U161	3E3,5D3,5D4,5D6,5D7	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U162	5B4	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U171	2C3	3324.0573	LATCH 8X TRI-ST	74HCT573
U172	2C6	3722.5256	SRAM CMOS 120ns	32K X 8
U181	2C4	3723.27512	EPROM CMOS 150ns	64K X 8
U182	2E4	3723.27512	EPROM CMOS 150ns	64K X 8
U221	6G3	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U261	5D4	3324.0155	DECODER 2 X 2-LN/4-LN	74HCT155
U262	5G6	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U271	1D3	3450.7705	SUPPLY VOLT SENSOR	5V
U361	5C1,5C2,6B3	3324.0000	GATE 4 X 2-IN NAND	74HCT00
U362	5C7,5D3,5F7	3324.0125	BUFFER 4X TRI-ST	74HCT125
U371	1C5	3331.0188	uPROCESSOR CMOS	80C188
U391	1D7	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U411	6F7	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U421	6F5	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U441	1B3,3F3,5H4	3325.0240	BUFFER 8X INV TRI-ST	74AC240
U461	1E7,5C2,5D4,5G4	3324.0032	GATE 4 X 2-IN OR	74HCT32
U462	5D7,5E6	3324.0074	FLIP-FLOP 2X D	74HCT74
U463	5C3	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U471	3G3	3323.4040	COUNTER 12-STAGE	74HC4040
Y341	1C1	3900.0020	CRYSTAL	20MHz

MAINFRAME INTERFACE 9MFI.4000 (6400.MFI4.3)



MFI-4, MAINFRAME INTERFACE ASSEMBLY

NOTE: There are five possible versions of the mainframe interface assembly depending upon the digital interface option (see Section 1.3), system configuration, and age. The MFI version can be determined from the identification decal attached to the rear panel digital connector. The code number will have the format "MFIx-yyyyy-zz" where "x" is the MFI version.

Introduction

The MFI-4 mainframe interface board provides five basic functions: master clock generation, GPIB or RS232 interface decoding and buffering, Audio Precision Interface Bus decoding and buffering, power on reset generation, and signal distribution to the four module compartments in the System One mainframe. The selection of RS232 or GPIB interface is made via a daughter board, the OMI-3, which contains the appropriate interface logic.

The MFI-4 contains all of the circuitry for communicating with a personal computer over the "APIB" (Audio Precision Interface Bus) interface bus. In addition it contains a reduced capability version of a personal computer and personal computer interface (PCI) card. The internal computer can then translate commands received over the GPIB or RS232 interface and convert them to APIB commands. These commands will drive the hardware internal to the System and will also appear on the rear panel APIB connector. Other System One equipment such as a DCX-127 or SWR-122 modules may be connected to the APIB connector. The internal computer will then control these as well. If desired, the internal computer may be disabled via the rocker switches on the rear panel and the System One will operate over the APIB from an external personal computer. The processor reads these on power up to see if it should be in APIB or internal computer mode. If APIB mode is selected, the internal computer shuts down and will not restart without power cycling.

System One Interface

The System One interface is a byte-wide multiplexed address and data bus. There are 256 addresses available in the System One from the eight bits of address information. The main functions of the interface are mapped into two I/O spaces of the host computer interface bus. One output byte from the host is used as the address byte. The other is used as the data byte. Two additional I/O spaces are used to read the status lines on the interface bus and to force a reset of the System One hardware if desired.

Master Clock Circuit <1>

The master clock for System One functions is provided by a 20 MHz oscillator. Q451 operates as a Colpitts oscillator with Y341 as the frequency reference element. C3501 pads the impedance of the crystal to allow some adjustment of frequency. R4404, C4503 and C4502 filter the +15V supply to eliminate noise coupling into the oscillator. C4401, R4405 and R4502 shift the signal from the oscillator to TTL logic levels for buffering by U441. Each of the four buffers drives a separate module to eliminate interaction between the cards and maximize signal amplitude. Resistors R3401 and R3302 reduce ringing on the clock lines and provide a controlled rise time.

Microprocessor <1>

The control functions are provided by U371, an Intel 80C188 CMOS 16-bit microprocessor with an 8-bit interface bus. It is similar to the 8088 microprocessor used in IBM type personal computers except that the clock generation, DMA, memory decoding peripheral decoding are included on chip. It also includes three onboard counter timers. The microprocessor executes a program loop which receives commands over RS232 or GPIB, parses them, programs the hardware appropriately and returns readings from the hardware when requested.

The microprocessor runs from the 20 MHz master clock via jumper R4701. This is divided by 2 internally to form the bus clock. The microprocessor contains all necessary chip select logic for enabling ROMs and RAMs. Supply voltage sensor U271 resets the microprocessor U371 and the remaining hardware when the supply voltage drops below 4.75V. It also has an active high open collector output which holds the chip select high during this time to prevent accidental writes to the EEROMs when the microprocessor is going down.

Memory <2>

The 8-bit data bus is multiplexed with the lower 8 address lines from the microprocessor. These eight bidirectional bus lines are labeled AD0 through AD7. 8-bit latch U171 demultiplexes the lower address lines to produce a 16-bit address bus. The address bus is labeled A0 through A15, lines A16 through A19 are not used.

The microprocessor does not contain RAM. In the MFI-4 this is provided by a 128k x 8 static RAM U382. Program memory is contained in two 128k x 8 ROMs U383 and U391. The /UCS output from the 80C188 is decoded by 2-to-4 line decoder U483 to provide independent chip select signals for the two ROMs. Program storage for the DSP module in GPIB applications is supplied by four EEROM devices U172, U181, U182 and U191 which are driven from /MCS0-/MCS3. Their chip select inputs are clamped to the supply during power up and down by diodes D2701, D2801, D2802, D2901, and power supply sensor U271.

Configuration Switches <3>

Tri-state buffer U111 and rocker switch S111 supply the bus address for GPIB applications or the baud rate selections for RS232 applications.

Short Interval Timer <3>

The timer information is obtained by the 8-bit counter U162. A 4 kHz signal derived from one of the 80C188 internal counter timers. The resulting resolution of the timer is 0.48 msec. The counter will rollover at 122.88 msec.

System One Interface Logic <4>

The data and address information from the APIB controller share the same 8-bit bus to the System One hardware. The interface also contains three strobe lines to indicate which type of information is carried on the bus at the time. These are described in the accompanying interface description. The bus timing is achieved by stretching all read and write operations of the host microprocessor bus to approximately 2 usec.

The Audio Precision Interface Bus connector is P211 at the right edge of the schematic. The four connectors for the cables to the modules are P421, P431, P432 and P441. Power supply connections enter through J351.

Wait State Generator <3>

The peripheral chip select signal from the 80C188 drives U261 and U161E for the final address decoding, U461D where it enables the bus driver U121 and U361B (through U161E) where it triggers the memory not ready pulse. The output of nand gate U361A will go high when either /IOR or /IOW are asserted. When this occurs, and the output of U161E is high there has been a read from or write to one of the addresses occupied by the System One interface. This drives the output of U361B low, turning on tri-state buffer U362C and releasing the counter U463 from reset. The counter is clocked from the 20 MHz master clock, allowing repeatable timing of the wait states. The outputs start from the low state, forcing a low on the IORDY line. This tells the microprocessor to wait while the write or read cycle is completed. At the end of the 2 usec interval the output of U463 will go high, releasing the processor from the wait state. An earlier output from the counter (at 1.5 usec) is used to force the write strobe line (EW) on the System One interface to finish its pulse before the host processor is released from the wait state. This guarantees that the data to be latched into the System One is still valid when the strobe pulse reaches the end of the cable.

Bus Drive <3>

The decoder U261 decodes the write and read operations to drive the appropriate strobe lines on the System One interface. The selected output of U261 will go low to implement the appropriate function. The 1Y3 output is enabled for data writes, driving the interface line EW high via inverter U262F. The 1Y2 output goes low for address writes driving the interface line EA high through U262G. The 1Y1 output is used to control the enabling of interrupts from the System One via U462B and to clear pending interrupts in U462A. The 1Y0 output drives the System One interface reset line through U262H, forcing ERST high, resetting all hardware modules.

The 2Y3 output of U261 goes low for data reads from the System One. This enables the output of the tri-state buffer U122 and places the data it onto the microprocessor bus. This output also drives the line ER on the System One interface, causing devices in the System One to place their data on the interface. The 2Y2 output of U261 drives the 4-bit tri-state buffer U161. The buffer outputs allow reads of the three System One status lines and the state of flip-flop U462A which latches any occurrence of an interrupt.

Bus Receive <1,3,4>

All data going out of the host is buffered by octal bus transceiver U121. The eight capacitors typified by C3103 limit the rise time of the data edges to reduce EMI generation. Data being read from the System One is buffered by the transparent octal latch U122. The eight RC networks, of which R211A/C3201 is typical, reduce noise picked up in the lines. Data entering the System One mainframe is filtered by the same networks and buffered by the octal bus transceiver U421. This data drives the address latch U221 and the four module connectors P421, P431, P432 and P441. The address information is latched and drives an additional eight lines on the module connectors. Data leaving the System One measurement hardware is buffered by octal buffer U411. Resistor network R2101 pulls the bus lines high when they are tri-stated to prevent oscillations of the bus buffers when the lines assume voltages near TTL threshold.

When the APIB controller places address information on the bus it strobes the EA line high. This is filtered by R1601 and C2607 to remove noise and buffered by inverter U262D. This produces a low going pulse which is used to strobe the address latch U221. This information is held until the next address write operation by the host.

When data is written from the APIB controller to the System One the EW line is pulled high. This is filtered by R1601 and C2608 and buffered by inverter U262B. The output of this gate is the /SWR line which strobes low to write data into any module in the System One.

When data is read from the System One into the APIB controller the ER line is pulled high. This is filtered by R1601 and C2605 and buffered by inverter U262C. The output of this gate is the /SRD line which strobes low to read data from any module in the System One. The /SRD line is combined with the /ATT line to enable the output bus buffer U411 and inverted by U441H and used to disable the input buffer U421. This prevents any bus contention by multiple buffers being active at one time. In the MFI-4 the /SRD line is buffered independently for each of the four modules in mainframe by quad OR gate U341.

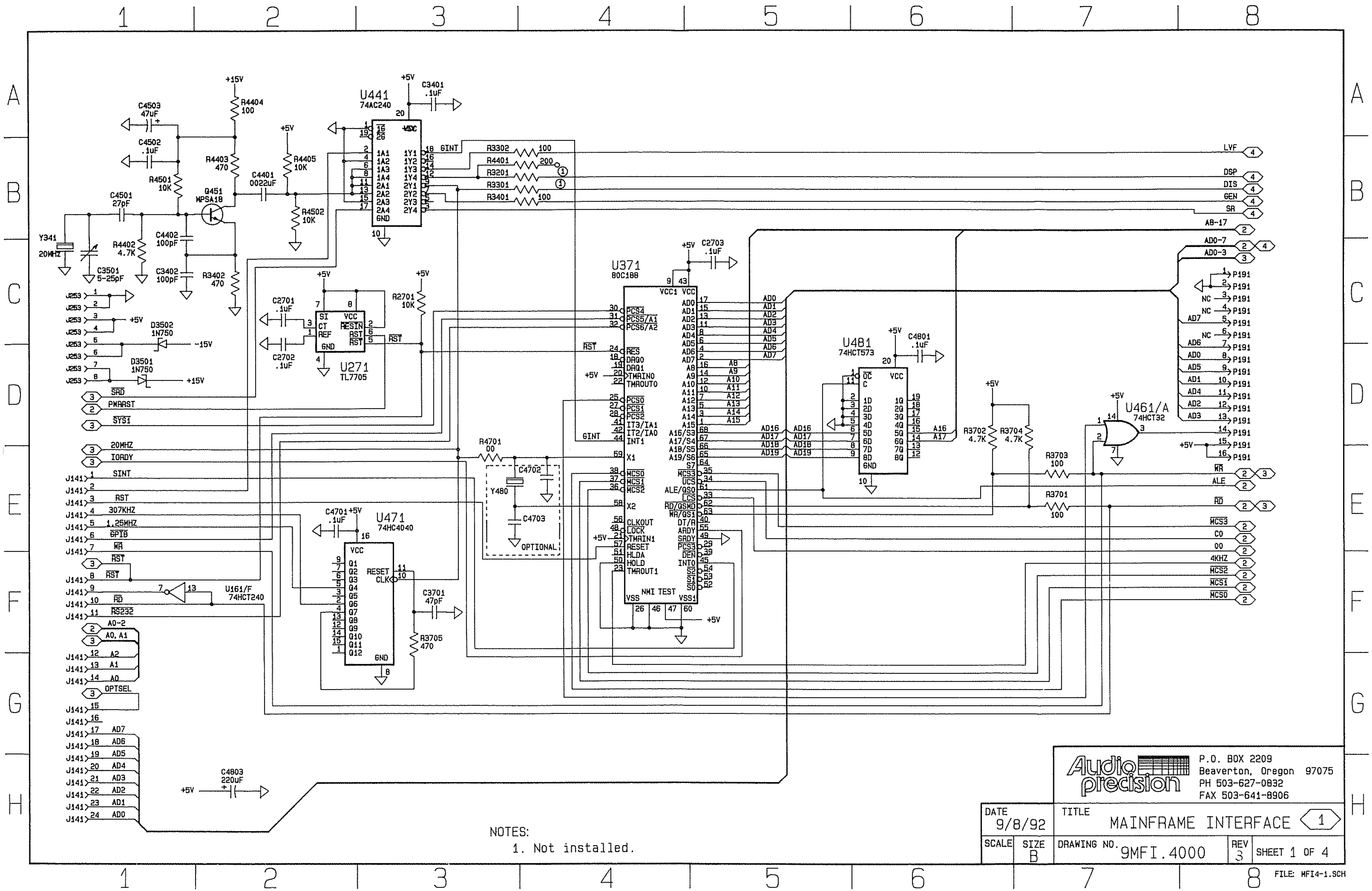
When any module in the System One mainframe senses its address on the address bus it pulls the /ATT line low. This serves two purposes. This information is passed to the microcomputer on the /EATT line so that the host may determine if a particular module is present. The outputs of U362A are open collector allowing the external bus to be wire ORed with other enclosures. The /ATT signal is also used to disable the read buffer U411 via U461 if there are no modules in the System One at that address. This allows multiple System One enclosures to be present on the external bus at the same time, if only one module at each address is used.

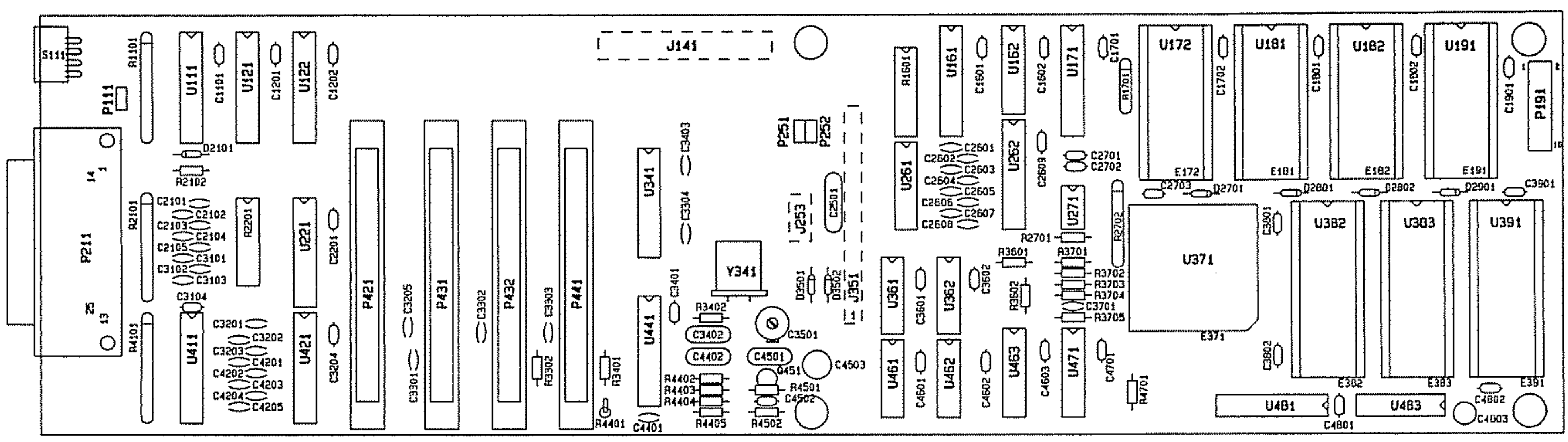
Reset Circuit <1,3,4>

Resetting of the measurement hardware can be initiated by either the host computer or by power cycling of the System One mainframe. The power-on reset is generated by the +5V supply sensor IC U271. The reset signal from the host computer enters the System One via pin 16 of P211, the digital interface connector. A high level on this line forces reset. Because of the pull up resistor R4101, disconnecting the cable when the hardware is in the APIB mode will also cause a reset. This line is filtered to remove noise and buffered by one section of inverter U262. NAND gates U361C and U361D are used to combine these two reset signals. Its output goes low, providing the /RESET signal to each of the modules.

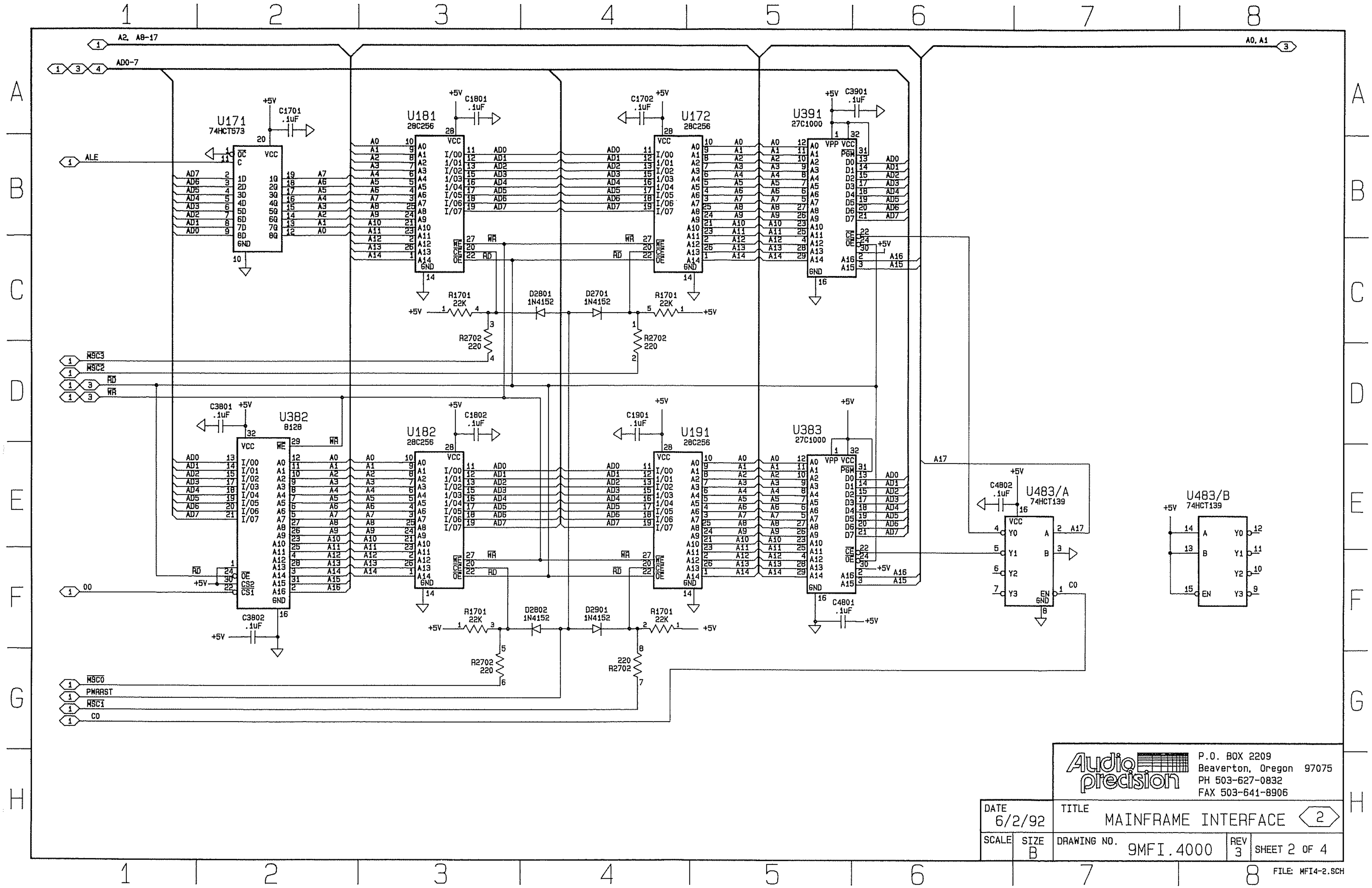
Miscellaneous Bus Operations

Diode D2101 is used to pull the PWR line low if the mainframe loses power. This may be sensed by the host to determine the failure. The /SIRQ line is a wired OR signal from the modules which is used to signal the host that service is necessary. It is buffered by U362 and drives the external bus in an open collector fashion. This allows the /EIRQ signal to be wire ORed among multiple System One enclosures. IRQ assertions which happen internally or on the external APIB bus are buffered by U161G and latched in U462. The state of U462 is read by the microprocessor via tri-state buffer U161. The /AUX signal is used by the dsp to signal that a new reading is ready.

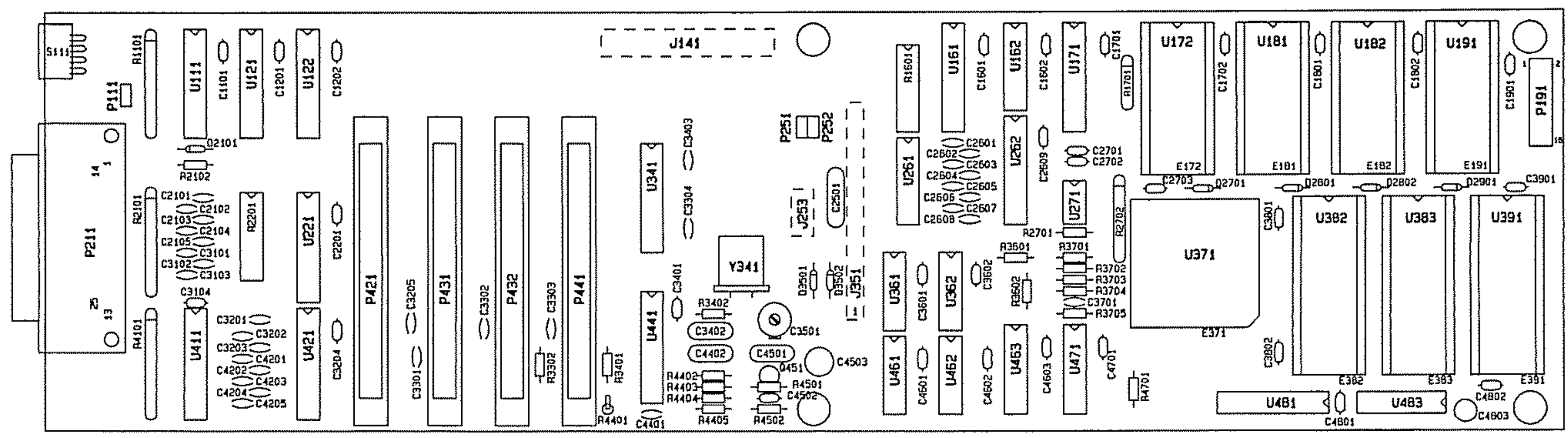

U441
74AC240
U371
80C188
U481
74HCT573
U271
TL7705
U471
74HC4040
U461/A
74HCT32
U161/F
74HCT240
Q451
MPSA18
Y341
20MHZ
Y480
OPTIONAL
LVF
DSP
DIS
GEN
SR
A8-17
AD0-7
AD0-3
SRD
PWRRST
SYSI
20MHZ
IORDY
SINT
RST
307KHZ
1.25MHZ
GPIB
WR
RD
RS232
A0-2
A0, A1
OPTSEL
ALE
MCS3
CO
OO
4KHZ
MCS2
MCS1
MCS0
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
9/8/92
TITLE
MAINFRAME INTERFACE
1
SCALE
SIZE
B
DRAWING NO.
9MFI.4000
REV
3
SHEET 1 OF 4
FILE: MFI4-1.SCH
NOTES:
1. Not installed.



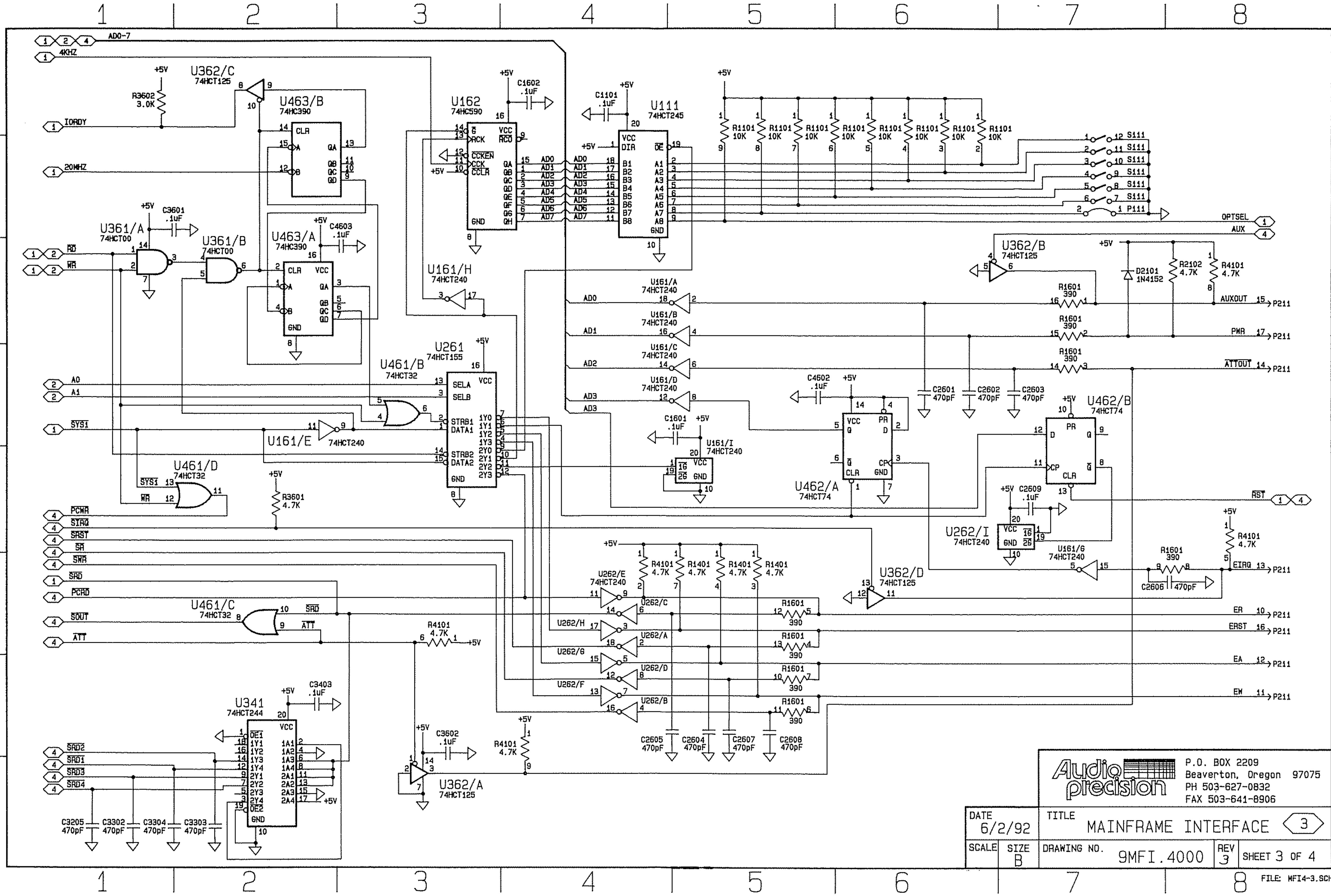
MAINFRAME INTERFACE 9MFI.4000 (6400.MFI4.3)



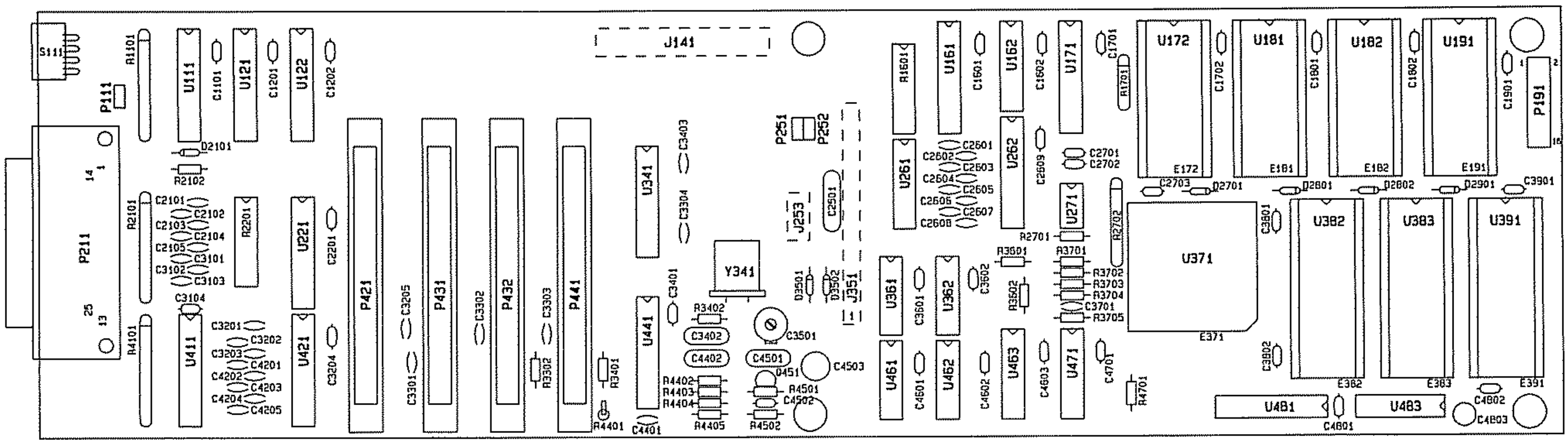
U171
74HCT573
U181
28C256
U172
28C256
U391
27C1000
U382
6128
U182
28C256
U191
28C256
U383
27C1000
U483/A
74HCT139
U483/B
74HCT139
A2, A8-17
AD0-7
A0, A1
ALE
MSC3
MSC2
RD
WR
00
MSC0
PWRRST
MSC1
C0
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
6/2/92
TITLE
MAINFRAME INTERFACE
SCALE
SIZE
B
DRAWING NO.
9MFI.4000
REV
3
SHEET 2 OF 4
FILE: MFI4-2.SCH



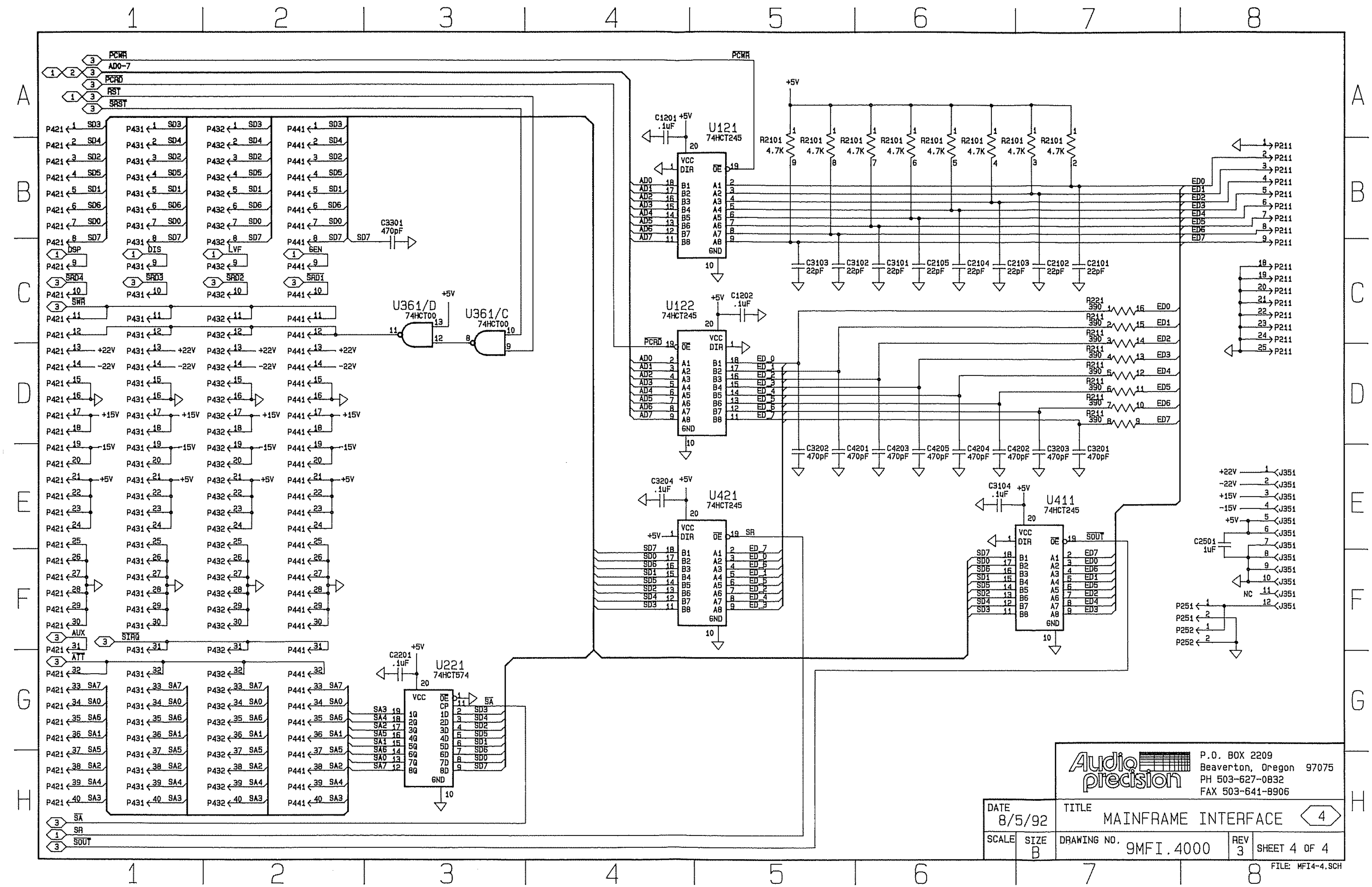
MAINFRAME INTERFACE 9MFI.4000 (6400.MFI4.3)



AD0-7
4KHZ
IORDY
20MHZ
RD
WR
A0
A1
SYS1
PCWR
SIRQ
SRST
SR
SWR
SRD
PCRD
SOUT
ATT
SRD2
SRD1
SRD3
SRD4
U362/C 74HCT125
R3602 3.0K
U463/B 74HC390
U361/A 74HCT00
C3601 .1uF
U361/B 74HCT00
U463/A 74HC390
C4603 .1uF
U162 74HC590
C1602 .1uF
U111 74HCT245
C1101 .1uF
R1101 10K
S111
P111
OPTSEL
AUX
U362/B 74HCT125
D2101 1N4152
R2102 4.7K
R4101 4.7K
R1601 390
AUXOUT
PWR
ATTOUT
P211
U161/H 74HCT240
U161/A 74HCT240
U161/B 74HCT240
U161/C 74HCT240
U161/D 74HCT240
U161/I 74HCT240
C1601 .1uF
U461/B 74HCT32
U261 74HCT155
U161/E 74HCT240
U461/D 74HCT32
R3601 4.7K
C4602 .1uF
U462/A 74HCT74
U462/B 74HCT74
C2601 470pF
C2602 470pF
C2603 470pF
C2609 .1uF
U262/I 74HCT240
U161/G 74HCT240
RST
EIRQ
C2606 470pF
U362/D 74HCT125
U262/E 74HCT240
U262/C
U262/H
U262/A
U262/G
U262/D
U262/F
U262/B
R1401 4.7K
ER
ERST
EA
EW
C2605 470pF
C2604 470pF
C2607 470pF
C2608 470pF
U461/C 74HCT32
U341 74HCT244
C3403 .1uF
C3205 470pF
C3302 470pF
C3304 470pF
C3303 470pF
C3602 .1uF
U362/A 74HCT125
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 6/2/92
TITLE MAINFRAME INTERFACE 3
SCALE
SIZE B
DRAWING NO. 9MFI.4000
REV 3
SHEET 3 OF 4
FILE: MFI4-3.SCH



MAINFRAME INTERFACE 9MFI.4000 (6400.MFI4.3)



Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE	
8/5/92	MAINFRAME INTERFACE	4

SCALE	SIZE	DRAWING NO.	REV	
	B	9MFI.4000	3	SHEET 4 OF 4

FILE: MFI4-4.SCH

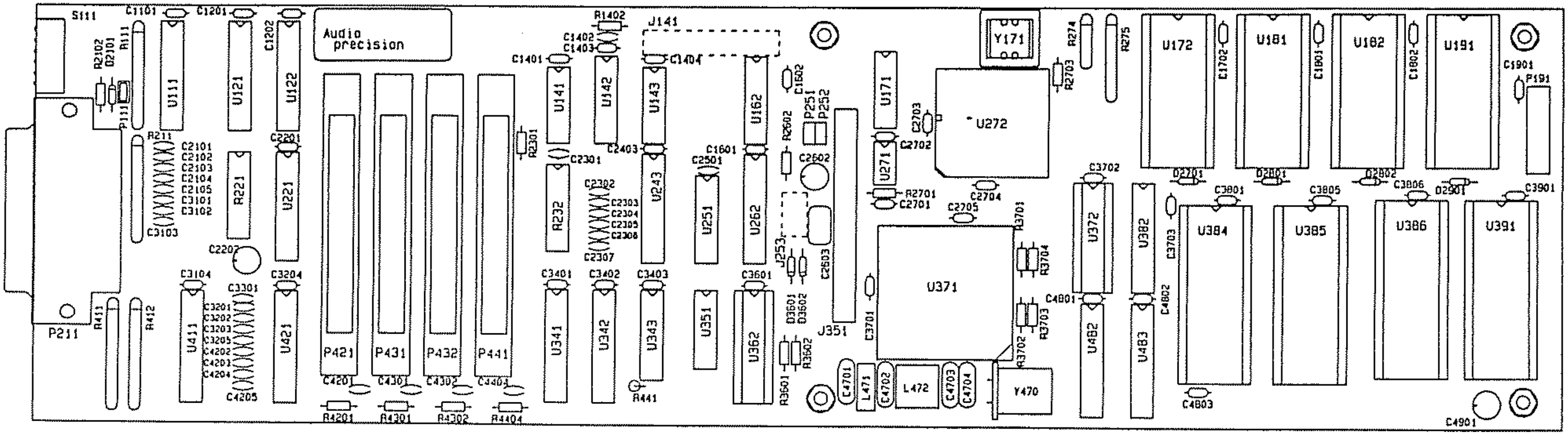
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	5A6	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	6A5	2172.0104	CAP CERAM 100V 20%	.1uF
C1202	6C5	2172.0104	CAP CERAM 100V 20%	.1uF
C1601	5C6	2172.0104	CAP CERAM 100V 20%	.1uF
C1602	5A4	2172.0104	CAP CERAM 100V 20%	.1uF
C1701	2B3	2172.0104	CAP CERAM 100V 20%	.1uF
C1702	2B6	2172.0104	CAP CERAM 100V 20%	.1uF
C1801	2B4	2172.0104	CAP CERAM 100V 20%	.1uF
C1802	2E4	2172.0104	CAP CERAM 100V 20%	.1uF
C1901	2E6	2172.0104	CAP CERAM 100V 20%	.1uF
C2101	6C7	2172.0222	CAP CERAM 100V 20%	.0022uF
C2102	6C7	2172.0222	CAP CERAM 100V 20%	.0022uF
C2103	6C7	2172.0222	CAP CERAM 100V 20%	.0022uF
C2104	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C2105	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C2201	6F3	2172.0104	CAP CERAM 100V 20%	.1uF
C2501	6D4	2454.0105	CAP POLYE 50V 5%	1uF
C2601	5D7	2172.0471	CAP CERAM 100V 20%	470pF
C2602	5D7	2172.0471	CAP CERAM 100V 20%	470pF
C2603	5D7	2172.0471	CAP CERAM 100V 20%	470pF
C2604	5E7	2172.0471	CAP CERAM 100V 20%	470pF
C2605	5H6	2172.0471	CAP CERAM 100V 20%	470pF
C2606	5H7	2172.0471	CAP CERAM 100V 20%	470pF
C2607	5H7	2172.0471	CAP CERAM 100V 20%	470pF
C2608	5H7	2172.0471	CAP CERAM 100V 20%	470pF
C2609	5F6	2172.0104	CAP CERAM 100V 20%	.1uF
C2701	1D3	2172.0104	CAP CERAM 100V 20%	.1uF
C2702	1D3	2172.0104	CAP CERAM 100V 20%	.1uF
C2703	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C3101	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3102	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3103	6C6	2172.0222	CAP CERAM 100V 20%	.0022uF
C3104	6E7	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C3202	6E7	2172.0471	CAP CERAM 100V 20%	470pF
C3203	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C3204	6E5	2172.0104	CAP CERAM 100V 20%	.1uF
C3205	5H1	2172.0471	CAP CERAM 100V 20%	470pF
C3301	6F3	2172.0471	CAP CERAM 100V 20%	470pF
C3302	5H1	2172.0471	CAP CERAM 100V 20%	470pF
C3303	5H1	2172.0471	CAP CERAM 100V 20%	470pF
C3304	5H1	2172.0471	CAP CERAM 100V 20%	470pF
C3401	3F3	2172.0104	CAP CERAM 100V 20%	.1uF
C3402	1D2	2296.0101	CAP MICA 500V 1%	100pF
C3403	3F3	2172.0104	CAP CERAM 100V 20%	.1uF
C3501	1C2	4450.0250	VAR CAP PC	5-25pF
C3601	5C2	2172.0104	CAP CERAM 100V 20%	.1uF
C3602	5E7	2172.0104	CAP CERAM 100V 20%	.1uF
C3701	3H3	2172.0470	CAP CERAM 100V 20%	47pF
C3801	2E3	2172.0104	CAP CERAM 100V 20%	.1uF
C3802	2G3	2172.0104	CAP CERAM 100V 20%	.1uF
C3901	1C7	2172.0104	CAP CERAM 100V 20%	.1uF

REPLACEABLE ELECTRICAL PARTS LIST: 9MFI.4000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C4201	6E7	2172.0471	CAP CERAM 100V 20%	470pF
C4202	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C4203	6E7	2172.0471	CAP CERAM 100V 20%	470pF
C4204	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C4205	6E6	2172.0471	CAP CERAM 100V 20%	470pF
C4401	1C2	2172.0222	CAP CERAM 100V 20%	.0022uF
C4402	1C2	2296.0101	CAP MICA 500V 1%	100pF
C4501	1C2	2294.0270	CAP MICA 500V 5%	27pF
C4502	1B2	2172.0104	CAP CERAM 100V 20%	.1uF
C4503	1B2	2932.0476	CAP AL-EL 25V 20%	47uF
C4601	5B2	2172.0104	CAP CERAM 100V 20%	.1uF
C4602	5E6	2172.0104	CAP CERAM 100V 20%	.1uF
C4603	5B3	2172.0104	CAP CERAM 100V 20%	.1uF
C4701	3G3	2172.0104	CAP CERAM 100V 20%	.1uF
C4801	2G8	2172.0104	CAP CERAM 100V 20%	.1uF
C4802	1F10	2172.0104	CAP CERAM 100V 20%	.1uF
C4803	1G2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
D2101	5C8	3110.4152	DIODE SIGNAL	4152
D2701	5C8	3110.4152	DIODE SIGNAL	4152
D2801	5C8	3110.4152	DIODE SIGNAL	4152
D2802	5C8	3110.4152	DIODE SIGNAL	4152
D2901	5C8	3110.4152	DIODE SIGNAL	4152
D3501	4G3	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D3502	3G4	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
J141	3C4,4V3,4F3	4221.1024	JACK PC 2 X .1	24 PIN
J253	3G3,4G3	4221.1008	JACK PC 2 X .1	8 PIN
J351	6C3	4152.0012	CABLE ASSY .156 18Ga	12 COND
P111	5C8	4221.0036	PLUG PC .1 X.43	36 PIN
P191	1C9	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P211	5D9,5E9,5G9,6B8	4225.0125	PLUG D-SUB PC 90'	25 PIN
P251	6D3	4221.0036	PLUG PC .1 X.43	36 PIN
P252	6D3	4221.0036	PLUG PC .1 X.43	36 PIN
P421	6H1	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P431	6H2	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P432	6H2	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
P441	6H2	4221.0040	PLUG PC W/EJECT 2X.1	40 PIN
Q451	1C2	3211.0018	XSTR NPN TO92	MPSA18
R1101	5A7,5A8	1984.9103	RES NET SIP 5% B	9 X 10K
R1601	5D7,5E8,5G8,5H8	1994.8391	RES NET DIP 5%	8 X 390
R1701		1985.4223	RES NET SIP 2% B	4 X 22K
R2101	6A7	1984.9472	RES NET SIP 5% B	X 4.7K
R2102	6F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R2201	6D7	1994.8391	RES NET DIP 5%	8 X 390
R2701	1D4	1214.0103	RES 1/4W C FLM 5%	10K
R2702		1984.4221	RES NET SIP 5% I	4 X 220
R3302	1B4	1214.0101	RES 1/4W C FLM 5%	100
R3401	1B4	1214.0101	RES 1/4W C FLM 5%	100

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R3402	1D2	1214.0471	RES 1/4W C FLM 5%	470
R3601	5F7	1214.0472	RES 1/4W C FLM 5%	4.7K
R3602	5D2	1214.0302	RES 1/4W C FLM 5%	3.0K
R3701	1F6	1214.0101	RES 1/4W C FLM 5%	100
R3702	1F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R3703	1F6	1214.0101	RES 1/4W C FLM 5%	100
R3704	1F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R3705	3G3	1214.0471	RES 1/4W C FLM 5%	470
R4101	5F7,5C8,5D8,5F8	1984.9472	RES NET SIP 5% B	9 X 4.
R4401	2B3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4402	1C2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4403	1B2	1214.0471	RES 1/4W C FLM 5%	470
R4404	1B2	1214.0101	RES 1/4W C FLM 5%	100
R4405	1B3	1214.0103	RES 1/4W C FLM 5%	10K
R4501	1C2	1214.0103	RES 1/4W C FLM 5%	10K
R4502	1C3	1214.0103	RES 1/4W C FLM 5%	10K
R4701	1C3	1214.0000	JUMPER .4 X.25	00
S111	5B8	4311.0006	SWITCH DIP 90'	6 POLE
U111	5B6	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U121	6B5	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U122	6D5	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U161	3E3,5D3,5D4,5D6,5D7	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U162	5B4	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U171	2C3	3324.0573	LATCH 8X TRI-ST	74HCT573
U172	2C6	3724.28256	EEPROM CMOS 200ns	32K X 8
U181	2C4	3724.28256	EEPROM CMOS 200ns	32K X 8
U182	2E4	3724.28256	EEPROM CMOS 200ns	32K X 8
U191	2E7	3724.28256	EEPROM CMOS 200ns	32K X 8
U221	6G3	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U261	5D4	3324.0155	DECODER 2 X 2-LN/4-LN	74HCT155
U262	5G6	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U271	1D3	3450.7705	SUPPLY VOLT SENSOR	5V
U341	5H2,5H3	3324.0244	BUFFER 8X TRI-STATE	74HCT244
U361	5C1,5C2,6B3	3324.0000	GATE 4 X 2-IN NAND	74HCT00
U362	5D3,5C7,5F7	3324.0125	BUFFER 4X TRI-ST	74HCT125
U371	1C5	3331.0188	uPROCESSOR CMOS	80C188
U382	2E3	3722.8128	SRAM CMOS 120ns	128K X 8
U383	2E9	3723.2710	EPROM CMOS 200ns	128K X 8
U391	1D7	3723.2710	EPROM CMOS 200ns	128K X 8
U411	6F7	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U421	6F5	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U441	1B3,3F3,5H4	3325.0240	BUFFER 8X INV TRI-ST	74AC240
U461	1D8,5C2,5D4,5G4	3324.0032	GATE 4 X 2-IN OR	74HCT32
U462	5D7,5E6	3324.0074	FLIP-FLOP 2X D	74HCT74
U463	5C3	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U471	3G3	3323.4040	COUNTER 12-STAGE	74HC4040
U481	1C7	3324.0573	LATCH 8X TRI-ST	74HCT573
U483	2F10	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
Y341	1C1	3900.0020	CRYSTAL	20MHz

MFI-5 MAINFRAME INTERFACE



MAINFRAME INTERFACE 9MFI.5000 (6400.MFI5.1)

MFI-5, MAINFRAME INTERFACE ASSEMBLY

NOTE: There are five possible versions of the mainframe interface assembly depending upon the digital interface option (see Section 1.3), system configuration, and age. The MFI version can be determined from the identification decal attached to the rear panel digital connector. The code number will have the format "MFIx-yyyyy-zz" where "x" is the MFI version.

Introduction

The MFI-5 mainframe interface board provides five basic functions: master clock generation, GPIB or RS232 interface decoding and buffering, Audio Precision Interface Bus (APIB) decoding and buffering, power on reset generation, and signal distribution to the four module compartments in the System One mainframe. The selection of RS232 or GPIB interface is made via a daughter board, the OMI-3, which contains the appropriate interface logic.

The MFI-5 differs from the MFI-4 in four areas: 1) the microprocessor has been upgraded and operates at twice the speed, 2) an optional coprocessor is supported, 3) RAM space has been doubled, and 4) GPIB Direct Memory Access is supported. All the features of the MFI-4 are included in the MFI-5, including local dsp program storage of GPIB applications to avoid downloading time over the interface bus.

The MFI-5 contains all of the circuitry for communicating with a personal computer over the "APIB" (Audio Precision Interface Bus) interface bus. In addition it contains a reduced capability version of a personal computer and personal computer interface (PCI) card. The internal computer can then translate commands received over the GPIB or RS232 interface and convert them to APIB commands. These commands will drive the hardware internal to the System One and will also appear on the rear panel APIB connector. Other System One equipment such as a DCX-127 or SWR-122 modules may be connected to the APIB connector. The internal computer will then control these as well. If desired, the internal computer may be disabled via the rocker switches on the rear panel and the System One will operate over the APIB from an external personal computer. The processor reads these on power up to see if it should be in APIB or internal computer mode. If APIB mode is selected, the internal computer shuts down and will not restart without power cycling.

System One Interface

The System One interface is a byte-wide multiplexed address and data bus. There are 256 addresses available in the System One from the eight bits of address information. The main functions of the interface are mapped into two I/O spaces of the host computer interface bus. One output byte from the host is used as the address byte. The other is used as the data byte. Two additional I/O spaces are used to read the status lines on the interface bus and to force a reset of the System One hardware if desired.

Master Clock Circuit <1>

The 80C186XL microprocessor used in the MFI-5 has an onboard oscillator. This oscillator uses a third-overtone crystal Y470 for generating a 40 MHz source. L471 and C4701 are required for proper third overtone operation. The 40 MHz is divided by two inside the 80C186XL, and the resulting 20 MHz master clock is buffered by U342. L472 allows the 40 MHz oscillator to be adjusted so that the 20 MHz master clock can be calibrated to the accuracy required by the System One measurement hardware. Each of the four buffers in U342 drives a separate module to eliminate interaction between the modules and maximize signal amplitude. Resistors R4302 and R4404 reduce ringing on the clock lines and provide a controlled rise time.

Microprocessor <1>

The control functions are provided by U371, an Intel 80C186XL 16-bit microprocessor operating at 20 MHz. It is similar to the 8086 microprocessor except that the clock generation, DMA, memory decoding, and peripheral decoding are included on chip. It also includes three onboard 16-bit counter timers. The 16-bit data bus is multiplexed with the lower 16 address lines from the microprocessor. These 16 bidirectional bus lines are labeled AD0 through AD15. Two 8-bit latches, U483 and U382, are used to de-multiplex the lower 16 address lines and U482 is used to latch A16 through A19, producing a 20-bit address bus.

The microprocessor executes a program loop which receives commands over RS232 or GPIB, parses them, programs the hardware appropriately, and returns readings from the hardware when requested.

Supply voltage sensor U271 resets the microprocessor U371 and the remaining hardware when the supply voltage drops below 4.75V. The sensor also has an active high open collector output which holds the chip select high during this time to prevent accidental writes to the EEPROMs when the microprocessor is going down.

Coprocessor <1>

The MFI-5 has support for an optional Intel 80C187 Math Coprocessor, U272, which can be used to improve floating-point execution time. The coprocessor interfaces directly with the 80C186XL, and is detected on powerup. Oscillator Y171 provides a 32 MHz clock source which is divided by two inside the 80C187, and used as its clock source.

Memory <2>

The MFI-5 accesses three different types of memory: RAM, ROM, and EEPROM. Memory accesses can be either byte-wide or word-wide, controlled by A0 and /BHE. The 80C186XL generates chip select outputs for specified memory ranges. Additional decoding is done by U372 to provide individual chip selects for each memory chip.

Two 128k x 8 static RAMs, U384 and U385, provide a total of 256k bytes of RAM. U372 uses /LCS, /BHE, and A0 to provide RAM chip selects. Two 128k x 8 ROMs, U386 and U391, provide a total of 256k byte of ROM for program storage. U372 uses /UCS, /BHE, and A0 to provide ROM chip selects. Four 32k x 8 EEPROMs, U172, U181, U182, and U191, provide 128k bytes of program storage for the DSP module in GPIB applications. U372 uses A19 through A16, A0, and /BHE to provide EEPROM chip selects, which are clamped to the supply during power cycles by diodes D2701, D2801, D2802, and D2901 and power supply sensor U271.

GPIB Direct Memory Access <1>

Both the 80C186XL microprocessor on the MFI-5 and TMS9914A GPIB Controller on the OMI-3 support Direct Memory Access (DMA), providing increased data throughput. DMA is first enabled by using /PCS2 to write a 1 to U171A, releasing U171B from reset. The DMA cycle is initiated by the TMS9914A by asserting /ACCRQ. This signal enters the MFI-5 through J141 pin 16, where it is inverted by U262F, and fed to the 80C186XL DMA Channel0 Request and also into the clock of U171B. The falling edge of /ACCRQ clocks the output of U171B high, which is fed into U362 where it is combined with /RD to invert DBIN, which is then fed back to the TMS9914A. After the DMA request is accepted by the 80C186XL, it drives a peripheral chip select line low to provide DMA Access Granted, /ACCGR, back to the TMS9914A. After the DMA transfer is completed, the 80C186XL will write a 0 to U171A to reset U171B, and return DBIN to its normal polarity.

Configuration Switches <3>

Tri-state buffer U111 and rocker switch S111 supply the bus address for GPIB applications or the baud rate selections for RS232 applications.

Short Interval Timer <3>

The timer information is obtained by the 8-bit counter U162. A 4 kHz signal is derived from one of the 80C186XL internal counter timers. The resulting resolution of the timer is 0.48 msec. The counter will rollover at 122.88 msec.

System One Interface Logic <3,4>

The data and address information from the APIB controller share the same 8-bit bus to the System One hardware. The interface also contains three strobe lines to indicate which type of information is carried on the bus at the time. These are described in the accompanying interface description. The bus timing is achieved by stretching all read and write operations of the host microprocessor bus to approximately 2.5 usec.

The Audio Precision Interface Bus connector is P211 at the right edge of the schematic. The four connectors for the cables to the modules are P421, P431, P432 and P441. Power supply connections enter through J351.

Wait State Generator <3>

A peripheral chip select signal from the 80C186XL drives U251 and U262E for the final address decoding, U351D where it enables the bus driver U121, and U362. The IORDY output from U362 is driven low by a read or write to any address occupied by the System One interface to cause the microprocessor to wait while the cycle is completed. The /STRTCNT output goes high at the same time IORDY goes low, and releases counter U343. The counter is clocked from the 20 MHz master clock, allowing repeatable timing of the wait states. At the end of the 2.5 usec interval the output of U343 will go high, driving IORDY high, and releasing the processor from the wait state. An earlier output from the counter (at 1.5 usec) is used to force the write strobe line (EW) on the System One interface to finish its pulse before the host processor is released from the wait state. This guarantees that the data to be latched into the System One is still valid when the strobe pulse reaches the end of the cable.

Bus Drive <3>

The decoder U251 decodes the write and read operations to drive the appropriate strobe lines on the System One interface. The selected output of U251 will go low to implement the appropriate function. The 1Y3 output is enabled for data writes, driving the interface line EW high via inverter U243F. The 1Y2 output goes low for address writes, driving the interface line EA high through U243G. The 1Y1 output is used to control the enabling of interrupts from the System One via U143B and to clear pending interrupts in U143A. The 1Y0 output drives the System One interface reset line through U243H, forcing ERST high, resetting all hardware modules.

The 2Y3 output of U251 goes low for data reads from the System One. This enables the output of the tri-state buffer U122 and places the data onto the microprocessor bus. This output also drives the line ER on the System One interface, causing devices in the System One to place their data on the interface. The 2Y2 output of U251 drives the 4-bit tri-state buffer U262. The buffer outputs drive the lower four bits of the multiplexed microprocessor bus, allowing reads of the three System One status lines and the state of flip-flop U143A which latches any occurrence of an interrupt.

Bus Receive <3,4>

All data going out of the host is buffered by octal bus transceiver U121. Eight capacitors, for example C3103, limit the rise time of the data edges to reduce EMI generation. Data being read from the System One is buffered by the transparent octal tranceiver U122. The eight RC networks, of which R221A/C3201 is typical, reduce noise picked up in the lines. Data entering the System One mainframe is filtered by the same networks and buffered by the octal bus transceiver U421. This data drives the address latch U221 and the four module connectors P421, P431, P432, and P441. The address information is latched and drives an additional eight lines on the module connectors. Data leaving the System One measurement hardware is buffered by octal buffer U411. Resistor network R211 pulls the bus lines high when they are tri-stated to prevent oscillations of the bus buffers when the lines assume voltages near TTL threshold.

When the APIB controller places address information on the bus it strobes the EA line high. This is filtered by R232 and C2306 to remove noise and buffered by inverter U243D. This produces a low going pulse which is used to strobe the address latch U221. This information is held until the next address write operation by the host.

When data is written from the APIB controller to the System One the EW line is pulled high. This is filtered by R232 and C2305 and buffered by inverter U243B. The output of this gate is the /SWR line which strobes low to write data into any module in the System One.

When data is read from the System One into the APIB controller the ER line is pulled high. This is filtered by R232 and C2304 and buffered by inverter U243C. The output of this gate is the /SRD line which strobes low to read data from any module in the System One. The /SRD line is combined with the /ATT line, to enable the output bus buffer U411, and also inverted by U342 and used to disable the input buffer U421. This prevents any bus contention by multiple buffers being active at one time. The /SRD line is individually distributed to each of the four modules using buffer U341.

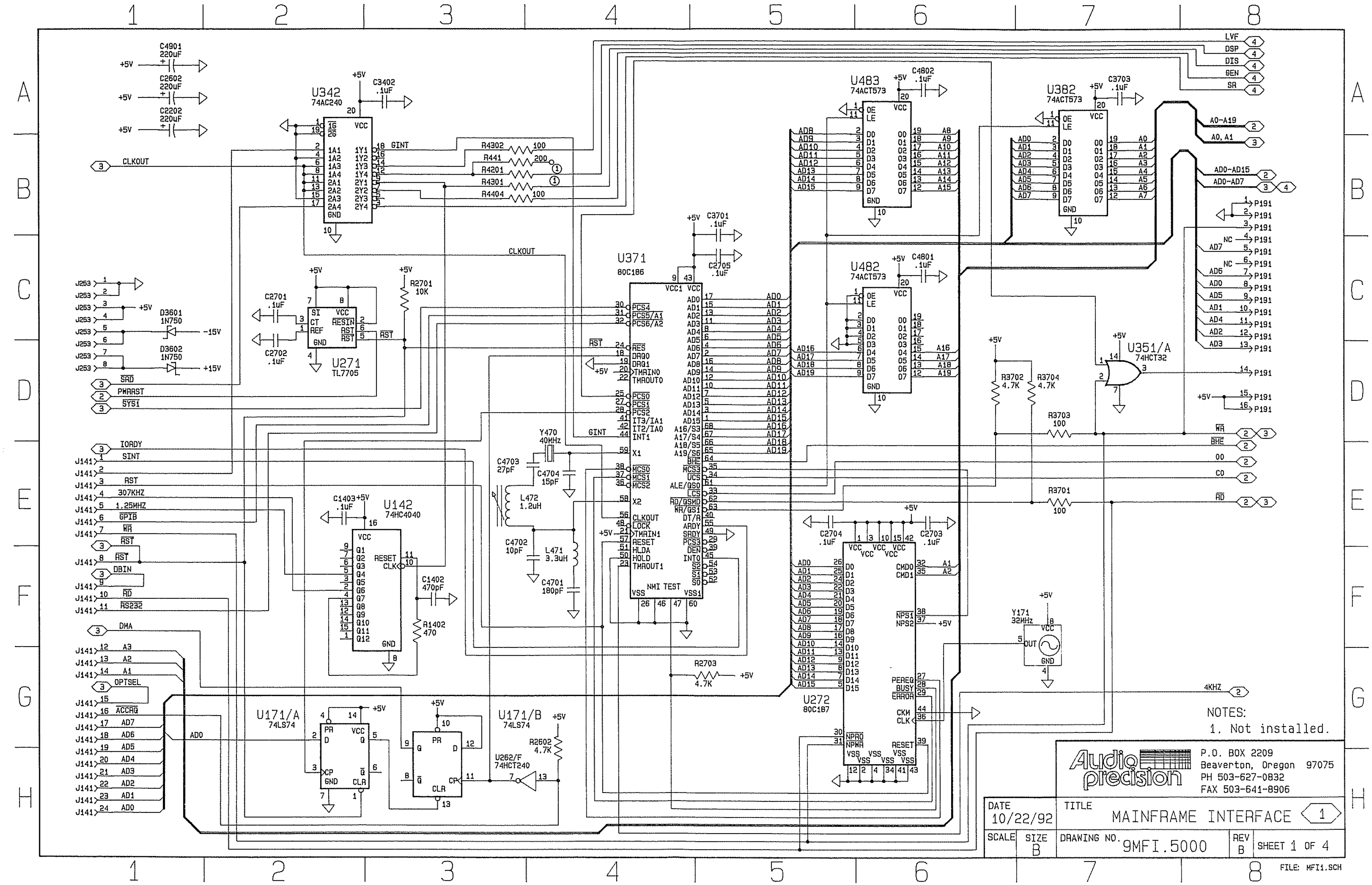
When any module in the System One mainframe senses its address on the address bus, it pulls the /ATT line low. This serves two purposes. This information is passed to the microcomputer on the /ATTOUT line so that the host may determine if a particular module is present. The output of U141A is open collector allowing the external bus to be wire ORed with other enclosures. The /ATT signal is also used to disable the read buffer U411 via U351C if there are no modules in the System One at that address. This allows multiple System One enclosures to be present on the external bus at the same time, if only one module at each address is used.

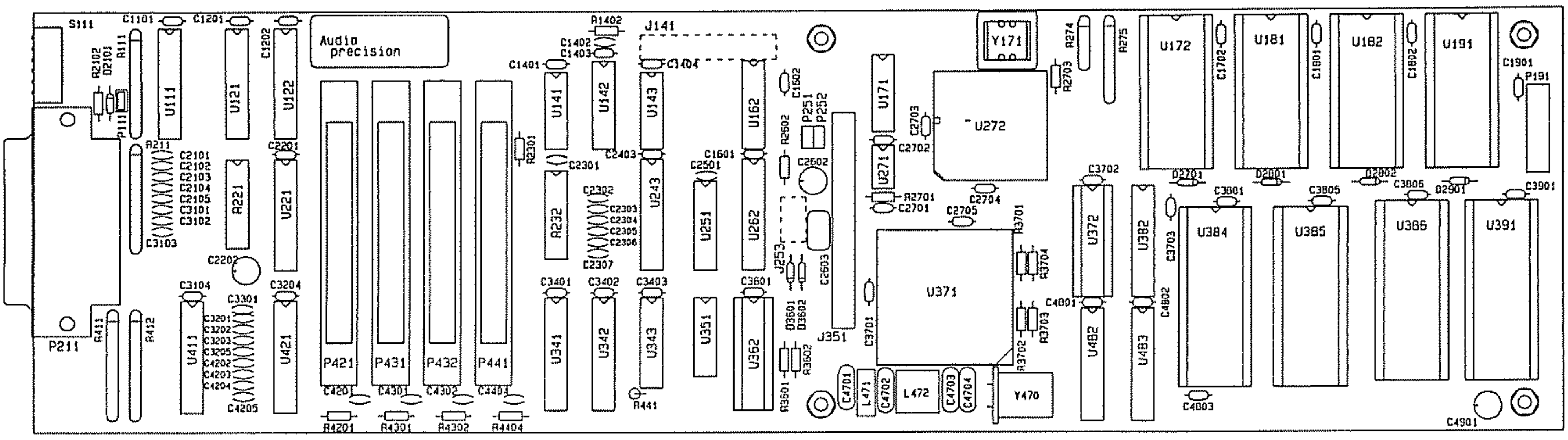
Reset Circuit <1,3>

Resetting of the measurement hardware can be initiated by either the host computer or by power cycling of the System One mainframe. The power-on reset is generated by the +5V supply voltage sensor IC U271. The reset signal from the host computer enters the System One via pin 16 of P211, the APIB connector. A high level on this line forces reset. Because of the pull up resistor R412, disconnecting the cable when the hardware is in the APIB mode will also cause a reset. This line is filtered to remove noise and buffered by U243A. U362 is used to combine these two reset signals, and provides /MRST to each of the modules.

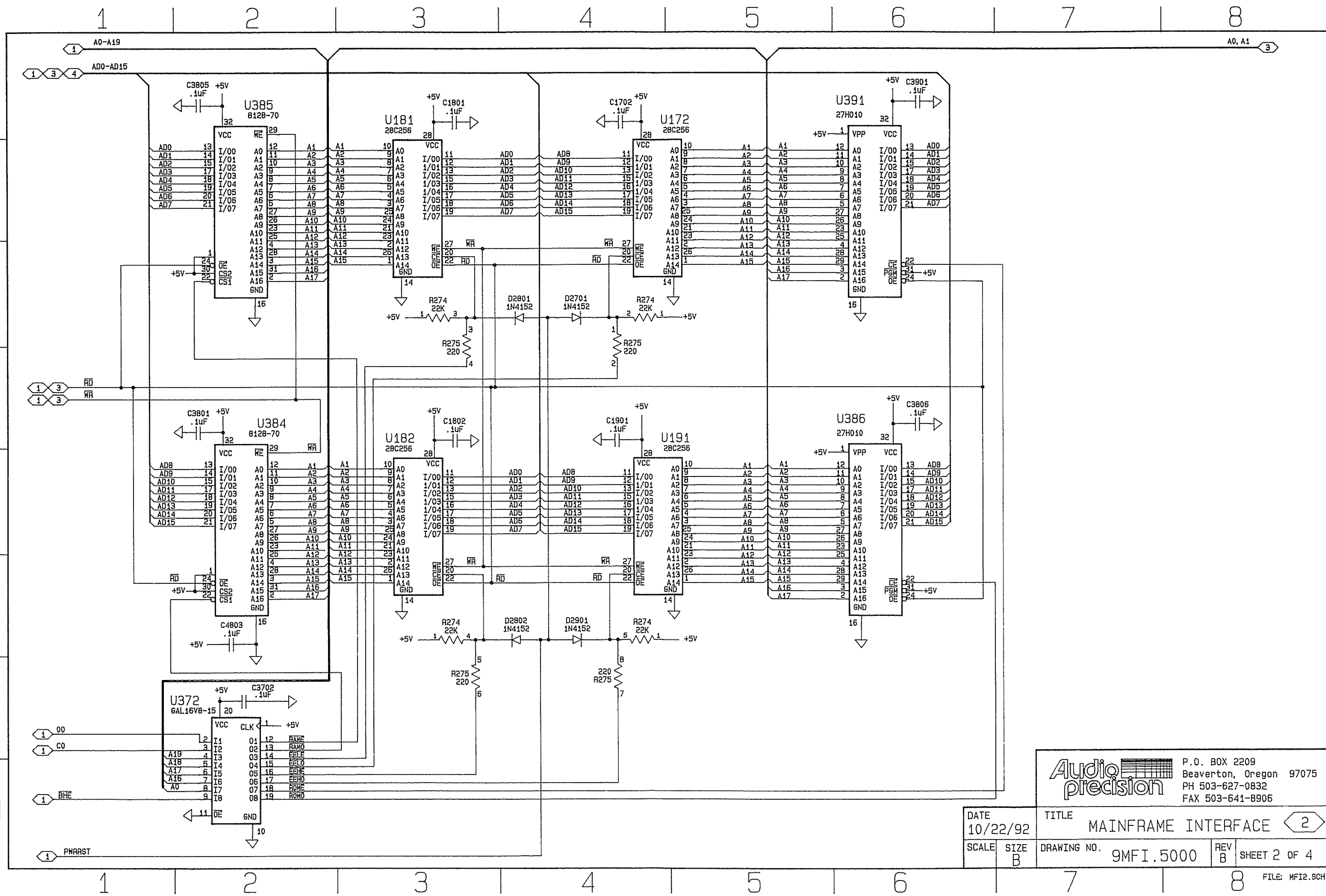
Miscellaneous Bus Operations

Diode D2101 is used to pull the PWR line low if the mainframe loses power. This may be sensed by the host to determine the failure. The /SIRQ line is a wired OR signal from the modules which is used to signal the host that service is necessary. It is buffered by U141D and drives the external bus in an open collector fashion. This allows the /EIRQ signal to be wire ORed among multiple System One enclosures. IRQ assertions which happen internally or on the external APIB bus are buffered by U262G and latched in U143A. The state of U143A is read by the microprocessor via tri-state buffer U262D. The /AUX signal is used by the dsp to signal that a new reading is ready.

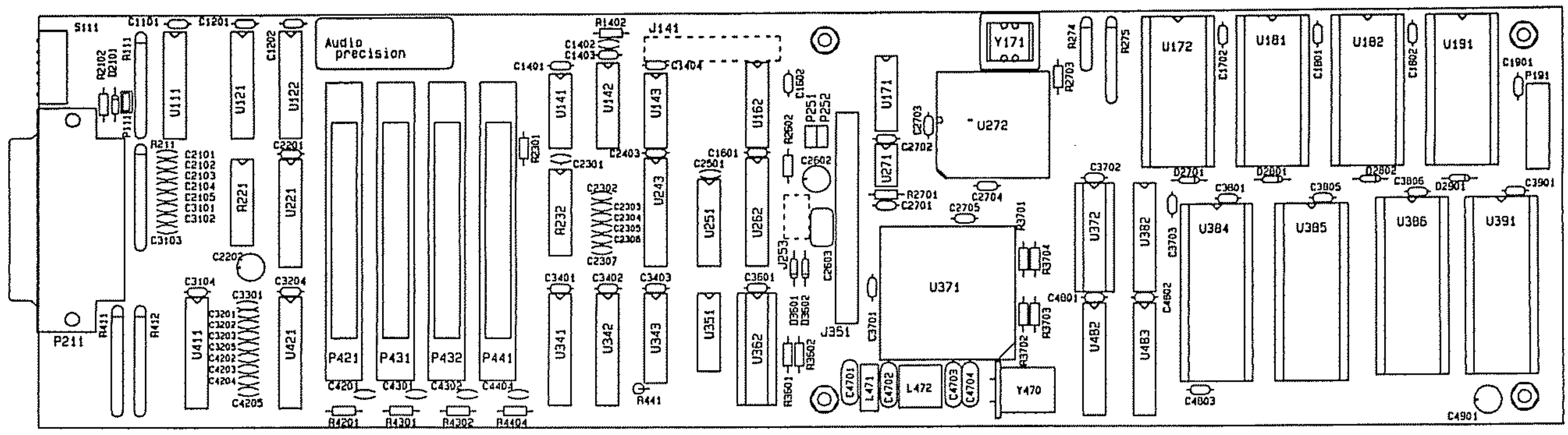

U342
74AC240
U271
TL7705
U142
74HC4040
U171/A
74LS74
U171/B
74LS74
U262/F
74HCT240
U371
80C186
U483
74ACT573
U482
74ACT573
U382
74ACT573
U351/A
74HCT32
U272
80C187
Y470
40MHz
Y171
32MHz
CLKOUT
A0-A19
AD0-AD15
AD0-AD7
LVF
DSP
DIS
GEN
SR
P191
4KHZ
NOTES:
1. Not installed.
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
10/22/92
TITLE
MAINFRAME INTERFACE
SCALE
SIZE
B
DRAWING NO.
9MFI.5000
REV
B
SHEET 1 OF 4
FILE: MFI1.SCH



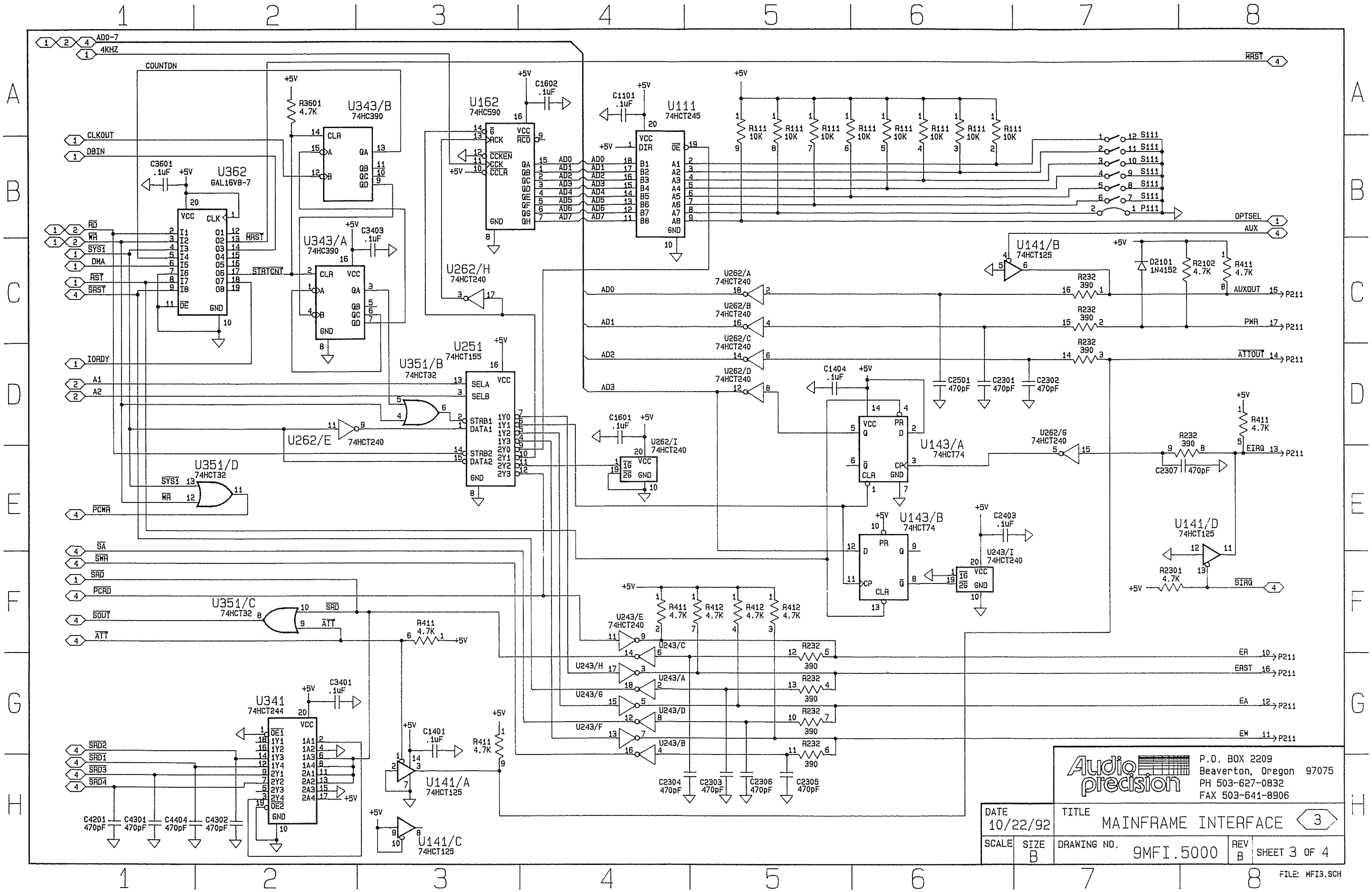
MAINFRAME INTERFACE 9MFI.5000 (6400.MFI5.1)

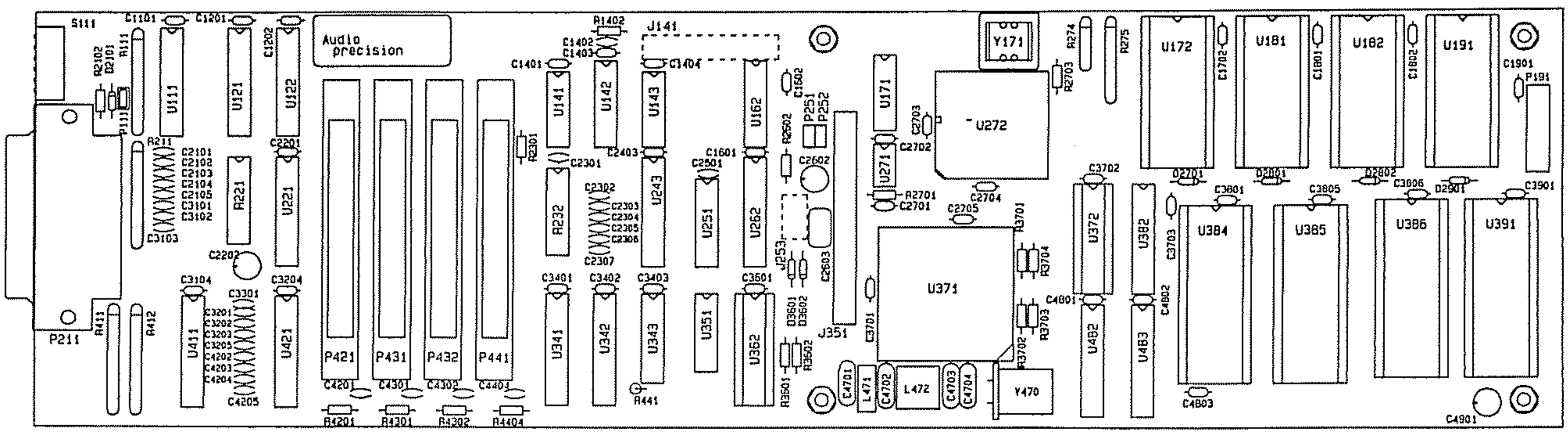


A0-A19
AD0-AD15
A0, A1
U385
8128-70
U384
8128-70
U181
28C256
U182
28C256
U172
28C256
U191
28C256
U391
27H010
U386
27H010
U372
GAL16V8-15
C3805 .1uF
C1801 .1uF
C1702 .1uF
C3901 .1uF
C3801 .1uF
C1802 .1uF
C1901 .1uF
C3806 .1uF
C4803 .1uF
C3702 .1uF
R274 22K
R275 220
D2801 1N4152
D2701 1N4152
D2802 1N4152
D2901 1N4152
RD
WR
00
C0
BHE
PWRRST
+5V
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 10/22/92
TITLE MAINFRAME INTERFACE
SCALE
SIZE B
DRAWING NO. 9MFI.5000
REV B
SHEET 2 OF 4
FILE: MFI2.SCH

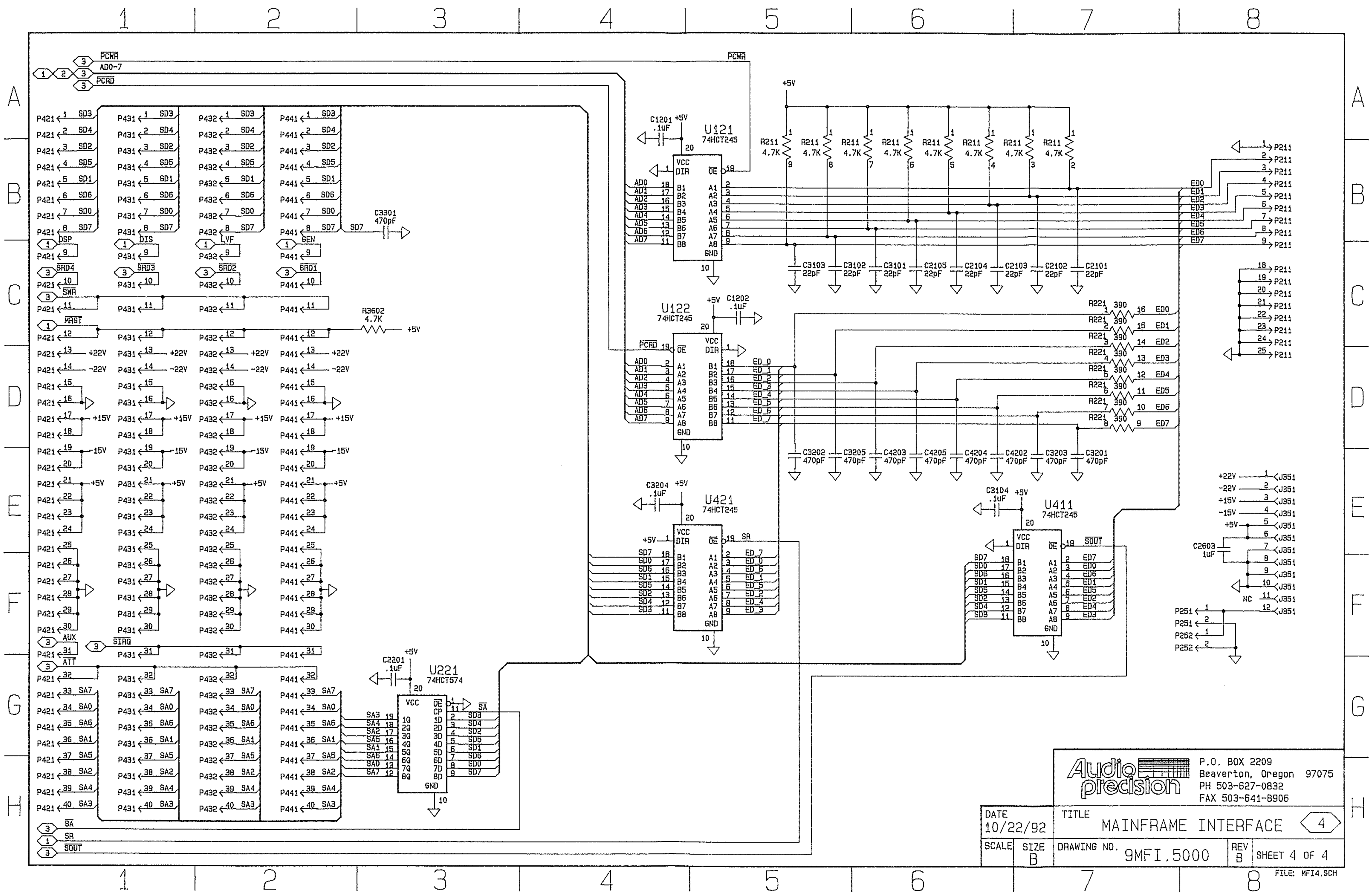


MAINFRAME INTERFACE 9MFI.5000 (6400.MFI5.1)


Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 10/22/92
TITLE MAINFRAME INTERFACE 3
SCALE
SIZE B
DRAWING NO. 9MFI.5000
REV B
SHEET 3 OF 4
FILE: MFI3.SCH



MAINFRAME INTERFACE 9MFI.5000 (6400.MFI5.1)



U121
74HCT245
U122
74HCT245
U421
74HCT245
U411
74HCT245
U221
74HCT574
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
10/22/92
TITLE
MAINFRAME INTERFACE
4
SCALE
SIZE
B
DRAWING NO.
9MFI.5000
REV
B
SHEET 4 OF 4
FILE: MFI4.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION					
C1101	3A4	2172.0104	CAP	CERAM	100V	20%	.1uF
C1201	4B4	2172.0104	CAP	CERAM	100V	20%	.1uF
C1202	4C5	2172.0104	CAP	CERAM	100V	20%	.1uF
C1401	3G3	2172.0104	CAP	CERAM	100V	20%	.1uF
C1402	1F3	2172.0471	CAP	CERAM	100V	20%	470pF
C1403	1E2	2172.0104	CAP	CERAM	100V	20%	.1uF
C1404	3D5	2172.0104	CAP	CERAM	100V	20%	.1uF
C1601	3E4	2172.0104	CAP	CERAM	100V	20%	.1uF
C1602	3A4	2172.0104	CAP	CERAM	100V	20%	.1uF
C1702	2B4	2172.0104	CAP	CERAM	100V	20%	.1uF
C1801	2A3	2172.0104	CAP	CERAM	100V	20%	.1uF
C1802	2E3	2172.0104	CAP	CERAM	100V	20%	.1uF
C1901	2E4	2172.0104	CAP	CERAM	100V	20%	.1uF
C2101	4C7	2172.0220	CAP	CERAM	100V	20%	22pF
C2102	4C7	2172.0220	CAP	CERAM	100V	20%	22pF
C2103	4C6	2172.0220	CAP	CERAM	100V	20%	22pF
C2104	4C6	2172.0220	CAP	CERAM	100V	20%	22pF
C2105	4C6	2172.0220	CAP	CERAM	100V	20%	22pF
C2201	4G3	2172.0104	CAP	CERAM	100V	20%	.1uF
C2202	1A1	2911.0227	CAP	EL-EL	10V		220uF
C2301	3D6	2172.0471	CAP	CERAM	100V	20%	470pF
C2302	3D7	2172.0471	CAP	CERAM	100V	20%	470pF
C2303	3H5	2172.0471	CAP	CERAM	100V	20%	470pF
C2304	3H4	2172.0471	CAP	CERAM	100V	20%	470pF
C2305	3H5	2172.0471	CAP	CERAM	100V	20%	470pF
C2306	3H5	2172.0471	CAP	CERAM	100V	20%	470pF
C2307	3E7	2172.0471	CAP	CERAM	100V	20%	470pF
C2403	3E7	2172.0104	CAP	CERAM	100V	20%	.1uF
C2501	3D6	2172.0471	CAP	CERAM	100V	20%	470pF
C2602	1A1	2911.0227	CAP	AL-EL10V			220uF
C2603	4F8	2454.0105	CAP	POLYE	50V	5%	1uF
C2701	1C2	2172.0104	CAP	CERAM	100V	20%	.1uF
C2702	1D2	2172.0104	CAP	CERAM	100V	20%	.1uF
C2703	1E6	2172.0104	CAP	CERAM	100V	20%	.1uF
C2704	1E5	2172.0104	CAP	CERAM	100V	20%	.1uF
C2705	1C5	2172.0104	CAP	CERAM	100V	20%	.1uF
C3101	4C6	2172.0220	CAP	CERAM	100V	20%	22pF
C3102	4C5	2172.0220	CAP	CERAM	100V	20%	22pF
C3103	4C5	2172.0220	CAP	CERAM	100V	20%	22pF
C3104	4E6	2172.0104	CAP	CERAM	100V	20%	.1uF
C3201	4E7	2172.0471	CAP	CERAM	100V	20%	470pF
C3202	4E5	2172.0471	CAP	CERAM	100V	20%	470pF
C3203	4E7	2172.0471	CAP	CERAM	100V	20%	470pF
C3204	4E4	2172.0104	CAP	CERAM	100V	20%	.1uF
C3205	4E	2172.0471	CAP	CERAM	100V	20%	470pF
C3301	4C3	2172.0471	CAP	CERAM	100V	20%	470pF
C3401	3G2	2172.0104	CAP	CERAM	100V	20%	.1uF
C3402	1A3	2172.0104	CAP	CERAM	100V	20%	.1uF
C3403	3C2	2172.0104	CAP	CERAM	100V	20%	.1uF
C3601	3B1	2172.0104	CAP	CERAM	100V	20%	.1uF
C3701	1C5	2172.0104	CAP	CERAM	100V	20%	.1uF
C3702	2G2	2172.0104	CAP	CERAM	100V	20%	.1uF

REPLACEABLE ELECTRICAL PARTS LIST: 9MFI.5000

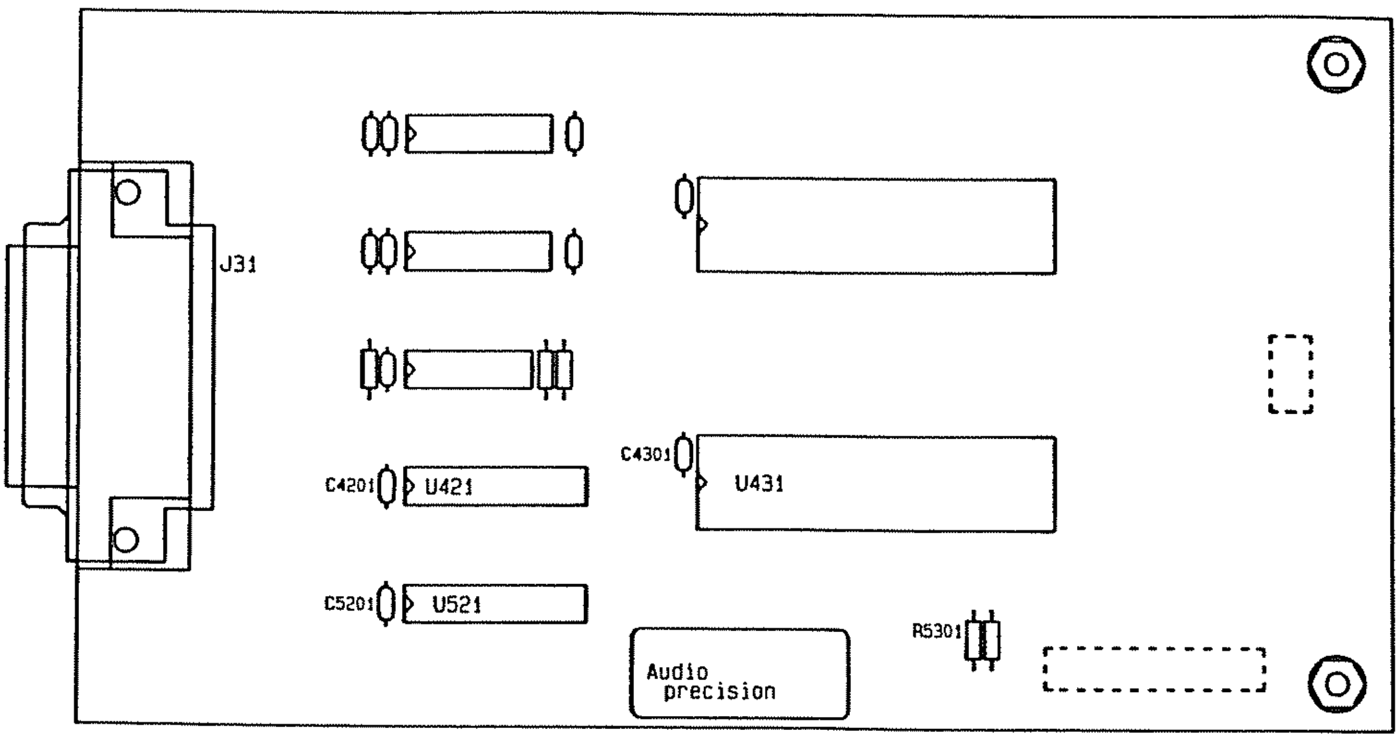
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C3703	1A7	2172.0104	CAP CERAM 100V 20%	.1uF
C3801	2D2	2172.0104	CAP CERAM 100V 20%	.1uF
C3805	2A2	2172.0104	CAP CERAM 100V 20%	.1uF
C3806	2D6	2172.0104	CAP CERAM 100V 20%	.1uF
C3901	2A6	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	3H1	2172.0471	CAP CERAM 100V 20%	470pF
C4202	4E6	2172.0471	CAP CERAM 100V 20%	470pF
C4203	4E6	2172.0471	CAP CERAM 100V 20%	470pF
C4204	4E6	2172.0471	CAP CERAM 100V 20%	470pF
C4205	4E6	2172.0471	CAP CERAM 100V 20%	470pF
C4301	3H1	2172.0471	CAP CERAM 100V 20%	470pF
C4302	3H4	2172.0471	CAP CERAM 100V 20%	470pF
C4404	3H1	2172.0471	CAP CERAM 100V 20%	470pF
C4701	1F4	2296.0181	CAP MICA 500V 1%	180pF
C4702	1F4	2294.0100	CAP MICA 500V 5%	10pF
C4703	1E3	2294.0270	CAP MICA 500V 5%	27pF
C4704	1E4	2294.0150	CAP MICA 500V 5%	15pF
C4801	1C5	2172.0104	CAP CERAM 100V 20%	.1uF
C4802	1A6	2172.0104	CAP CERAM 100V 20%	.1uF
C4803	2F2	2172.0104	CAP CERAM 100V 20%	.1uF
C4901	1A1	2911.0227	CAP AL-El 10V	220uF
D2101	3C7	3110.4152	DIODE SIGNAL	4152
D2701	2C4	3110.4152	DIODE SIGNAL	4152
D2801	2C4	3110.4152	DIODE SIGNAL	4152
D2802	2F4	3110.4152	DIODE SIGNAL	4152
D2901	2F4	3110.4152	DIODE SIGNAL	4152
D3601	1C1	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D3602	1D1	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
J141	1E1-1H1	4221.1024	JACK PC 2 X .1	24 PIN
J253	1C1,1D1	4221.1008	JACK PC 2 X .1	8 PIN
J351	4E8,4F8	4152.0012	CABLE ASSY .156 18Ga	12 COND
L471	1F4	4510.0339	INDUCOR	3.3uH
L472	1E4	4440.0129	COIL UNEABLE RF	1.2uH
P111	---	4221.0036	PLUG PC .1 X.43	36 PIN
P191	1B8-1D8	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P211	3C8-3G8,4B8,4C8	4225.0125	PLUG D-SUB PC 90'	25 PIN
P251	4F8	4221.0036	PLUG PC .1 X.43	36 PIN
P252	4F8	4221.0036	PLUG PC .1 X.43	36 PIN
P421	4A1-4H1	4221.0040	PLUG PC W/EJEC 2X.1	40 PIN
P431	4A1-4H1	4221.0040	PLUG PC W/EJEC 2X.1	40 PIN
P432	4A1-4H1	4221.0040	PLUG PC W/EJEC 2X.1	40 PIN
P441	4A1-4H1	4221.0040	PLUG PC W/EJEC 2X.1	40 PIN
R111	3B5,3B6	1984.9103	RES NE SIP 5% B	9 X 10K
R1402	1G3	1214.0471	RES 1/4W C FLM 5%	470
R2102	3C8	1214.0472	RES 1/4W C FLM 5%	4.7K
R211	4B5-4B7	1984.9472	RES NE SIP 5% B	9 X 4.7K
R221	4C7,4D7	1994.8391	RES NE DIP 5%	8 X 390
R2301	3F7	1214.0472	RES 1/4W C FLM 5%	4.7K
R232	3C7,3D7,3F5,3G5	1994.8391	RES NE DIP 5%	8 X 390
R2602	1H4	1214.0472	RES 1/4W C FLM 5%	4.7K
R2701	1C3	1214.0103	RES 1/4W C FLM 5%	10K
R2703	1G5	1214.0472	RES 1/4W C FLM 5%	4.7K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION
R274	2C3, 2C4, 2F3, 2F4	1985.4223	RES NE SIP 2% B 4 X 22K
R275	2D3,2D4,2G3,2G4	1984.4221	RES NE SIP 5% I 4 X 220
R3601	3A2	1214.0472	RES 1/4W C FLM 5% 4.7K
R3602	4C3	1214.0472	RES 1/4W C FLM 5% 4.7K
R3701	1E7	1214.0101	RES 1/4W C FLM 5% 100
R3702	1D6	1214.0472	RES 1/4W C FLM 5% 4.7K
R3703	1D7	1214.0101	RES 1/4W C FLM 5% 100
R3704	1D7	1214.0472	RES 1/4W C FLM 5% 4.7K
R411	3C8,3D8,3G3,3F4	1984.9472	RES NE SIP 5% B 9 X 4.7K
R412	3F5	1984.9472	RES NE SIP 5% B 9 X 4.7K
R4201	1B3	1214.0000	JUMPER .4 X.25 00
R4301	1B3	1214.0000	JUMPER .4 X.25 00
R4302	1B3	1214.0101	RES 1/4W C FLM 5% 100
R4404	1B3	1214.0101	RES 1/4W C FLM 5% 100
R441	1B3	1214.0201.1	RES 1/4W C FLM 5% VER 200
S111	3B7	4311.0006	SWI CH DIP 90' 6 POLE
U111	3A4	3324.0245	RANSCVR 8X RI-S 74HC245
U121	4B4	3324.0245	RANSCVR 8X RI-S 74HC245
U122	4C4	3324.0245	RANSCVR 8X RI-S 74HC245
U141	3C6, 3E7, 3H3	3324.0125	BUFFER 4X RI-S 74HC125
U142	1E3	3323.4040	COUNER 12-SAGE 74HC4040
U143	3D6, 3E6	3324.0074	FLIP-FLOP 2X D 74HC74
U162	3A3	3323.0590	COUNER 8-BI RI-S 74HC590
U171	1G2,1G3	3313.0074	FLIP-FLOP 2X D 74LS74
U172	2A5	3724.28256	EEPROM CMOS 200ns 32K X 8
U181	2A3	3724.28256	EEPROM CMOS 200ns 32K X 8
U182	2E3	3724.28256	EEPROM CMOS 200ns 32K X 8
U191	2E5	3724.28256	EEPROM CMOS 200ns 32K X 8
U221	4G3	3324.0574	FLIP-FLOP 8X D RI-S 74HC574
U243	3F4,3F6,3G4	3324.0240	BUFFER 8X INV RI-S 74HC240
U251	3D3	3324.0155	DECODER 2 X 2-LN/4-LN 74HC155
U262	3C3,3C5,3D5, 3E2,3E4,3E6,3H3	3324.0240	BUFFER 8X INV RI-S 74HC240
U271	1D2	3450.7705	SUPPLY VOL SENSOR 5V
U341	3G2	3324.0244	BUFFER 8X RI-SAE 74HC244
U342	1A2	3325.0240	BUFFER 8X INV RI-S 74AC240
U343	3A2, 3C2	3323.0390	COUNER 2 X 4-BI DEC 74HC390
U351	1D7,3D3,3E2,3F2	3324.0032	GA E 4 X 2-IN OR 74HC32
U362	3B2	3342.16V8.M3	GEN.ARRAY GAL16V8-7 MFI5 U362
U371	1C4	3331.0186	uPROCESSOR CMOS 20MHz 80C186
U372	2G2	3342.16V8.M3	GEN.ARRAY GAL16V8-7 MFI5 U362
U382	1A7	3326.0573	LA CH 8X RI-S 74AC573
U384	2E2	3722.8128.1	SRAM CMOS 70ns 128K X 8
U385	2A2	3722.8128.1	SRAM CMOS 70ns 128K X 8
U386	2E6	3723.2710.1	EPROM CMOS 80ns 128K X 8
U391	2A6	3723.2710.1	EPROM CMOS 80ns 128K X 8
U411	4E7	3324.0245	RANSCVR 8X RI-S 74HC245
U421	4E4	3324.0245	RANSCVR 8X RI-S 74HC245
U482	1C6	3326.0573	LA CH 8X RI-S 74AC573
U483	1A6	3326.0573	LA CH 8X RI-S 74AC573
Y470	1E4	3900.0040	CRYSAL 40MHz

OMI-3

DIGITAL INTERFACE OPTION

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C3201	3E6	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	3D7	2172.0104	CAP CERAM 100V 20%	.1uF
C4301	3D7	2172.0104	CAP CERAM 100V 20%	.1uF
C5201	3C7	2172.0104	CAP CERAM 100V 20%	.1uF
J31	3C-G8	4225.0024	JACK IEEE-488 W/SHELL	24 PIN
P34	3G4	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P53	3C-G3	4221.0072	PLUG PC 2X.1 X.43	72 PIN
R3202	3D5	1214.0472	RES 1/4W C FLM 5%	4.7K
R3203	3E5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5301	3F4	1214.0472	RES 1/4W C FLM 5%	4.7K
R5302		1214.0000	JUMPER .4 X.25	00
U321	3E6	3324.0125	BUFFER 4X TRI-ST	74HCT125
U421	3E6	3333.0161	GPIB TRANSCEIVER	75ALS161
U431	3D4	3332.9914	GPIB CONTROLLER	TMS9914A
U521	3C6	3333.0160	GPIB TRANSCEIVER	75ALS160



9OMI.300G FOR G-VERSION CONFIGURATIONS (6200.OMI1.1)

OMI-3, MAINFRAME INTERFACE ASSEMBLY

Introduction

The OMI-3 board is present only in "G" or "S" system versions. It mounts to the MFI-3, MFI-4, or MFI-5 mainframe interface board and contains the hardware and rear panel connector specific to the GPIB or RS232 digital interfaces.

G-Version OMI-3

GPIB interface communications are handled by U431. This integrated circuit performs bus protocol operations. A 1.25 MHz master clock for its operation is provided by counter U471 which divides the 20 MHz system clock by approximately 16. Resistor R3705 and capacitor C3701 alter this division ratio slightly from 16 to allow derivation of the 307 kHz clock required for RS232 operation.

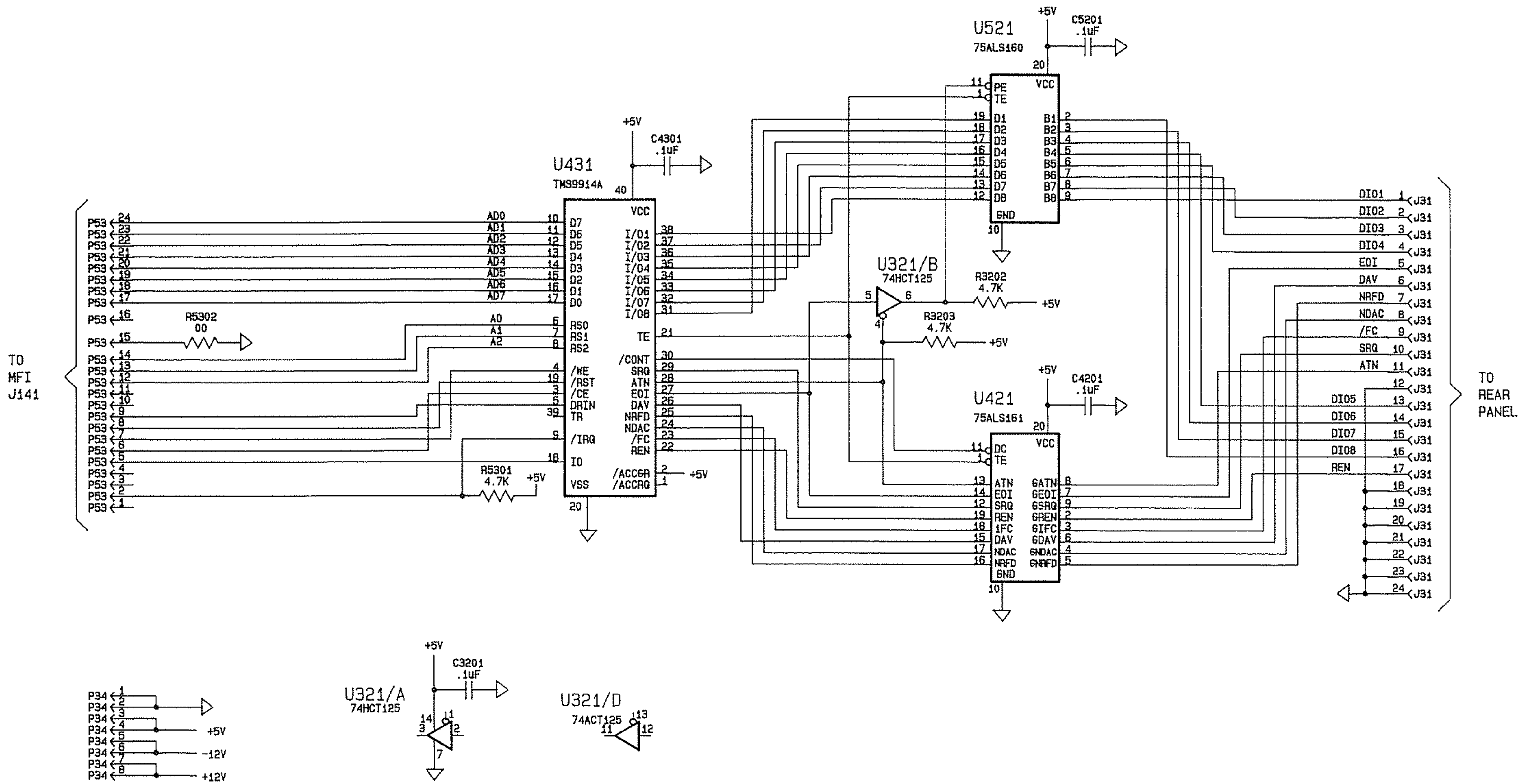
GPIB data bus buffering functions are provided by octal line transceiver U421. Control line buffering and drive functions are provided by octal line transceiver U521.

S-Version OMI-3

RS232 interface communications are handled by UART U231. This integrated circuit performs framing, serial to parallel conversion, and parity functions. A 307 kHz master clock for its operation is provided by counter U471 which divides the 20 MHz system clock. Resistor R3705 and capacitor C3701 alter this division ratio from a binary value by resetting the counter every 128 clock cycles.

Voltage level shifting and line buffering functions are provided by U121 and U221. The devices marked "Tx" are line drivers and shift the 5V logic levels of the UART to ±12V RS232 levels. The devices marked "Rx" are line receivers and shift the ±12V RS232 levels to the 5V logic levels of the UART.

ECO#	SHEET#	DATE	APPROVAL



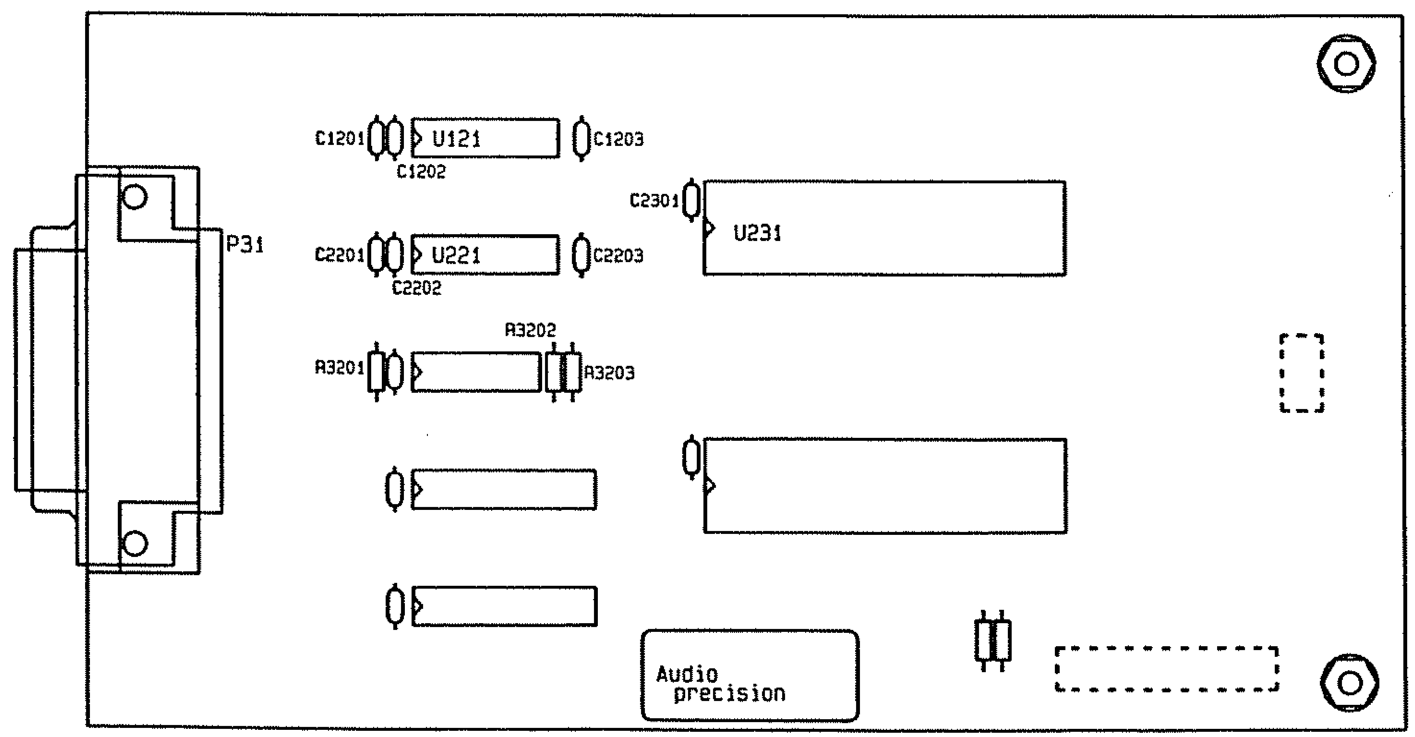
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE		
9/4/92	GPIB INTERFACE OPTION		
SCALE / SIZE B	DRAWING NO. 90MI.300G	REV 1	SHEET 1 OF 1

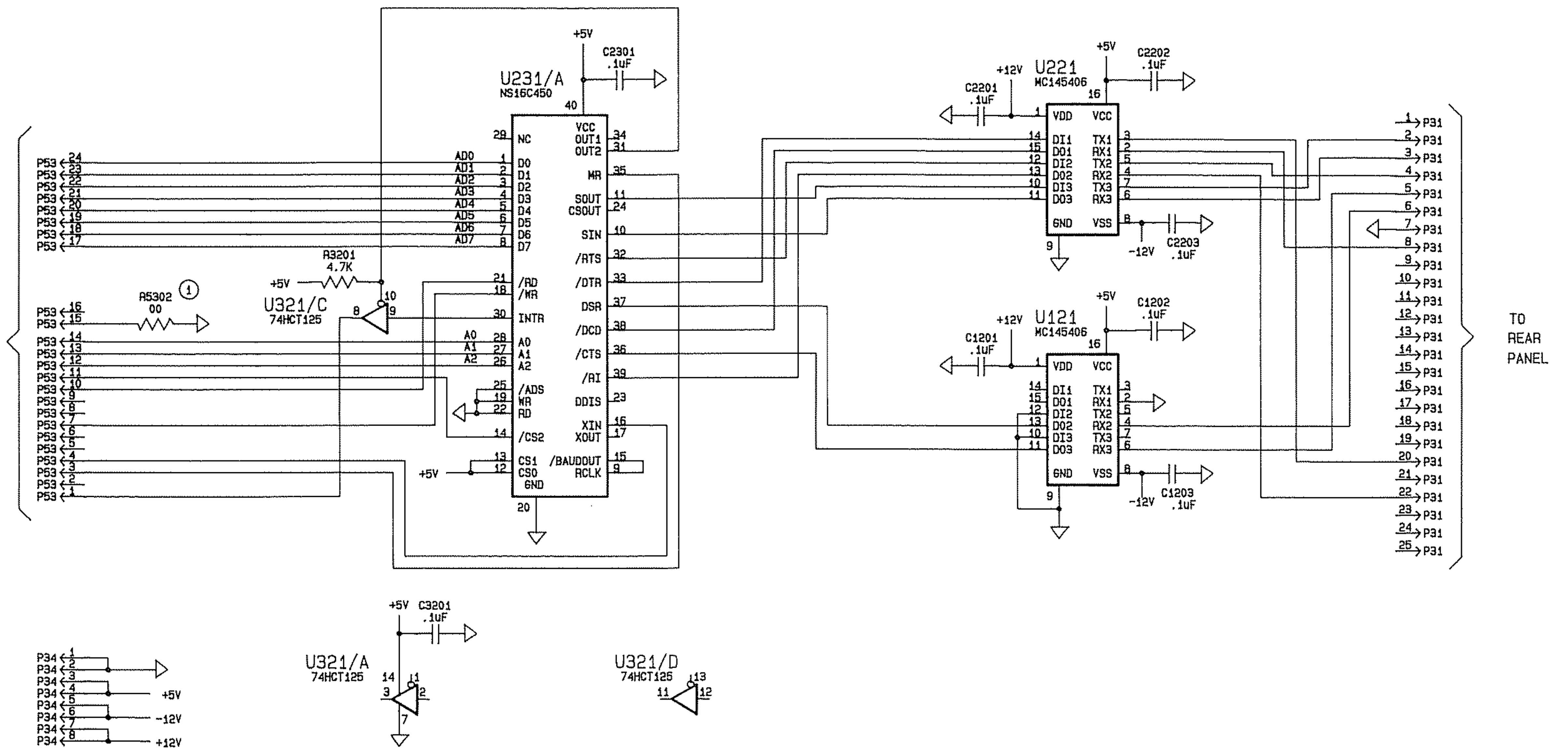
FILE: 0MI300G.SCH

Replaceable Electrical Parts List: 9OMI.300S

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
.C1201	4E6	2172.0104	CAP CERAM 100V 20%	.1uF
C1202	4D6	2172.0104	CAP CERAM 100V 20%	.1uF
C1203	4E6	2172.0104	CAP CERAM 100V 20%	.1uF
C2201	4C6	2172.0104	CAP CERAM 100V 20%	.1uF
C2202	4C6	2172.0104	CAP CERAM 100V 20%	.1uF
C2203	4C6	2172.0104	CAP CERAM 100V 20%	.1uF
C2301	4C5	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	4G4	2172.0104	CAP CERAM 100V 20%	.1uF
P31	4C-F8	4225.0125	PLUG D-SUB PC 90'	25 PIN
P34	4G4	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P53	4C-G3	4221.0072	PLUG PC 2X.1 X.43	72 PIN
R3201	4F4	1214.0472	RES 1/4W C FLM 5%	4.7K
R5302	4G4	1214.0000	JUMPER .4 X.25	00
U121	4C7,4D6,4D7,4E7	3333.5406	RS232 DRIVER/RCVR	MC145406
U221	4C6,4E6,4F7	3333.5406	RS232 DRIVER/RCVR	MC145406
U231	4D1	3332.16450	ASYNCH COMM ELEMENT	NS16450
U321	4F4	3324.0125	BUFFER 4X TRI-ST	74HCT125



9OMI.300S FOR S-VERSION CONFIGURATIONS (6200.OMI1.1)



NOTES:

1. NOT INSTALLED

ECO#	SHEET#	DATE	APPROVAL

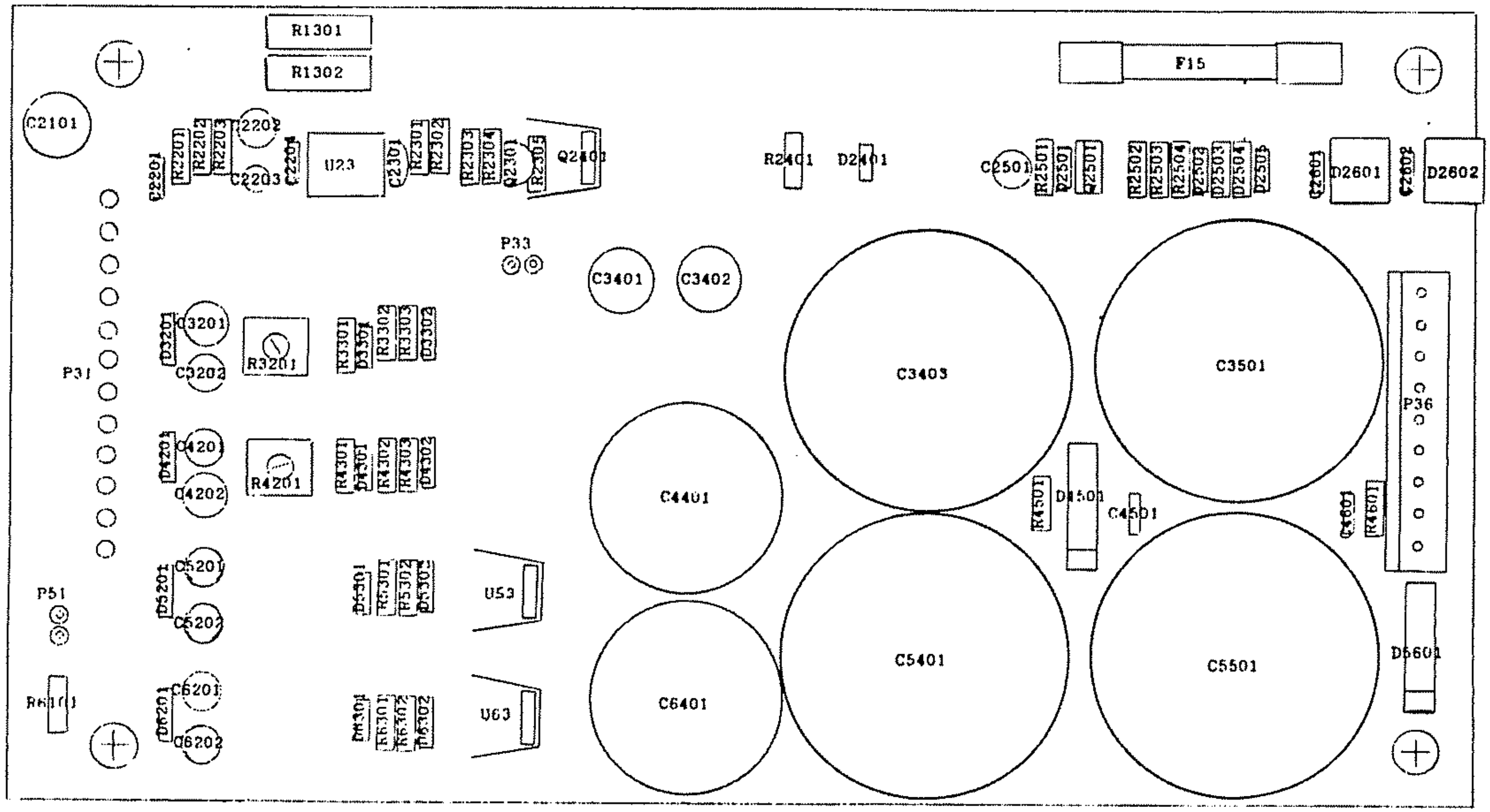
Audio precision

P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 9/3/92	TITLE RS232 INTERFACE SERIAL OPTION		
SCALE	SIZE B	DRAWING NO. 90MI.300S	REV 1	SHEET 1 OF 1

FILE: OMI300S.SCH

PSA-1 POWER SUPPLY



POWER SUPPLY (9PSA.1000)

PSA-1, POWER SUPPLY MODULE

NOTE: There have been two versions of the power supply module. The PSA-1 version contains 3 heatsinks while the PSA-2 version contains 5 heatsinks. The PSA-2 must be installed in any DSP configuration system.

Introduction

The PSA-1 power supply module provides five regulated voltages (+5V, +15V, -15V, +22V, and -22V), plus an unregulated supply for the cooling fan. A power line sync signal and power fail reset drive signal are also provided.

+5V Supply

A center tapped transformer winding is full wave rectified by D2601 and D2602 and filtered by C3501 and C5501 to provide a 8-12 V raw dc supply. This is fed through fuse F17 into the main pass device Q2401 which forms part of a complementary darlington with Q2402. The emitter of the darlington drives the output through the current sense resistors R1301 and R1302. The output voltage is sensed by U23A via R2201 and is compared to a +5V reference developed by R2202 and R2203 from the +15V supply. Since U23 is an open collector output device it is pulled up by R2304. This voltage is buffered by emitter follower Q2301 and used to drive the darlington output pair. C2203 provides dominant pole compensation of U23A and C2301 continues this compensation when the equivalent series resistance (ESR) of C2203 prevents continued rolloff.

Current limiting occurs at about 8.0 A and is provided by sensing the voltage drop across the sense resistors R1301 and R1302. This drop is offset 400 mV negative by R2301 and R2301 to be less than +5 V until current limit is reached. U23B compares this voltage to the +5V supply output and will swing negative when the voltage on the sense resistors exceeds 400 mV. Since the output is open collector this will cause the reference voltage seen by U23A to go to ground, shutting down the supply. D2501 senses the output voltage and will fire the SCR crowbar Q2501 whenever the output voltage exceeds approximately +5.6 V. This blows the fuse F17 and protects the logic circuits from overvoltage in the event of a catastrophic failure in the regulator circuit.

±15V Supplies

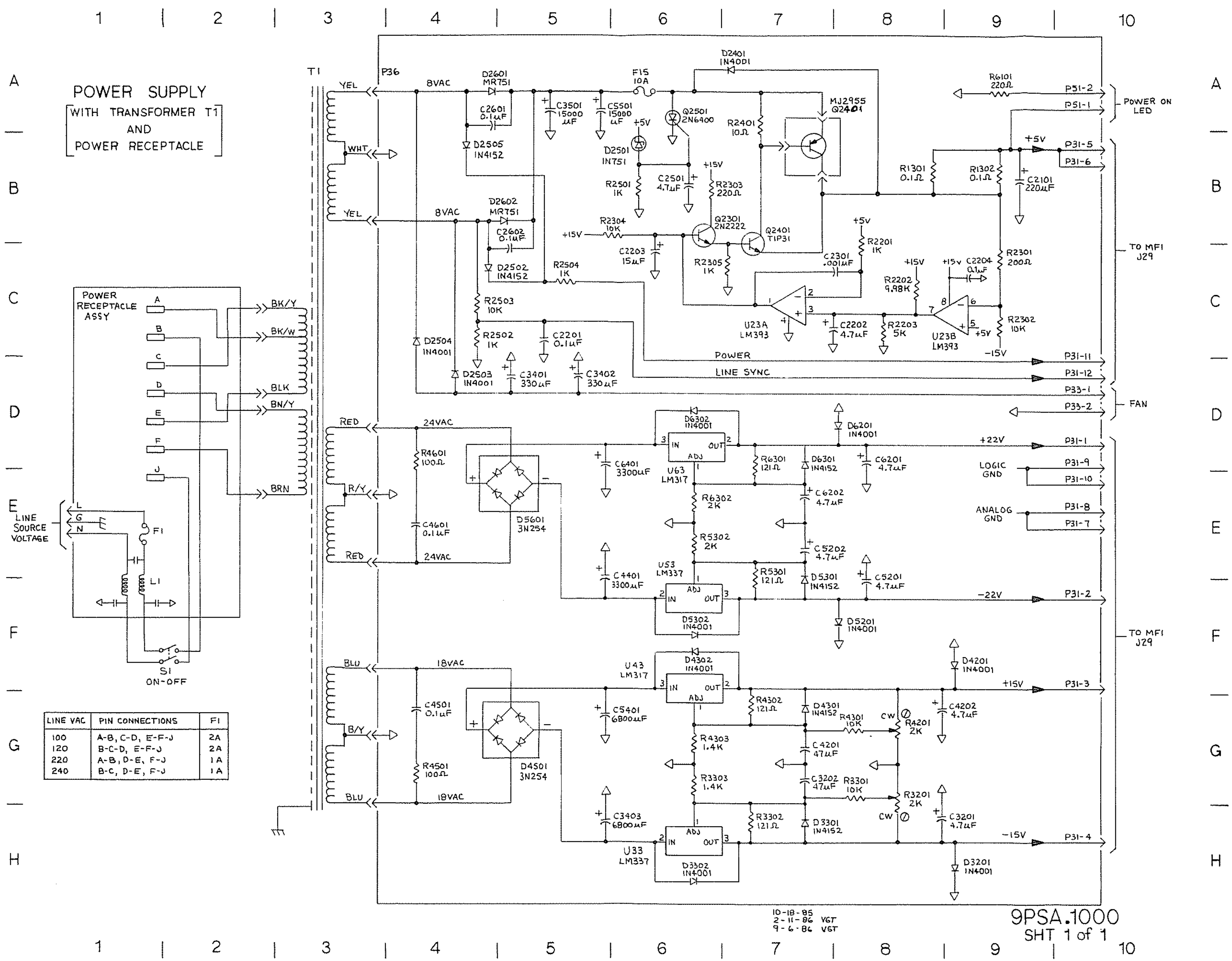
A center tapped transformer winding drives a pair of full wave rectifiers formed by D4501. Filtering is provided by C5401 and C3401. The raw voltage is regulated by three terminal adjustable regulators U43 and U33. Resistor dividers R4302/R4303 and R3302/R3303 scale the output voltages to +15V and -15V respectively. Potentiometers R4201 and R3201 and resistors R4301 and R3301 adjust the divider ratios to compensate for tolerances of the regulators and allow accurate supply voltages. C4202 and C3202 provide filtering to eliminate noise generated internal to the regulators. C4201 and C3202 reduce the output impedance at high frequencies. D4201 and D3201 protect against reverse voltage on the regulator outputs. D4301 D4302, D3301 and D3302 provide capacitor discharge paths during power down or supply fault conditions.

±22V Supplies

A center tapped transformer winding drives a pair of full wave rectifiers formed by D5601. Filtering is provided by C4401 and C6401. The raw voltage is regulated by three terminal adjustable regulators U63 and U53. Resistor dividers R6301/R6302 and R5301/R5302 scale the output voltages to +22V and -22V respectively. C6202 and C5202 provide filtering to eliminate noise generated internal to the regulators. C6201 and C5201 reduce the output impedance at high frequencies. D6201 and D5201 protect against reverse voltage on the regulator outputs. D6301 D6302, D5301 and D5302 provide discharge paths for the capacitors during power down or supply fault conditions.

Fan Supply & Power Down Signal

D2504 and D2503 full wave rectify ac power from the same winding that provides the +5V supply. The rectified voltage is filtered by C3401 and C3402 to produce an approximately -12V unregulated supply. Diodes D2502 and D2505 provide a sense signal for the reset circuits located on the mainframe interface circuit board. Resistor R2504 protects against short circuits destroying the diodes. Line sync is provided by tapping one side of the ac signal from this same winding.



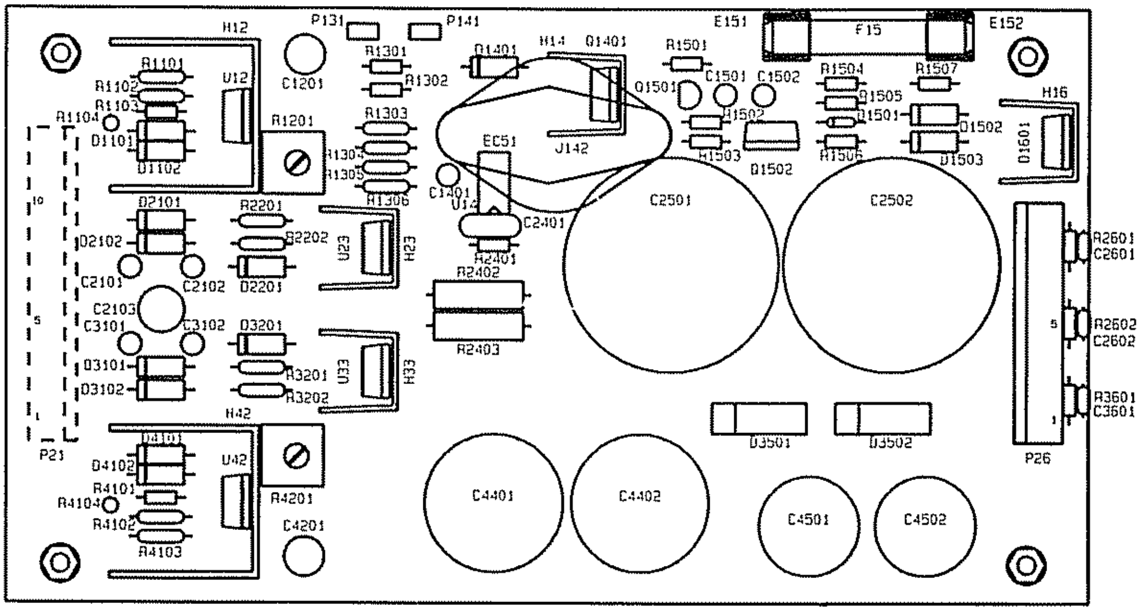
LINE VAC	PIN CONNECTIONS	F1
100	A-B, C-D, E-F-J	2A
120	B-C-D, E-F-J	2A
220	A-B, D-E, F-J	1A
240	B-C, D-E, F-J	1A

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C2101	1B9	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2201	1C5	2172.0104	CAP CERAM 100V 20%	.1uF
C2202	1C8	2942.0475	CAP AL-EL 35V 20%	4.7uF
C2203	1C6	2832.0156	CAP TA-EL 25V 20%	15uF
C2204	1C10	2172.0104	CAP CERAM 100V 20%	.1uF
C2301	1C8	2172.0102	CAP CERAM 100V 20%	.001uF
C2501	1B6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C2601	1A4	2172.0104	CAP CERAM 100V 20%	.1uF
C2602	1C5	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	1H9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3202	1G7	2932.0476	CAP AL-EL 25V 20%	47uF
C3401	1D5	2932.0337	CAP AL-EL 25V 20%	330uF
C3402	1D5	2932.0337	CAP AL-EL 25V 20%	330uF
C3403	1H5	2941.0688	CAP AL-EL 35V +80/-20%	6800uF
C3501	1A5	2921.0159	CAP AL-EL 16V +80/-20%	15mF
C4201	1G7	2932.0476	CAP AL-EL 25V 20%	47uF
C4202	1G9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4401	1E5	2941.0338	CAP AL-EL 35V +80/-20%	3300uF
C4501	1G4	2172.0104	CAP CERAM 100V 20%	.1uF
C4601	1E4	2172.0104	CAP CERAM 100V 20%	.1uF
C5201	1F8	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5202	1E7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5401	1G5	2941.0688	CAP AL-EL 35V +80/-20%	6800uF
C5501	1A5	2921.0159	CAP AL-EL 16V +80/-20%	15mF
C6201	1D8	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6202	1E7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6401	1D5	2941.0338	CAP AL-EL 35V +80/-20%	3300uF
D2401	1A7	3111.4001	DIODE POWER 1A 50V	1N4001
D2501	1B6	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D2502	1C4	3110.4152	DIODE SIGNAL	1N4152
D2503	1D4	3111.4001	DIODE POWER 1A 50V	1N4001
D2504	1C4	3111.4001	DIODE POWER 1A 50V	1N4001
D2505	1B4	3110.4152	DIODE SIGNAL	1N4152
D2601	1A4	3113.0751	DIODE POWER 6A 100V	MR751
D2602	1B5	3113.0751	DIODE POWER 6A 100V	MR751
D3201	1H9	3111.4001	DIODE POWER 1A 50V	1N4001
D3301	1H7	3110.4152	DIODE SIGNAL	1N4152
D3302	1H6	3111.4001	DIODE POWER 1A 50V	1N4001
D4201	1F9	3111.4001	DIODE POWER 1A 50V	1N4001
D4301	1G7	3110.4152	DIODE SIGNAL	1N4152
D4302	1F6	3111.4001	DIODE POWER 1A 50V	1N4001
D4501	1G5	3140.0254	BRIDGE 2A 100V	3N254
D5201	1F8	3111.4001	DIODE POWER 1A 50V	1N4001
D5301	1E7	3110.4152	DIODE SIGNAL	1N4152
D5302	1F6	3111.4001	DIODE POWER 1A 50V	1N4001
D5601	1E5	3140.0254	BRIDGE 2A 100V	3N254
D6201	1D8	3111.4001	DIODE POWER 1A 50V	1N4001
D6301	1D7	3110.4152	DIODE SIGNAL	1N4152
D6302	1D6	3111.4001	DIODE POWER 1A 50V	1N4001
E1501	---	4261.0001	FUSE CLIP PC	

Replaceable Electrical Parts List: 9PSA.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
E1601	—	4261.0001	FUSE CLIP PC	
F15	1A6	4610.1000	FUSE NORM-BLO 1/4	10A
H24	—	7210.0001	HEAT SINK PC CLIP	TO220
H53	—	7210.0001	HEAT SINK PC CLIP	TO220
H63	—	7210.0001	HEAT SINK PC CLIP	TO220
P31	1B10	4222.0012	PLUG PC .156	12 PIN
P33	1D10	4221.0036	PLUG PC .1 X.43	36 PIN
P36	1A3	4222.0009	PLUG PC .156	9 PIN
P51	1A10	4221.0036	PLUG PC .1 X.43	36 PIN
Q2301	1B6	3211.2222	XSTR NPN TO92	PN2222A
Q2401	1B7	3225.0031	XSTR PNP TO220	TIP31A
Q2501	1A6	3241.6400	SCR 16A 50V	2N6400
R1301	1B8	1656.1008	RES 3W W WND 1%	.10
R1302	1B9	1656.1008	RES 3W W WND 1%	.10
R2201	1B8	1214.0102	RES 1/4W C FLM 5%	1K
R2202	1C8	1139.9981	RES 1/8W M FLM .1%	9.98K
R2203	1C8	1139.5001	RES 1/8W M FLM .1%	5.00K
R2301	1C9	1136.2000	RES 1/8W M FLM 1%	200
R2302	1C9	1136.1002	RES 1/8W M FLM 1%	10.0K
R2303	1B6	1214.0221	RES 1/4W C FLM 5%	220
R2304	1B6	1214.0103	RES 1/4W C FLM 5%	10K
R2305	1C7	1214.0102	RES 1/4W C FLM 5%	1K
R2401	1A7	1214.0100	RES 1/4W C FLM 5%	10
R2501	1B6	1214.0102	RES 1/4W C FLM 5%	1K
R2502	1C4	1214.0102	RES 1/4W C FLM 5%	1K
R2503	1C4	1214.0103	RES 1/4W C FLM 5%	10K
R2504	1C5	1214.0102	RES 1/4W C FLM 5%	1K
R3201	1G8	4412.0202	POT TRIM PC ENC	2K
R3301	1G8	1214.0103	RES 1/4W C FLM 5%	10K
R3302	1H7	1136.1210	RES 1/8W M FLM 1%	121
R3303	1G6	1136.1401	RES 1/8W M FLM 1%	1.40K
R4201	1G8	4412.0202	POT TRIM PC ENC	2K
R4301	1G8	1214.0103	RES 1/4W C FLM 5%	10K
R4302	1G7	1136.1210	RES 1/8W M FLM 1%	121
R4303	1G6	1136.1401	RES 1/8W M FLM 1%	1.40K
R4501	1G4	1214.0101	RES 1/4W C FLM 5%	100
R4601	1D4	1214.0101	RES 1/4W C FLM 5%	100
R5301	1E7	1136.1210	RES 1/8W M FLM 1%	121
R5302	1E6	1139.2001	RES 1/8W M FLM .1%	2.00K
R6101	1A9	1214.0221	RES 1/4W C FLM 5%	220
R6301	1D7	1136.1210	RES 1/8W M FLM 1%	121
R6302	1E6	1139.2001	RES 1/8W M FLM .1%	2.00K
U23	1C7,1C9	3422.0393	COMPARATOR DUAL	LM393
U53	1F6	3431.0337	VOLT REG NEG VAR TO220	LM337
U63	1D6	3430.0317	VOLT REG POS VAR TO220	LM317

PSA-2 POWER SUPPLY



POWER SUPPLY 9PSA.2000 (6200.PSA2.1)

PSA-2, POWER SUPPLY MODULE

NOTE: There have been two versions of the power supply module. The PSA-1 version contains 3 heatsinks while the PSA-2 version contains 5 heatsinks. The PSA-2 must be installed in any DSP configuration system.

Introduction

The PSA-2 power supply provides five regulated voltages (+5V, +15V, -15V, +22V, and -22V), plus an unregulated supply for the cooling fan. A power line sync signal and power fail reset drive signal are also provided.

+5V Supply

A center tapped transformer winding is full wave rectified by D1601 and D1602 and filtered by C2501 and C2502 to provide a +8V to +11 V raw dc supply. The raw dc is fed through fuse F15 to the main pass device EC51 mounted on the chassis. EC51 and Q1401 are connected in a complementary darlington configuration. The emitter of Q1401 drives the output through current sense resistors R2402 and R2403. The output voltage is sensed by U14A via R2401 and is compared to the +5V reference determined by R1305, R1306 and the +15V supply. R1503 provides the pullup for the open collector output of U14. C1501 provides dominant pole compensation. C2401 continues this compensation when the equivalent series resistance (ESR) of C1501 prevents continued rolloff.

Current limiting occurs at about 7.5 Amp by sensing the voltage drop across the sense resistors R2402 and R2403. This drop is offset about 370 mV negative by R1303 and R1304 to be less than +5 V until current limit is reached. When supply current exceeds approximately 7.5 Amp, the voltage at pin 6 of U14B will become more positive than the voltage at pin 5 (+5V). U14B begins to conduct and drops the +5 reference generated by R1305 and R1306. D1501 senses if the output voltage exceeds approximately +5.6 V and will fire the SCR crowbar Q1502 and blow fuse F15. R1504 and C1502 form a lowpass filter to prevent high frequency and impulsive noise from triggering the crowbar circuit erroneously.

±15V Supplies

A center tapped transformer winding drives a full wave rectifier bridge D3501. Filtering is provided by C4401 and C4401. The raw voltage is regulated by three terminal adjustable regulators U42 and U12. Resistor dividers R4102/R4103 and R1101/R1102 scale the output voltages to +15V and -15V respectively. Potentiometers R4201 and R1201 and resistors R4101 and R1103 adjust the divider ratios to compensate for tolerances of the regulators and allow accurate supply voltages. C4201 and C1201 provide filtering to eliminate noise generated internal to the regulators. C3101 and C2102 insure high frequency stability of the voltage regulators. D3102 and D2101 protect against reverse voltage on the regulator outputs. D4101, D4102, D1101 and D1102 provide capacitor discharge paths during power down and supply fault conditions.

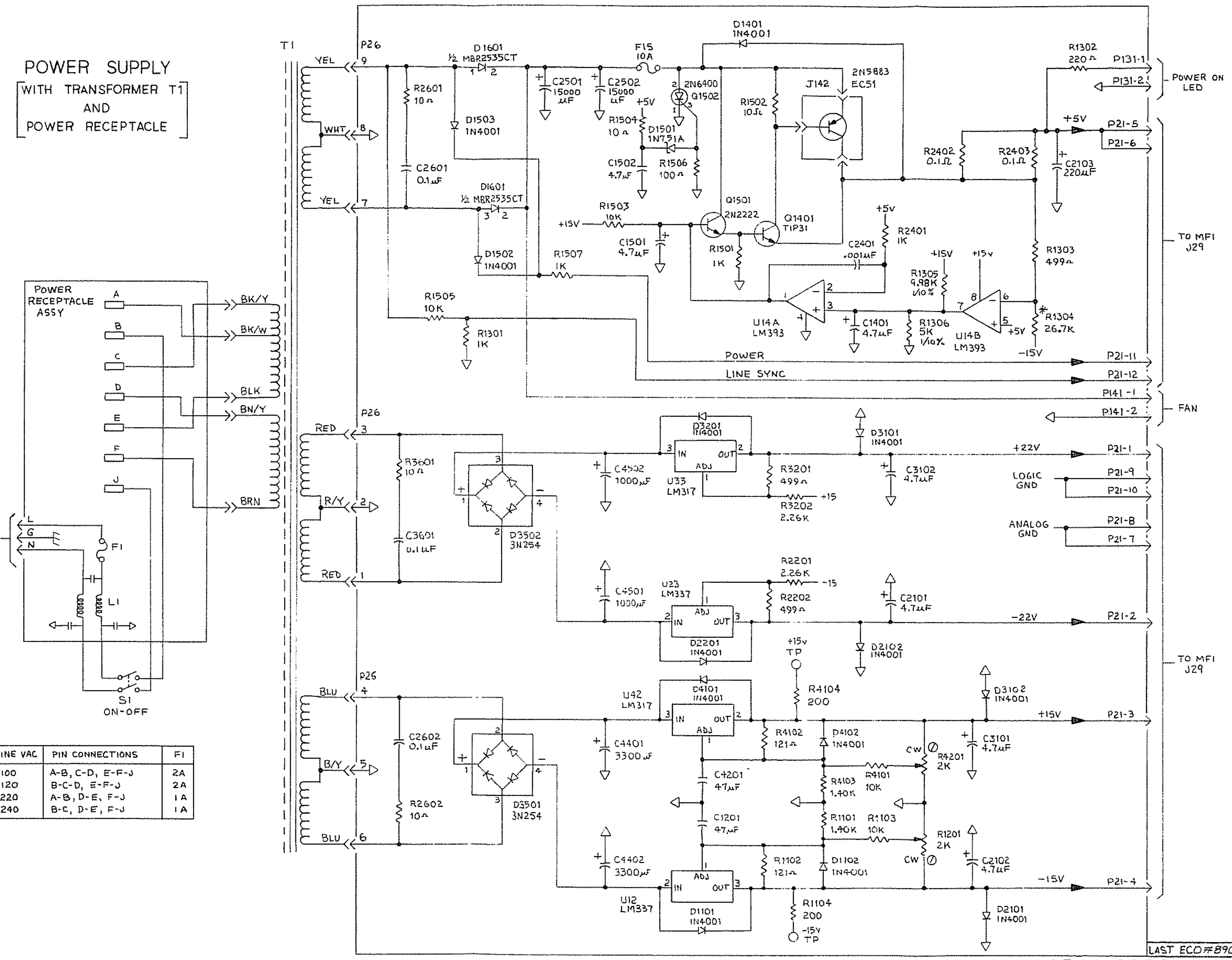
±22V Supplies

A center tapped transformer winding drives a full wave rectifier bridge D3502. Filtering is provided by C4501 and C4502. The raw voltage is regulated by three terminal adjustable regulators U33 and U23. Resistor dividers R3201/R3202 and R2201/R2202 scale the output voltages to +22V and -22V respectively. Note that the ±22V supplies are effectively referenced to the ±15V supplies. C3201 and C2101 insure high frequency stability of the regulators. D3101 and D2102 protect against reverse voltage on the regulator outputs.

Fan Supply & Power Down Signal

The fan is powered directly from the raw +8V to +11V supply with no additional filtering or protection. A short at this point in the circuit may cause the main fuse in the power entry module to blow. Diodes D1502 and D1503 provide a sense signal for the reset circuits located on the mainframe interface circuit board. Resistor R1507 provides inherent current limiting protection. Line sync is provided by tapping one side of the ac signal from the +5V winding through R1301 and R1505.

POWER SUPPLY
[WITH TRANSFORMER T1 AND POWER RECEPTACLE]



LINE VAC	PIN CONNECTIONS	F1
100	A-B, C-D, E-F-J	2A
120	B-C-D, E-F-J	2A
220	A-B, D-E, F-J	1A
240	B-C, D-E, F-J	1A

LAST ECO #89021

9PSA.2000 DATE: 1-8-91

SHT 1 of 1

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1201	1G6	2932.0476	CAP AL-EL 25V 20%	47UF
C1401	1C7	2942.0475	CAP AL-EL 35V 20%	4.7UF
C1501	1C6	2942.0475	CAP AL-EL 35V 20%	4.7UF
C1502	1B6	2942.0475	CAP AL-EL 35V 20%	4.7UF
C2101	1F8	2942.0475	CAP AL-EL 35V 20%	4.7UF
C2102	1H9	2942.0475	CAP AL-EL 35V 20%	4.7UF
C2103	1B9	2911.0227	CAP AL-EL 10V +80/-20%	220UF
C2401	1C8	2276.0102	CAP MICA 100V 1%	.001UF
C2501	1A5	2921.0159	CAP AL-EL 16V +80/-20%	15MF
C2502	1B6	2921.0159	CAP AL-EL 16V +80/-20%	15MF
C2601	1B4	2172.0104	CAP CERAM 100V 20%	.1UF
C2602	1G4	2172.0104	CAP CERAM 100V 20%	.1UF
C3101	1G9	2942.0475	CAP AL-EL 35V 20%	4.7UF
C3102	1D8	2942.0475	CAP AL-EL 35V 20%	4.7UF
C3601	1E4	2172.0104	CAP CERAM 100V 20%	.1UF
C4201	1G6	2932.0476	CAP AL-EL 25V 20%	47UF
C4401	1G6	2941.0338	CAP AL-EL 35V +80/-20%	3300UF
C4402	1D6	2941.0338	CAP AL-EL 35V +80/-20%	3300UF
C4501	1E6	2941.0108	CAP AL-EL 35V +80/-20%	1000UF
C4502	1E6	2941.0108	CAP AL-EL 35V +80/-20%	1000UF
D1101	1H6	3111.4001	DIODE POWER 1A 50V	4001
D1102	1H7	3111.4001	DIODE POWER 1A 50V	4001
D1401	1A7	3111.4001	DIODE POWER 1A 50V	4001
D1501	1B6	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D1502	1C4	3111.4001	DIODE POWER 1A 50V	4001
D1503	1B4	3111.4001	DIODE POWER 1A 50V	4001
D1601	1A4,1B4	3125.2535	DIODE SHTKY DUAL 20A	MBR2535CT
D2101	1H9	3111.4001	DIODE POWER 1A 50V	4001
D2102	1F7	3111.4001	DIODE POWER 1A 50V	4001
D2201	1F6	3111.4001	DIODE POWER 1A 50V	4001
D3101	1D7	3111.4001	DIODE POWER 1A 50V	4001
D3102	1F9	3111.4001	DIODE POWER 1A 50V	4001
D3201	1D6	3111.4001	DIODE POWER 1A 50V	4001
D3501	1G5	3140.0254	BRIDGE 2A 100V	3N254
D3502	1E5	3140.0254	BRIDGE 2A 100V	3N254
D4101	1F6	3111.4001	DIODE POWER 1A 50V	4001
D4102	1G7	3111.4001	DIODE POWER 1A 50V	4001
E151		4261.0001	FUSE CLIP PC	
E152		4261.0001	FUSE CLIP PC	
F15	1A6	4610.1000	FUSE NORM-BLO 1/4	10A
H12		7210.0002	HEAT SINK PC SCREW MT	TO220
H14		7210.0001	HEAT SINK PC CLIP	TO220
H16		7210.0001	HEAT SINK PC CLIP	TO220
H23		7210.0001	HEAT SINK PC CLIP	TO220
H33		7210.0001	HEAT SINK PC CLIP	TO220
H42		7210.0002	HEAT SINK PC SCREW MT	TO220
J142	1B7	4231.0003	SOCKET XSTR PC	TO3

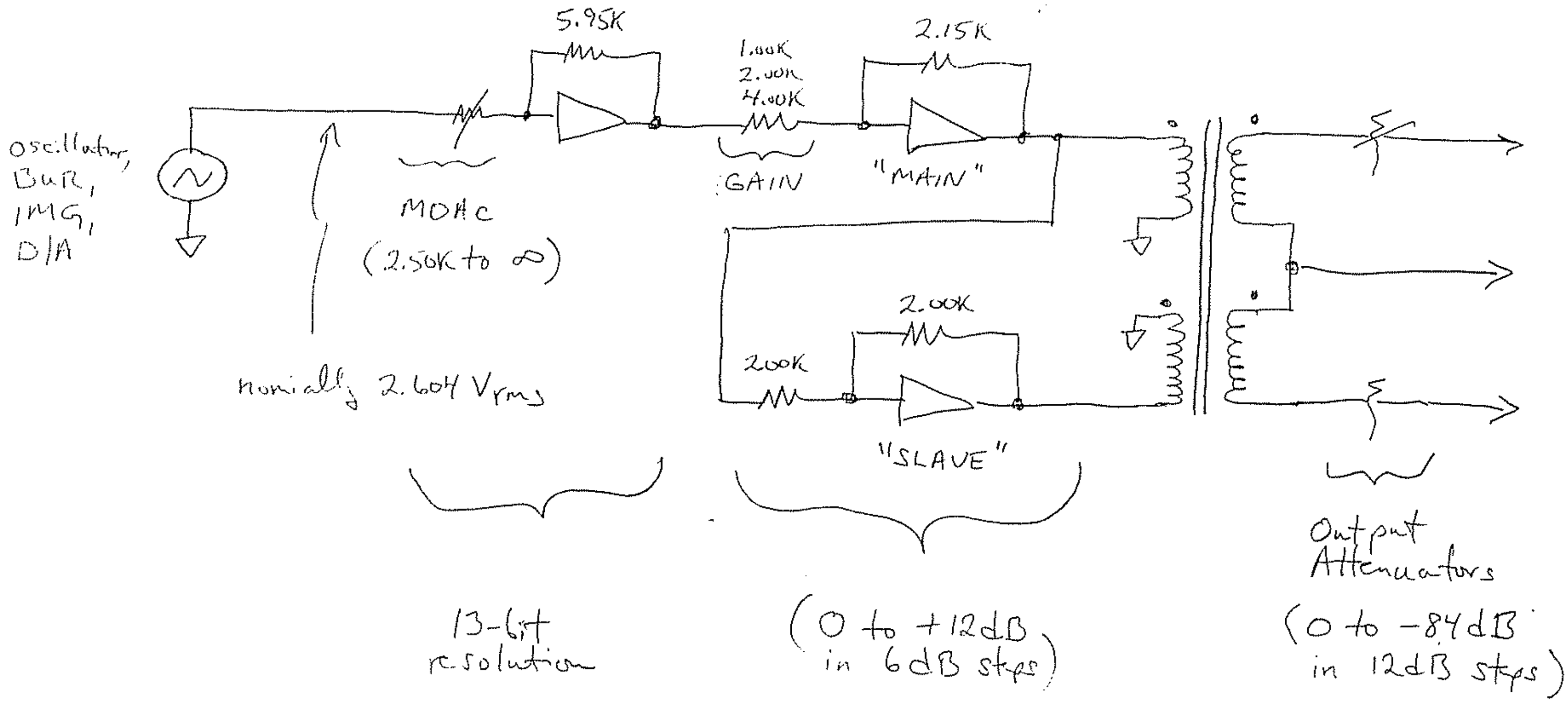
REPLACEABLE ELECTRICAL PARTS LIST: 9PSA.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
P131	1A10	4221.0036	PLUG PC .1 X.43	36 PIN
P141	1D10	4221.0036	PLUG PC .1 X.43	36 PIN
P21	1D-H10	4222.0012	PLUG PC .156	12 PIN
P26	1A-H4	4222.0009	PLUG PC .156	9 PIN
Q1401	1C7	3225.0031	XSTR NPN TO220	TIP31C
Q1501	1C6	3211.2222	XSTR NPN TO92	PN2222A
Q1502	1A6	3241.6400	SCR 16A 50V	2N6400
R1101	1G7	1136.1401	RES 1/8W M FLM 1%	1.40K
R1102	1H7	1136.1210	RES 1/8W M FLM 1%	121
R1103	1G8	1214.0103	RES 1/4W C FLM 5%	10K
R1104	1H7	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R1201	1G8	4412.0202	POT TRIM PC ENC	2K
R1301	1C4	1214.0102	RES 1/4W C FLM 5%	1K
R1302	1A9	1214.0221	RES 1/4W C FLM 5%	220
R1303	1C9	1136.4990	RES 1/8W M FLM 1%	499
R1304	1C9	1136.2672	RES 1/8W M FLM 1%	26.7K
R1305	1C8	1139.9981	RES 1/8W M FLM .1%	9.98K
R1306	1C8	1139.5001	RES 1/8W M FLM .1%	5.00K
R1501	1C6	1214.0102	RES 1/4W C FLM 5%	1K
R1502	1B7	1214.0100	RES 1/4W C FLM 5%	10
R1503	1C5	1214.0103	RES 1/4W C FLM 5%	10K
R1504	1B6	1214.0100	RES 1/4W C FLM 5%	10
R1505	1C4	1214.0103	RES 1/4W C FLM 5%	10K
R1506	1B6	1214.0101	RES 1/4W C FLM 5%	100
R1507	1C5	1214.0102	RES 1/4W C FLM 5%	1K
R2201	1E7	1136.2261	RES 1/8W M FLM 1%	2.26K
R2202	1F7	1136.4990	RES 1/8W M FLM 1%	499
R2401	1C8	1214.0102	RES 1/4W C FLM 5%	1K
R2402	1B8	1656.1008	RES 3W W WND 1%	.10
R2403	1B9	1656.1008	RES 3W W WND 1%	.10
R2601	1B4	1214.0100	RES 1/4W C FLM 5%	10
R2602	1G4	1214.0100	RES 1/4W C FLM 5%	10
R3201	1E7	1136.4990	RES 1/8W M FLM 1%	499
R3202	1E7	1136.2261	RES 1/8W M FLM 1%	2.26K
R3601	1E4	1214.0100	RES 1/4W C FLM 5%	10
R4101	1G8	1214.0103	RES 1/4W C FLM 5%	10K
R4102	1G7	1136.1210	RES 1/8W M FLM 1%	121
R4103	1G7	1136.1401	RES 1/8W M FLM 1%	1.40K
R4104	1F7	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4201	1G8	4412.0202	POT TRIM PC ENC	2K
U12	1H6	3431.0337	VOLT REG NEG VAR TO220	LM337
U14	1C7,1C8	3422.0393	COMPARATOR DUAL	LM393
U23	1F6	3431.0337	VOLT REG NEG VAR TO220	LM337
U33	1D6	3430.0317	VOLT REG POS VAR TO220	LM317
U42	1F6	3430.0317	VOLT REG POS VAR TO220	LM317

GEN-1 GENERATOR MODULE

AMPAD 22-141 50 SHEETS
22-142 100 SHEETS
22-144 200 SHEETS

SGEN AMPLITUDE CONTROL



— B Hofer
FEB 2002

SYSTEM TWO GENERATOR OUTPUT RANGES

(Cascade and Cascade Plus running under APWIN 2.20 or higher)

VOLTAGE RANGE (balanced configuration)			MDAC resolution (lsb)	GAIN CONTROL			OUTPUT ATTENUATORS			
				K961 (/2)	K962 (x2)	U862 gain	K781 (-12)	K861 (-24)	K981 (-48)	total dB
13.333 V	to	26.666 V	3.26 mV	off	on	x 2.150	off	off	off	0 dB
6.480 V	to	13.333 V	1.63 mV	off	off	x 1.075	off	off	off	0 dB
3.240 V	to	6.480 V	0.81 mV	on	off	x 0.5375	off	off	off	0 dB
1.620 V	to	3.240 V	407 uV	off	off	x 1.075	on	off	off	12 dB
0.810 V	to	1.620 V	203 uV	on	off	x 0.5375	on	off	off	12 dB
405.0 mV	to	0.810 V	102 uV	off	off	x 1.075	off	on	off	24 dB
202.5 mV	to	405.0 mV	50.9 uV	on	off	x 0.5375	off	on	off	24 dB
101.3 mV	to	202.5 mV	25.4 uV	off	off	x 1.075	on	on	off	36 dB
50.63 mV	to	101.3 mV	12.7 uV	on	off	x 0.5375	on	on	off	36 dB
25.31 mV	to	50.63 mV	6.36 uV	off	off	x 1.075	off	off	on	48 dB
12.66 mV	to	25.31 mV	3.18 uV	on	off	x 0.5375	off	off	on	48 dB
6.328 mV	to	12.66 mV	1.59 uV	off	off	x 1.075	on	off	on	60 dB
3.164 mV	to	6.328 mV	0.80 uV	on	off	x 0.5375	on	off	on	60 dB
1.582 mV	to	3.164 mV	0.40 uV	off	off	x 1.075	off	on	on	72 dB
791 uV	to	1.582 mV	0.20 uV	on	off	x 0.5375	off	on	on	72 dB
395.5 uV	to	791 uV	0.10 uV	off	off	x 1.075	on	on	on	84 dB
0 V	to	395.5 uV	0.05 uV	on	off	x 0.5375	on	on	on	84 dB

SYSTEM TWO GENERATOR OUTPUT RANGES

(S2 and Cascade running under APWIN 2.1x or lower)

VOLTAGE RANGE (balanced configuration)			MDAC resolution (lsb)	GAIN CONTROL			OUTPUT ATTENUATORS			
				K961 (/2)	K962 (x2)	U862 gain	K781 (-12)	K861 (-24)	K981 (-48)	total dB
12.000 V	to	26.666 V	3.26 mV	off	on	x 2.150	off	off	off	0 dB
6.000 V	to	12.000 V	1.63 mV	off	off	x 1.075	off	off	off	0 dB
3.000 V	to	6.000 V	0.81 mV	on	off	x 0.5375	off	off	off	0 dB
1.500 V	to	3.000 V	407 uV	off	off	x 1.075	on	off	off	12 dB
0.750 V	to	1.500 V	203 uV	on	off	x 0.5375	on	off	off	12 dB
375 mV	to	0.750 V	102 uV	off	off	x 1.075	off	on	off	24 dB
187.5 mV	to	375 mV	50.9 uV	on	off	x 0.5375	off	on	off	24 dB
93.8 mV	to	187.5 mV	25.4 uV	off	off	x 1.075	on	on	off	36 dB
46.88 mV	to	93.8 mV	12.7 uV	on	off	x 0.5375	on	on	off	36 dB
23.44 mV	to	46.88 mV	6.36 uV	off	off	x 1.075	off	off	on	48 dB
11.72 mV	to	23.44 mV	3.18 uV	on	off	x 0.5375	off	off	on	48 dB
5.859 mV	to	11.72 mV	1.59 uV	off	off	x 1.075	on	off	on	60 dB
2.930 mV	to	5.859 mV	0.80 uV	on	off	x 0.5375	on	off	on	60 dB
1.465 mV	to	2.930 mV	0.40 uV	off	off	x 1.075	off	on	on	72 dB
732 uV	to	1.465 mV	0.20 uV	on	off	x 0.5375	off	on	on	72 dB
366 uV	to	732 uV	0.10 uV	off	off	x 1.075	on	on	on	84 dB
0 V	to	366 uV	0.05 uV	on	off	x 0.5375	on	on	on	84 dB

SYSTEM ONE GENERATOR OUTPUT RANGES

(all versions of S1.EXE and APWIN)

VOLTAGE RANGE (balanced configuration)			MDAC resolution (lsb)	GAIN CONTROL		OUTPUT ATTENUATORS		
				K23 (+8)	K34 (-24)	K47 (-12)	K57 (-24)	total dB
10.600 V	to	26.666 V	3.26 mV	on	off	off	off	+8 dB
2.650 V	to	10.600 V	1.30 mV	off	off	off	off	0 dB
662.5 mV	to	2.650 V	325.5 uV	off	off	on	off	-12 dB
165.6 mV	to	662.5 mV	81.4 uV	off	off	on	on	-24 dB
41.40 mV	to	165.6 mV	20.3 uV	off	off	on	on	-36 dB
10.35 mV	to	41.40 mV	5.09 uV	off	on	off	on	-48 dB
0.000	to	10.35 mV	1.27 uV	on	on	on	on	-60 dB

GEN-1, GENERATOR MODULE

The GEN-1 module circuit board contains a state variable oscillator, sample and hold leveler, variable gain amplifier, transformer coupled output amplifier, attenuators, and a period measuring frequency counter. There is additional digital logic on the board to perform address decoding and data latching functions.

Digital Interface < 1 >

The digital interface circuitry consists of the period counter and the address decoding logic. P30 at the left edge of the schematic is the 40-pin cable connection to the MFI board. The entering data is buffered by U101 and used to drive the various latches on the board. The direction of U101 is controlled by the /RD line. The upper four bits of the address bus are compared with the switch settings of S50 by U401. The address is normally set to 2. When a match is found the output of U401 on pin 6 goes high. This drives the address decoders U311 and U312, the /ATT line through Q4001 and is inverted by U411B to drive the data buffer U101 and the option board address decoder U411A.

The address decoder U311 decodes the lower four address bits to select one of the readings ports on the board. The outputs go low when a read from the respective address is taken. The address decoder U312 decodes the lower four address bits to select one of the latches on the board. The outputs go low when data is written to the respective address. Octal latches U151 and U152 hold the frequency information from the host computer. The decade range information appears on F1 and F2, while the mantissa of the frequency word appears on F2 through F15. These lines drive the frequency setting MDACs in the oscillator loop. The decade range bits also drive the tuning capacitor selection circuits and are used to select the prescale ratio in the frequency counter.

Frequency Counter < 1 >

U111, U112, U113, U211, U212, U213, U221 form the frequency counter. This is a period counter whose output is reciprocated by the host computer to obtain a frequency reading. U213 and U221 control the prescaling of the oscillator signal. A square wave version of the oscillator signal drives the clock input of the 12-bit counter U213. One of the outputs of the counter is selected by the 1-of-8 data selector U221. When the counter reaches the desired number of counts the output of the selector will transition from low to high. The number of counts required before the output transitions is determined by the setting of the two decade select bits and the MSB of the frequency word.

TABLE GEN1.1
FREQUENCY COUNTER SCALING

FREQUENCY RANGE	COUNTER DIVIDE	# OF CYCLES
10.00-102.3 Hz	2	1
102.4-204.7 Hz	4	2
204.8-1023 Hz	16	8
1.024-2.047 kHz	32	16
2.048-10.23 kHz	128	64
10.24-20.47 kHz	512	256
20.48-102.3 kHz	2048	1024
102.4-204.8 kHz	4096	2048

The 20 MHz clock is counted by a pair of 12-bit counters U211 and U212. Their outputs drive three 8-bit latches: U111, U112 and U113. The strobe inputs of these latches is fed from the output of the prescale data selector U221 pin 5. When the desired prescale count is reached the strobe inputs will be driven high, capturing the count at that time. A flip-flop U421 is used to synchronize the operation of the clock counters and the prescaler counters. When a measurement is desired the host computer reads from the 0 port. This sets U421B, sending its /Q output low, and drives the data input of U421A low. On the next rising edge of the oscillator main sync signal the Q output will go low, releasing the three counters from reset. They will then start to count. Because of the delay introduced by R5108 and C5103 the oscillator prescale counter will count the same edge that started the count process. When the correct prescale value is reached the Y output of U221 will go high and capture the desired clock count. This signal also clears the start flip-flop U421B. An inverted version of the prescale pulse is taken from the W output of the data selector and used to set U421A. This resets the counters for the next trigger.

U301C buffers and inverts the strobe signal from U221. This signal is used to shut down the clock to the counters via U301B. After a delay introduced by R3002 and C3007 the latch signal is passed through U301A to flip-flop U421B and the latches U111, U112 and U113.

Main Oscillator Loop <2>

The main oscillator loop consists of two integrators and an inverter wired in a ring. This is a standard state variable oscillator/filter loop. The frequency of oscillation is determined by the frequency at which the gain around the loop is unity. The frequency will therefore be determined by the integrator input resistors and feedback capacitors along with the gain of the inverter. This frequency is given by the equation:

$$\text{Freq} = \frac{\text{sqrt(Gain)}}{2\pi * R * C}$$

where the R is the input resistance to the integrators and C is the feedback capacitance. Both capacitors and resistors must be adjusted to cover the range from 10 Hz to 204 kHz. The feedback capacitors are switched in decade steps. The integrator resistors are adjusted within each decade by multiplying D/A converters.

TABLE GEN1.2 shows the range of values for various frequencies of operation. The setting of intermediate MDAC values results in frequencies between the limits given for a particular capacitor value.

TABLE GEN1.2
TYPICAL TUNING ELEMENT VALUES vs FREQUENCY

FREQUENCY	TUNING C	MDAC RESISTANCE
10.00 Hz	333 nF + 330 pF	51.2 kOhms
20.47 Hz	333 nF + 330 pF	25.0 kOhms
204.775 Hz	333 nF + 330 pF	2.50 kOhms
205.00 Hz	33 nF + 330 pF	25.0 kOhms
2.04775 kHz	33 nF + 330 pF	2.50 kOhms
2.050 kHz	3 nF + 330 pF	25.0 kOhms
20.4775 kHz	3 nF + 330 pF	2.50 kOhms
20.500 kHz	330 pF	25.0 kOhms
204.775 kHz	330 pF	2.50 kOhms

Op-amps U171 and U271 are the two integrators while U252 forms the inverter. The variable resistance elements are comprised of the MDACs A161 and A162. These hybrid devices are custom-built high accuracy multiplying D/A converters. They are not repairable to the component level and must be replaced as a unit.

NOTE: Certain aspects of the MDAC design are protected by US patent 4,631,522.

The feedback capacitors are switched by JFETs operating as linearized switches. JFETs Q2601, Q2602, Q2603, Q2801, Q2802, and Q2803 exhibit approximately 5 Ohms resistance when on. They are wired from the appropriate capacitor to the corresponding integrator summing junction. Resistor dividers (for example R2801-R2802 on Q2801) place 1/2 of the drain voltage on the gate to reduce distortion of the JFET when it is conducting. To turn a pair of the JFETs off the gates are pulled negative by one section of U352 through two of the diodes Q2804-Q2806 and Q2604-Q2606. The diodes are transistors with their collectors and bases tied together. Additional resistors are placed from the drains to ground to prevent the drains from being pulled negative by the resistor linearizing networks and turning the JFETs back on.

Each of the integrator stages is compensated for unity gain stability by a two pole network consisting of 47pF capacitors and a 560 Ohm resistor. A 27 Ohm-470 pF RC network from each integrator output to ground improves high frequency stability of the op-amp output stage. Bias current compensation for U171 is provided by R1701 and potentiometer R1602. This is adjusted for a minimum change in sinewave amplitude between 2 kHz and 2.1 kHz.

The inverter stage is formed by U252 and the associated resistors and JFETs. The gain is slightly more than unity. The exact gain in each band is different and is adjusted by the appropriate potentiometer. The adjustment networks are switched in for each decade to compensate for the tolerances of the capacitors. The gain of the inverter is also adjustable by the CMOS D/A converter U251. Its range is scaled by resistors R2404 and R2403 to be within 0.5% of the nominal value. The setting of the MDAC is controlled by the host computer via the octal latch U141. In the HIGH ACCURACY mode of frequency tuning the host computer reads the actual frequency using the counter described earlier, and sets U251 to correct the error.

The amplitude of an RC oscillator is inherently undefined. The control of the oscillator amplitude is performed by adjusting the amount of positive and negative feedback from the output of the first integrator to the input of the inverter. This is accomplished via a four quadrant multiplier consisting of U361, JFET Q3601, and associated components. The inverting gain of the stage is set by R3605 and R3606. This gain is not changed by the presence of JFET Q3601 from the negative input to ground. The noninverting gain depends upon the resistance of Q3601 and is scaled to match the range of the inverting gain path by R3608 and R3609. When the JFET resistance is at its minimum of 25-30 Ohms the gain of the non-inverting path will be at a maximum. This will occur at a gate voltage of 0 V, giving the maximum amount of boost to the oscillator amplitude. When the gate voltage goes very negative the JFET will turn off and the inverting path gain will dominate. This will reduce the oscillator amplitude.

Once the correct amplitude is attained the resistance of the JFET will be maintained at the value necessary to obtain the correct amplitude. Normal operation will maintain the gate voltage at approximately -3 V. The drive for the gate comes from the leveler circuit described below.

The amplitude control range of the main leveler circuit is limited to reduce the amount of distortion it can introduce. As a result it is limited in the speed with which it can correct an error in oscillator amplitude. Therefore there is a second "speed-up" circuit which is capable of getting the oscillator amplitude close to the desired value quickly. JFET Q3602 is used as a switch to apply a large amount of feedback to U252 rapidly increase the oscillation amplitude. In normal operation the gate is held at -15 V which keeps the JFET off. When the speed-up circuit senses that the amplitude is less than about 0.707 of the correct value it allows the gate to rise to ground, turning Q3603 on.

Leveler <3>

The leveler circuits maintain a constant output amplitude of the state variable loop despite changes in the characteristics of components in the loop. These circuits look at the amplitude of the signal and compare it to a reference. Any discrepancy is then corrected, maintaining a constant amplitude. The leveler circuitry consists of a comparison amplifier, a dual stage sample and hold, loop compensation integrator, sampling pulse generator, speed-up comparator and settling test comparator.

The output signal from the oscillator labeled 0° is subtracted from a reference by U510B. The reference is supplied by D5001, adjustment for tolerance is provided by R5001. The output of U510B is clamped by diode D5002 to prevent excessive amplitude during the majority of the time when the sinewave is below its most positive peak. The output of the comparison amplifier is sampled by JFET switch Q5105 and stored on C5206. The sampled voltage is buffered by U521A and drives a second sampler composed of Q5202 and C5201. U521B buffers the output of the second sampler to enable driving the loop integrator.

The JFET switches require up to -10 V gate-source bias for pinch off. This is accomplished by pulling the gate to the -15V supply via NPN transistors Q5104 and Q5102. Level translation of the TTL control signals to the NPN transistors is provided by PNP transistors Q5103 and Q5101. When the TTL drive signal is high, current will be injected into the base of the NPN device turning it on. The collector will go low, pulling the gate to -15 V and turning off the JFET. When the TTL input is low both transistors will be off and the JFET gate will rise to the potential of the source, thus turning it on.

The output of U521B appears at the ERROR test point and is a dc voltage representing the difference between the peak value of the signal and the reference. The error signal is then integrated by U523B, inverted by U523A, and mixed with the proportional error signal from U521B to obtain the control signal which drives the JFET multiplier described earlier. For optimum speed of leveling, the time constant of the integrator must be a function of frequency. By connecting the integrator input resistor for a fixed amount of time each cycle the resistance will appear to increase as the frequency goes down. This is due to the fixed pulse width creating a decreasing duty factor as the frequency decreases.

The sampling pulses are generated by squaring the 90° signal from the oscillator with U510A. Its output is clamped by D5101-D5103 and fed to a Schmitt NAND U412A used as a buffer. The output is a square wave which crosses zero when the peak of the 0° signal occurs. This drives the first sampler and a one shot circuit composed of U412B, C5106, D4101 and R4105. It also supplies the signal for the front panel SYNC OUTPUT connector via circuitry on schematic <4>. The output of the one shot is a 100 usec pulse which is used to drive the second sample-and-hold. This is also the fixed width pulse used to switch the integrator input resistor. Both sync signals are used to drive the period counter on schematic <1>. Comparators U422C and U422D are used to drive JFET switches Q5204 and Q5205. These are used to reduce the bandwidth of the sample and hold at lower frequencies to reduce amplitude modulation noise of the sinewave. At frequencies below 20.4 kHz, Q5204 switches 270 Ohms in series with C5206. At frequencies below 2.04 kHz, Q5205 switches an additional 1 kOhm in series with the capacitor. Capacitors C5107 and C5205 compensate for the charge injection of their respective JFET switches.

When the leveler has established a stable level for the oscillator the output of the second sample and hold will be zero. This is because the peaks of the sinewave have been made equal to the reference.

Quad comparator U531 and its associated components provide the drive signal for the speed-up JFET Q3602. At any instant of time a correctly leveled generator will have either the 90° or the 0° signals within 0.707 of the peak value. By comparing the 0° and 90° signals against both positive and negative references of 0.65 of the peak value a low amplitude condition can be detected. The outputs of the comparators are paralleled in a wired-OR configuration and drive the speed-up JFET. If either of the signals goes below the required amplitude, the output will be allowed to go high thus turning on the JFET switch and bringing the amplitude up quickly. Since there is gain around the oscillator loop R5314 and R5315 attenuate the 90° signal to match the amplitude of the 0° signal.

Option Switching <4>

The main sync signal from the oscillator leveler is fed to data selector U313 and up to the option boards. This selects between the main sync and the sync signal from the option boards. The output of U313 is clamped and isolated with resistors to drive the front panel SYNC bnc. The status information from the option boards, the frequency counter reading ready signal, the output current limit sense and the oscillator leveled signals drive tri-state octal buffer U121.

The 0° signal from the oscillator is fed to the option boards and relay K54. The output of this relay drives the MDAC variable gain stage on schematic <5>. This signal is also buffered by U431B and drives the front panel MONITOR OUTPUT connector. The other input to the relay comes from the option boards and from Q5301 which can switch the 90° signal into the output. Mode control information is latched with U122 and used to drive the select relay K54, the 90° select JFET Q5301, the oscillator shutdown comparator and various functions on the option boards. After power on reset the outputs of U122 are held in tri-state by the safety line until the host computer can write the correct data to it. The remainder of the schematic shows the other signal connections to the option board connectors J20 and J23, power supplies, the data bus, a portion of the address bus, and various status and mode lines discussed earlier.

Variable Gain Amplifier <5>

Generator amplitude is controlled by a variable gain amplifier, range switching relays K23 & K34, and two output attenuators located on schematic <8>. The variable gain amplifier is composed of U331 and provides amplitude control by varying both its input and feedback resistances. Hybrid A24 functions as a programmable input resistor with 13-bit resolution. The minimum resistance of A24 with all control bits on (the on state is a logic low) is 2.50 kOhm. The feedback resistance of U331 is switched via K23 to provide a +8 dB (x2.5) gain increase for the highest output amplitude range. K34 switches a 24 dB (1/16) attenuator in series with the transformer drive amplifier to obtain the two lowest output amplitude ranges.

All amplitude units are internally converted to open circuit (unloaded) Vrms. Following range selection, the 13-bit control word is determined using the formula:

$$V_{out}\ (rms) = (Vmax/8192) * N$$

where Vmax is the range maximum and N is the value of the 13-bit variable gain stage control word. Amplitude settability is Vmax/8192, or approximately 0.0011 dB near the top of each range.

TABLE GEN1.3 lists the ranges and the state of the gain setting relays and output attenuators for the balanced output mode. The output ranges and Vmax must be divided by 2 (-6 dB) for unbalanced or common-mode-test modes. Attenuator and gain setting resistor tolerances can cause 0.02-0.04 dB ratio errors between ranges.

TABLE GEN1.3
BALANCED OUTPUT VOLTAGE RANGES

RANGE	Vmax	K23	K34	ATTEN
10.60-26.66 V	26.667 V	On	On	0 dB
2.650-10.60 V	10.667 V	Off	On	0 dB
0.6625-2.650 V	2.667 V	Off	On	12 dB
165.6-662.5 mV	666.7 mV	Off	On	24 dB
41.40-165.6 mV	166.7 mV	Off	On	12+24 dB
10.35-41.40 mV	41.67 mV	Off	Off	24 dB
0-10.35 mV	10.42 mV	Off	Off	12+24 dB

Data latches U131 and U132 provide the control bits for A24 (13-bits), K23, and K34. The output of flip-flop U412 holds the data latches in the disabled state until data is written to the MSB of the amplitude word. This signal, labeled SAFETY, is used to disable the data latches located on schematics <4> and <8> until the host computer can service the generator module.

Transformer Drive Circuit <5>

The signal from the variable gain stage is connected to output amplifier A which, in turn, drives a second amplifier B and the output coupling transformer, T56. This doubles the available output voltage swing and balances the drive to T56 to reduce output imbalance. Amplifiers A and B are of identical design and shown on schematics <6> and <7>. When de-energized, K34 reduces the inverting gain of amplifier A by 24 dB (1/16) to provide the two lowest output amplitude ranges (see TABLE GEN1.3).

The low side of the primary winding driven by amplifier A is grounded through a sense resistor built inside the transformer. The signal across the sense resistance is coupled back into the positive input of amplifier A, creating a negative drive impedance condition. If the magnitude of the negative drive impedance exactly matches the primary winding resistance, transformer distortion (due to non-linear excitation currents) will disappear. Distortion reduction can exceed 60 dB when R4601 is properly adjusted.

NOTE: Certain aspects of this circuit are protected by US Patent 4,614,914.

U431A and associated components form a very low frequency servo to maintain the output offset of amplifier A near 0 V. Comparators U422A and U422B sense the peak primary current. If it exceeds approximately 140-150 mA, the comparators will trip and signal the host computer that there is an overload condition.

Output Amplifiers <6,7>

The circuits of the two output amplifiers are basically identical, and only one (schematic <6>) will be discussed for convenience. The input signal is applied to the differential pair Q4401 and Q4402. Diodes D4401 and D4402 provide protection against overload. The input pair is driven from constant current source Q4501 and its associated biasing resistors. The differential output current from the front end drives a current mirror Q4404 and Q4403. The output of the mirror is buffered by Q4405 which drives the transconductance amplifier Q4502. The output stage is fully complementary consisting of driver transistors Q4503 and Q4504 and output devices Q4505 and Q4506. The emitter resistors of the drivers are bootstrapped by capacitors C4501 and C4502. Biasing is provided by R4509 and R4505. Diodes D4501 and D4502 act as current limiters, shunting base drive when the total amplifier output current through R4513 and R4512 exceeds approximately 200-240 mA. Diodes D4503 and D4504 protect against flyback voltages at the output of the amplifier. The output stage power supplies are decoupled differentially by C4508 to eliminate current spikes on the power supplies. Compensation for the amplifier is provided by two pole network C4503, C4504, R4503, and R4409 and by the pole zero network R4502 and C4505.

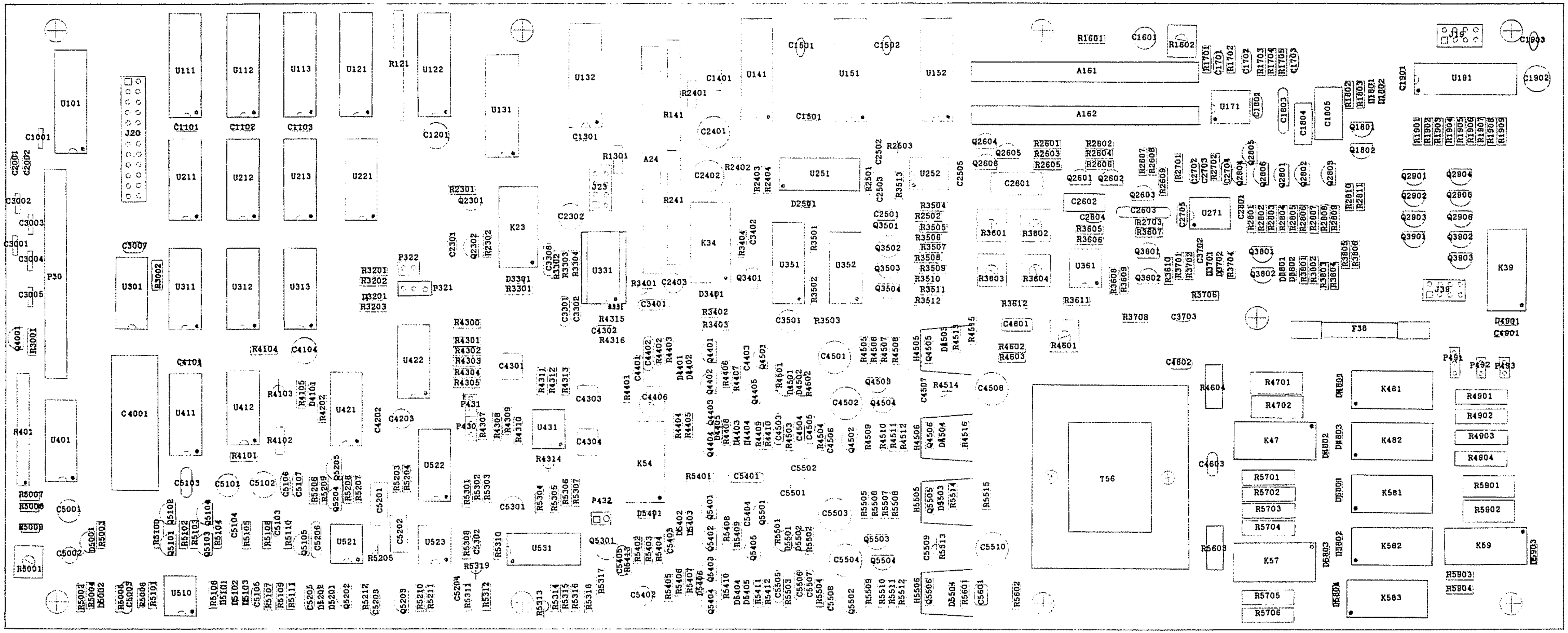
Output Attenuators and Switching <8>

The transformer output drives attenuator networks and output switching relays. The transformer secondaries are padded by resistors R4604 and R5603 to establish the basic generator source impedance of 50 Ohms (36 Ohms in systems with option **EURZ** installed). The small leakage inductance of the transformer is compensated by capacitors C4602 and C4603. These are factory selected to obtain the least reactive output impedance by comparing unloaded and loaded high frequency responses. The outputs from these networks are connected to a 12 dB step attenuator R4702-R5701 and R4701-R5702, switched by K47; and a 24 dB step attenuator R5704-R5706 and R5703-R5705, switched by K57. The balanced and attenuated output signals at this point are labeled VP and VN. These feed the output configuration switching of both the generator module and the channel B output circuitry located on the DUA-1 board via J39.

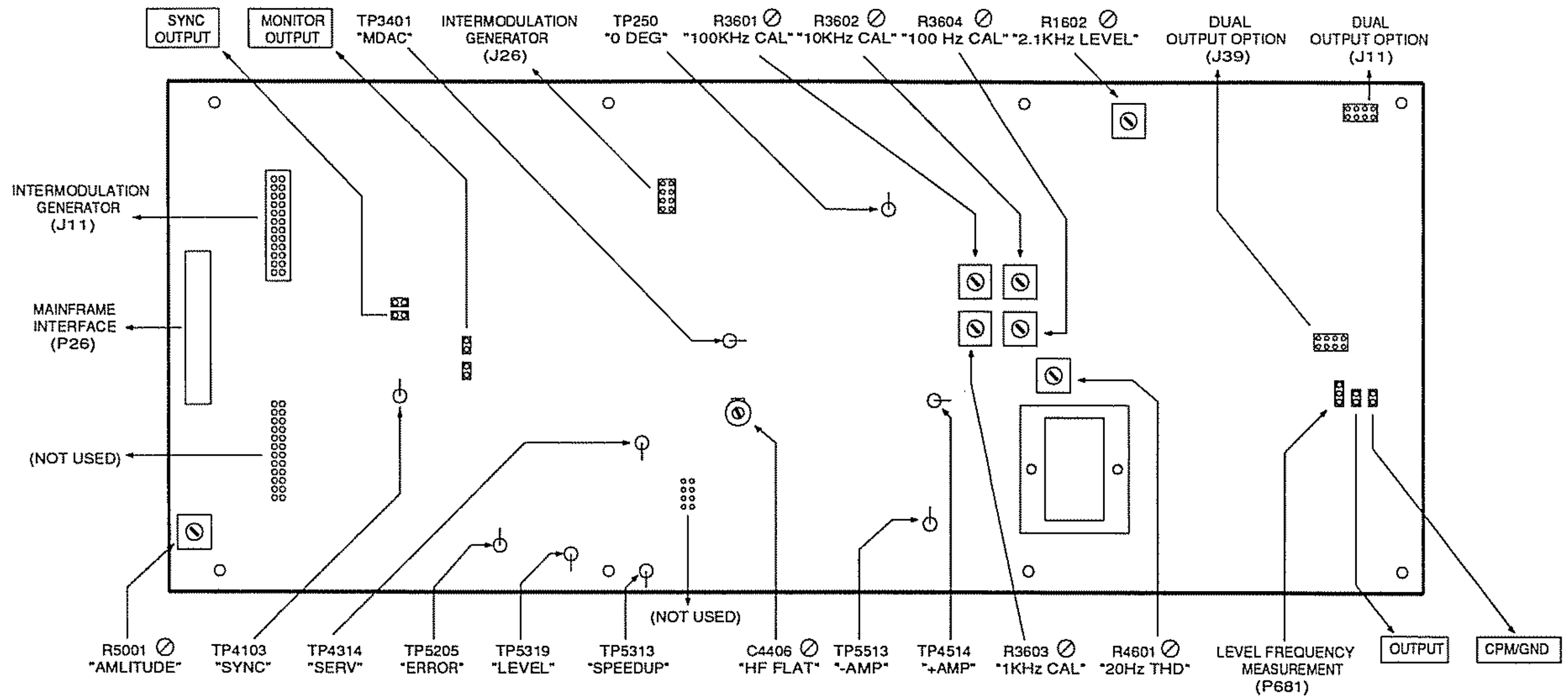
Signals VP and VN pass through the output on/off relay K583 to the output impedance selection circuitry. R5903 and R5904 provide the proper back termination when K583 is off. When both K581 and K582 are off, R4901, R4902, R4903, and R4904 increase the source resistance to 600 Ohms. If K581 is energized, resistors R5901 and R5902 shunt the output resistance down to 150 Ohms (200 Ohms in systems with option **EURZ** installed).

If K59 is energized the center tap of the resistors will be driven from one half of the transformer, creating the common mode test configuration. The unbalanced output configuration is selected by K482 which taps one half of the transformer and lifts R4902 to correct the output impedance. The output may be grounded through fuse F38 via relay K39. The output feeds the front panel connectors and is also connected to generator monitor relay K481.

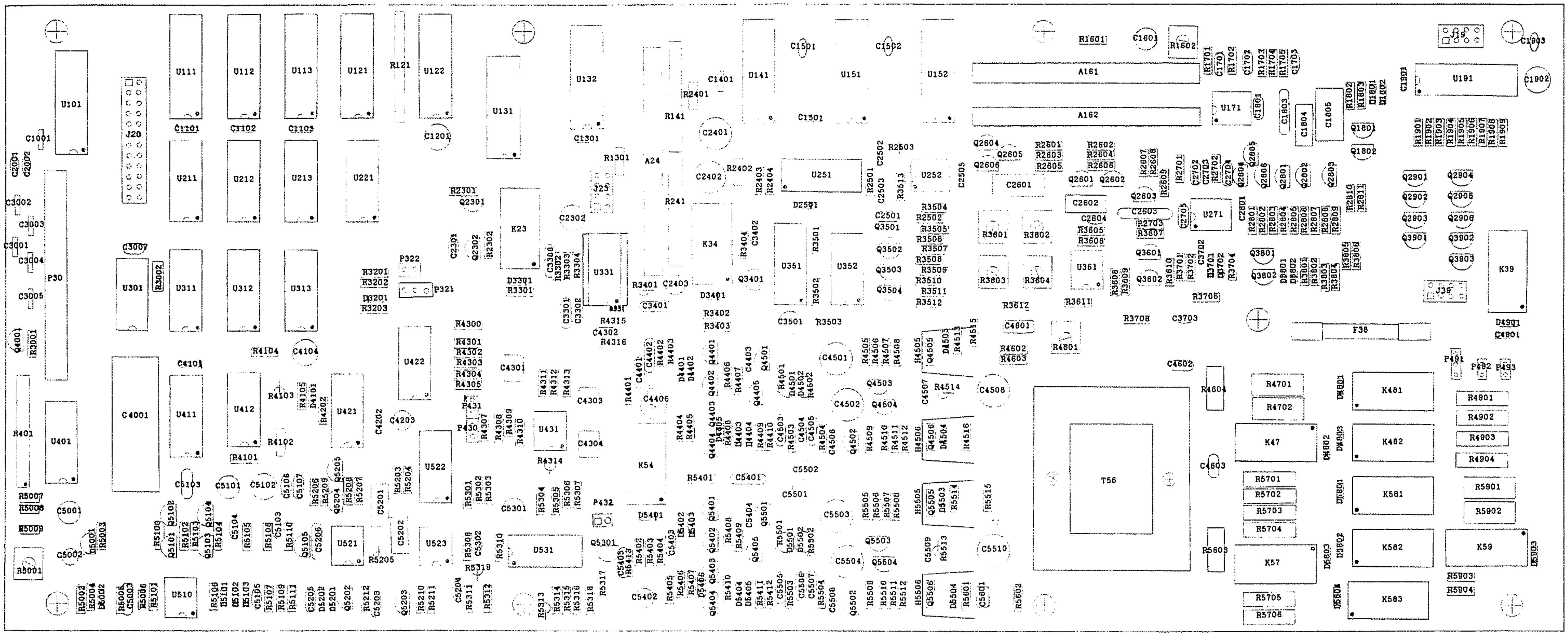
Data is latched by U191 to drive the relays. Resistor, transistor and diode networks (for example R1903-Q2902-D4802) provide the current capability to drive the relays. When a power on reset occurs the output of U191 is shut down via the SAFETY line, tri-stating the outputs and shutting off all relays.



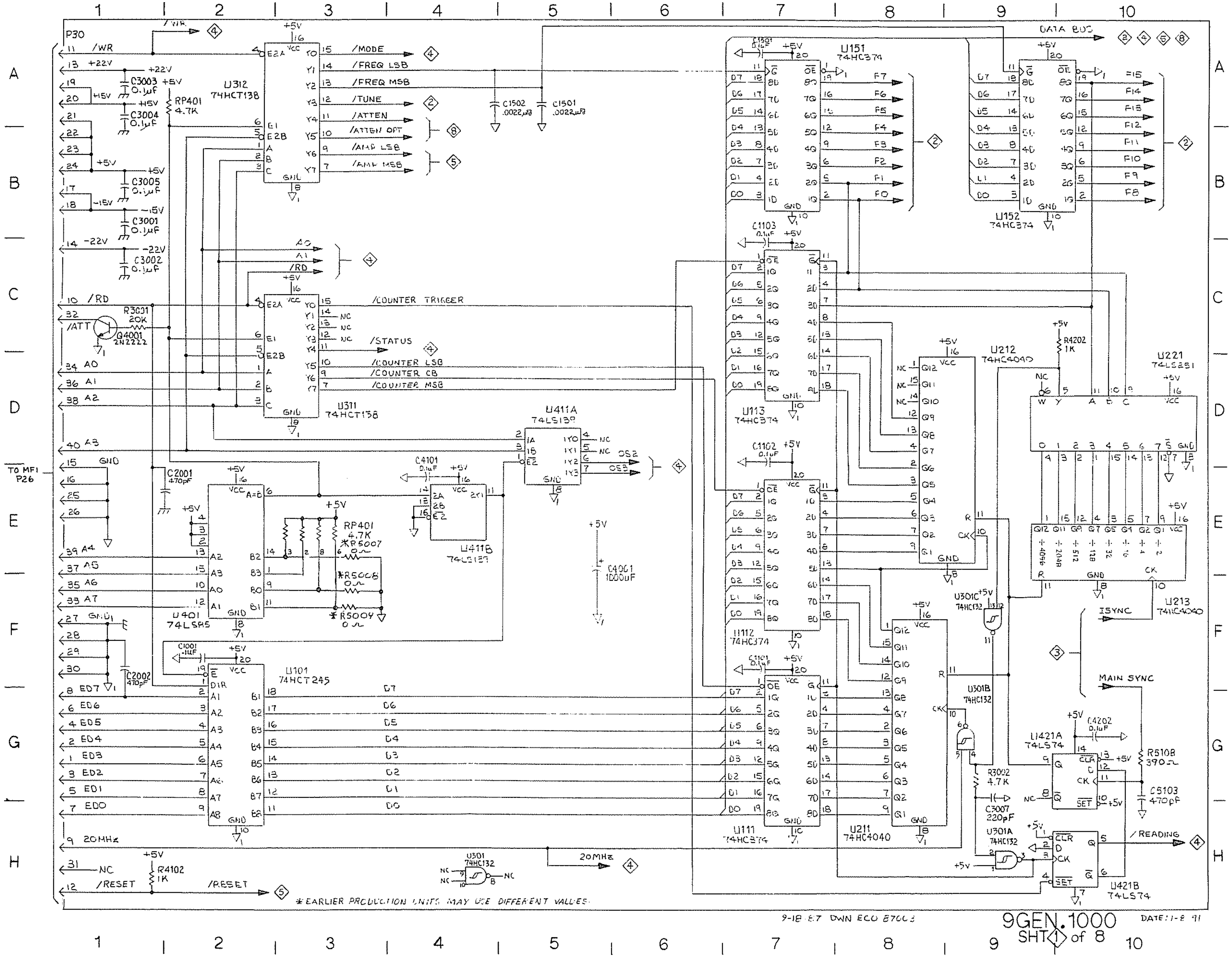
GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)

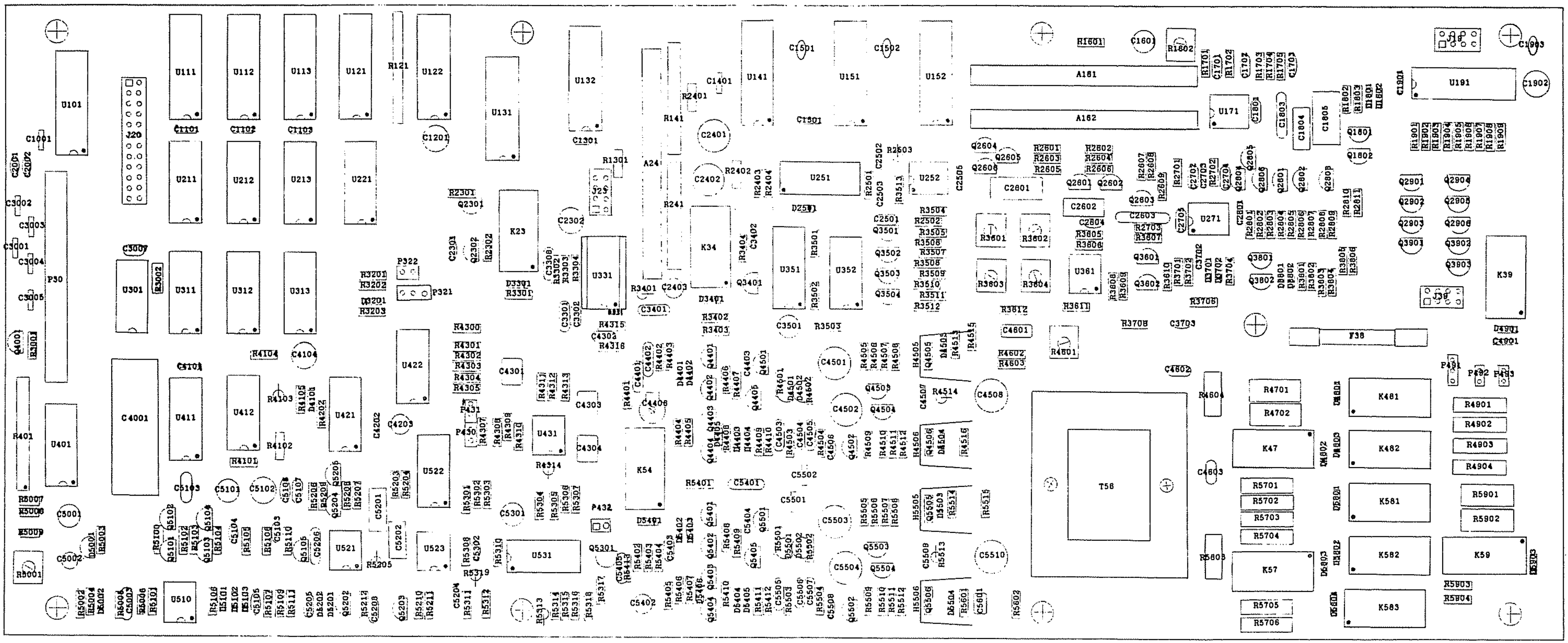


SYNC OUTPUT
MONITOR OUTPUT
TP3401 "MDAC"
INTERMODULATION GENERATOR (J26)
TP250 "0 DEG"
R3601 "100KHz CAL"
R3602 "10KHz CAL"
R3604 "100 Hz CAL"
R1602 "2.1KHz LEVEL"
DUAL OUTPUT OPTION (J39)
DUAL OUTPUT OPTION (J11)
INTERMODULATION GENERATOR (J11)
MAINFRAME INTERFACE (P26)
(NOT USED)
(NOT USED)
R5001 "AMLITUDE"
TP4103 "SYNC"
TP4314 "SERV"
TP5205 "ERROR"
TP5319 "LEVEL"
TP5313 "SPEEDUP"
C4406 "HF FLAT"
TP5513 "-AMP"
TP4514 "+AMP"
R3603 "1KHz CAL"
R4601 "20Hz THD"
LEVEL FREQUENCY MEASUREMENT (P681)
OUTPUT
CPM/GND

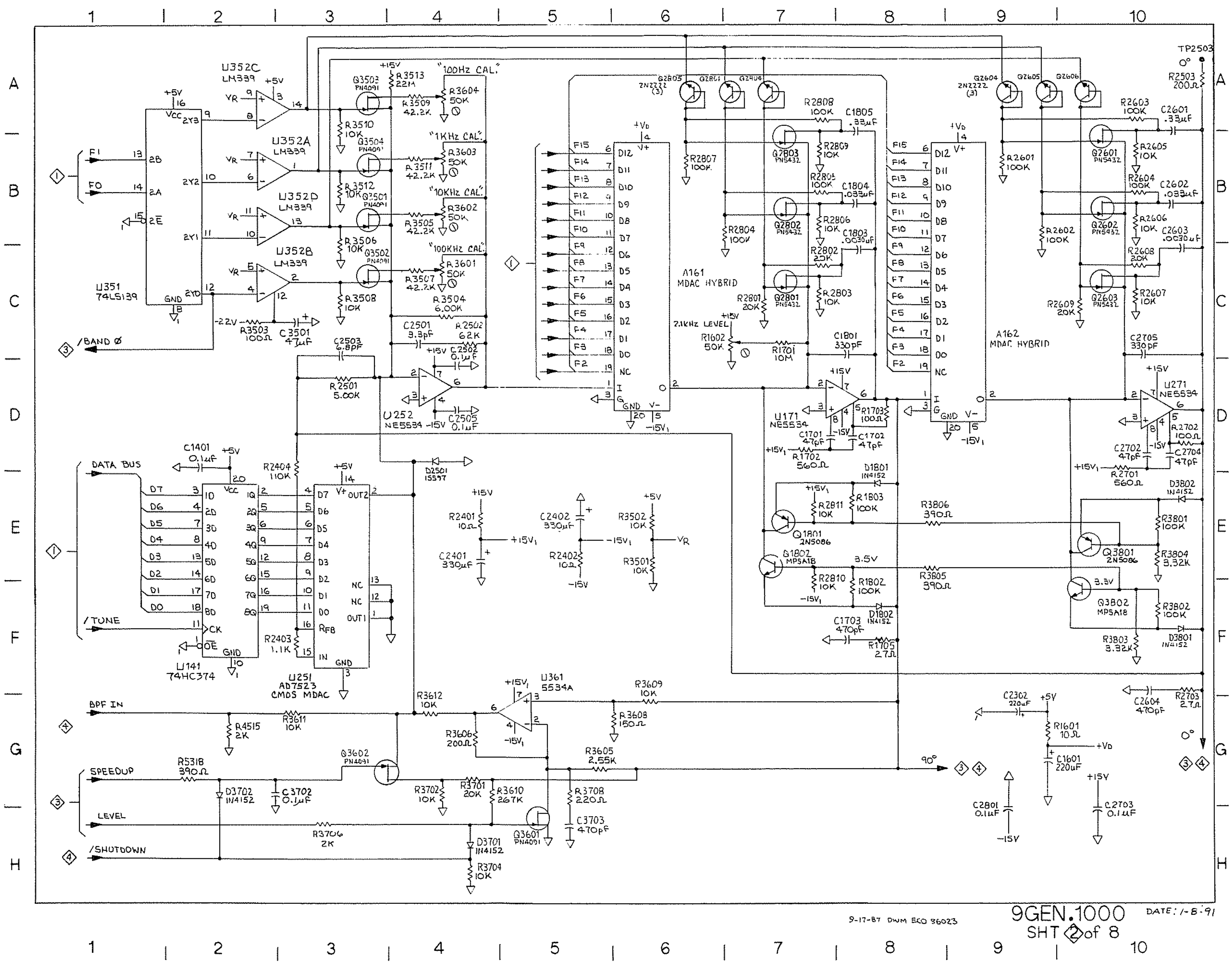


GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)


P30
/WR
+22V
+5V
-15V
-22V
C3003 0.1µF
C3004 0.1µF
C3005 0.1µF
C3001 0.1µF
C3002 0.1µF
RP401 4.7K
U312 74HCT138
/MODE
/FREQ LSB
/FREQ MSB
/TUNE
/ATTEN
/ATTEN OFF
/AMP LSB
/AMP MSB
C1502 .0022µF
C1501 .0022µF
DATA BUS
U151 74HC374
U152 74HC374
F0 F1 F2 F3 F4 F5 F6 F7
F8 F9 F10 F11 F12 F13 F14 F15
A0
A1
/RD
/ATT
R3001 20K
Q4001 2N2222
U311 74HCT138
/COUNTER TRIGGER
/STATUS
/COUNTER LSB
/COUNTER CB
/COUNTER MSB
U113 74HC374
U212 74HC4040
R4202 1K
U221 74LS251
A2
A3
U411A 74LS139
OS2
OS3
TO MF1 P26
GND
C2001 470pF
C4101 0.1µF
U411B 74LS139
C4001 1000µF
A4 A5 A6 A7
U401 74LS85
RP401 4.7K
*R5007 0Ω
*R5008 0Ω
*R5009 0Ω
U112 74HC374
U213 74HC4040
U301C 74HC132
ISYNC
MAIN SYNC
C2002 470pF
C1001 .1µF
U101 74HCT245
ED7 ED6 ED5 ED4 ED3 ED2 ED1 ED0
D7 D6 D5 D4 D3 D2 D1 D0
U111 74HC374
U211 74HC4040
U301B 74HC132
R3002 4.7K
C3007 220pF
U421A 74LS74
C4202 0.1µF
R5108 390Ω
C5103 470pF
U301A 74HC132
/READING
U421B 74LS74
20MHz
R4102 1K
/RESET
U301 74HC132
*EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.
9-18-87 DWN ECO 87003
9GEN.1000
SHT 1 of 8
DATE 11-8-91



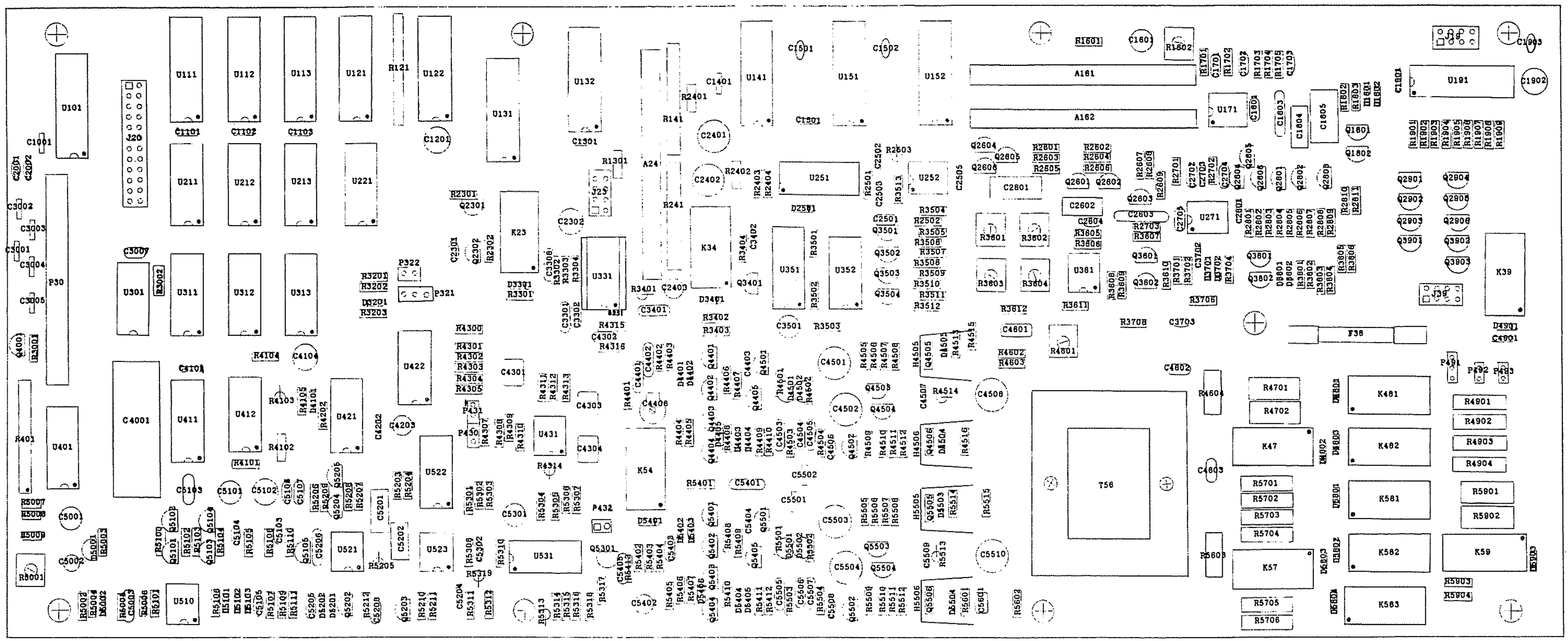
GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)



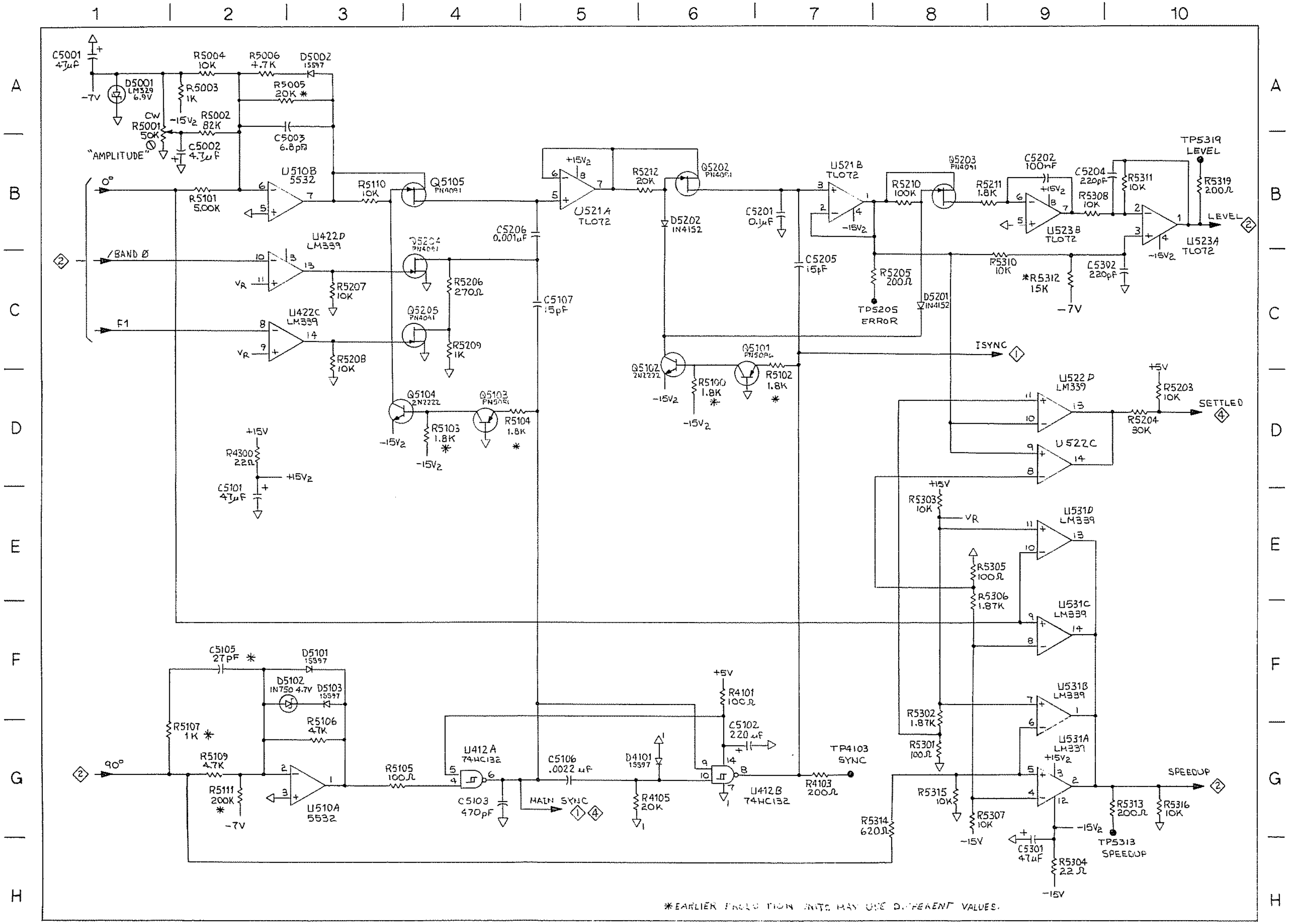
9-17-87 DWM ECO 86023

9GEN.1000 SHT 2 of 8

DATE: 1-8-91



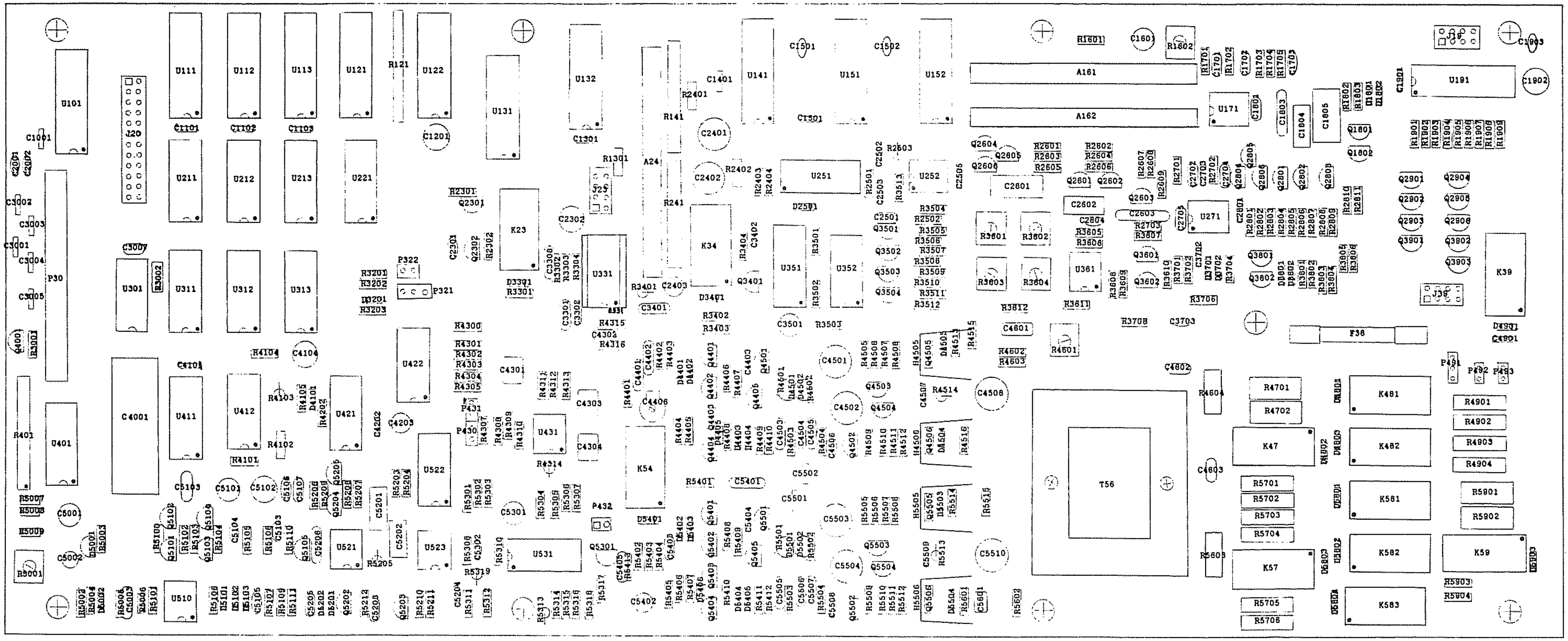
GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)



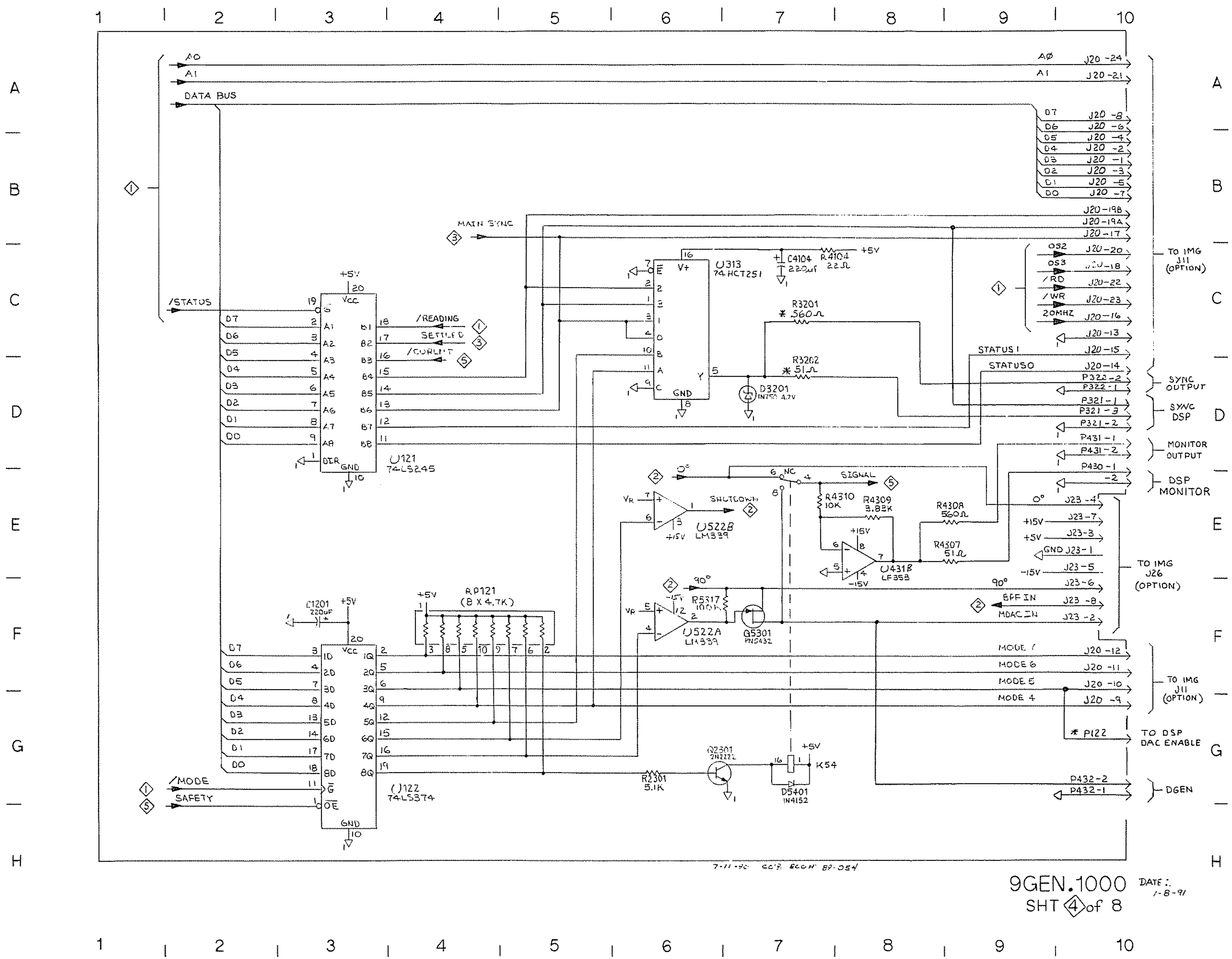
9-17-87 DWM ECO 57004

9GEN.1000 DATE: 1-8-91

SHT 3 of 8

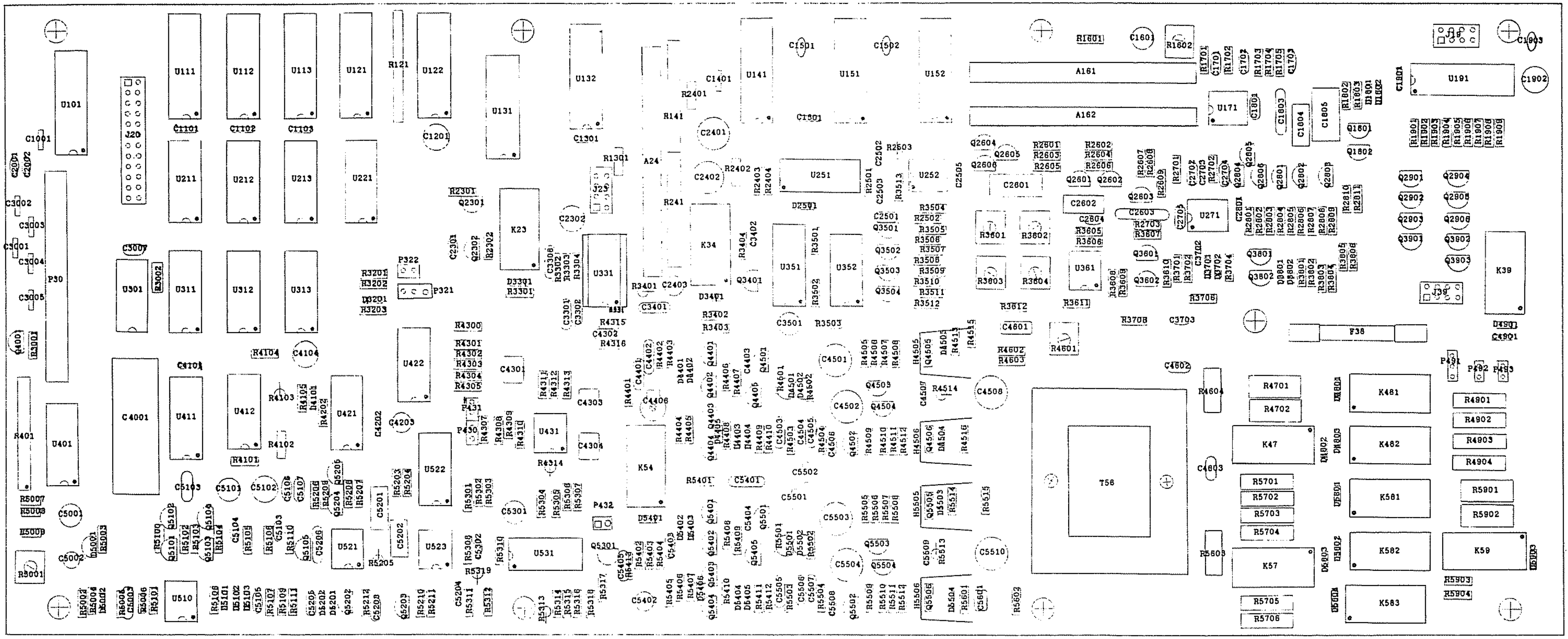


GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)

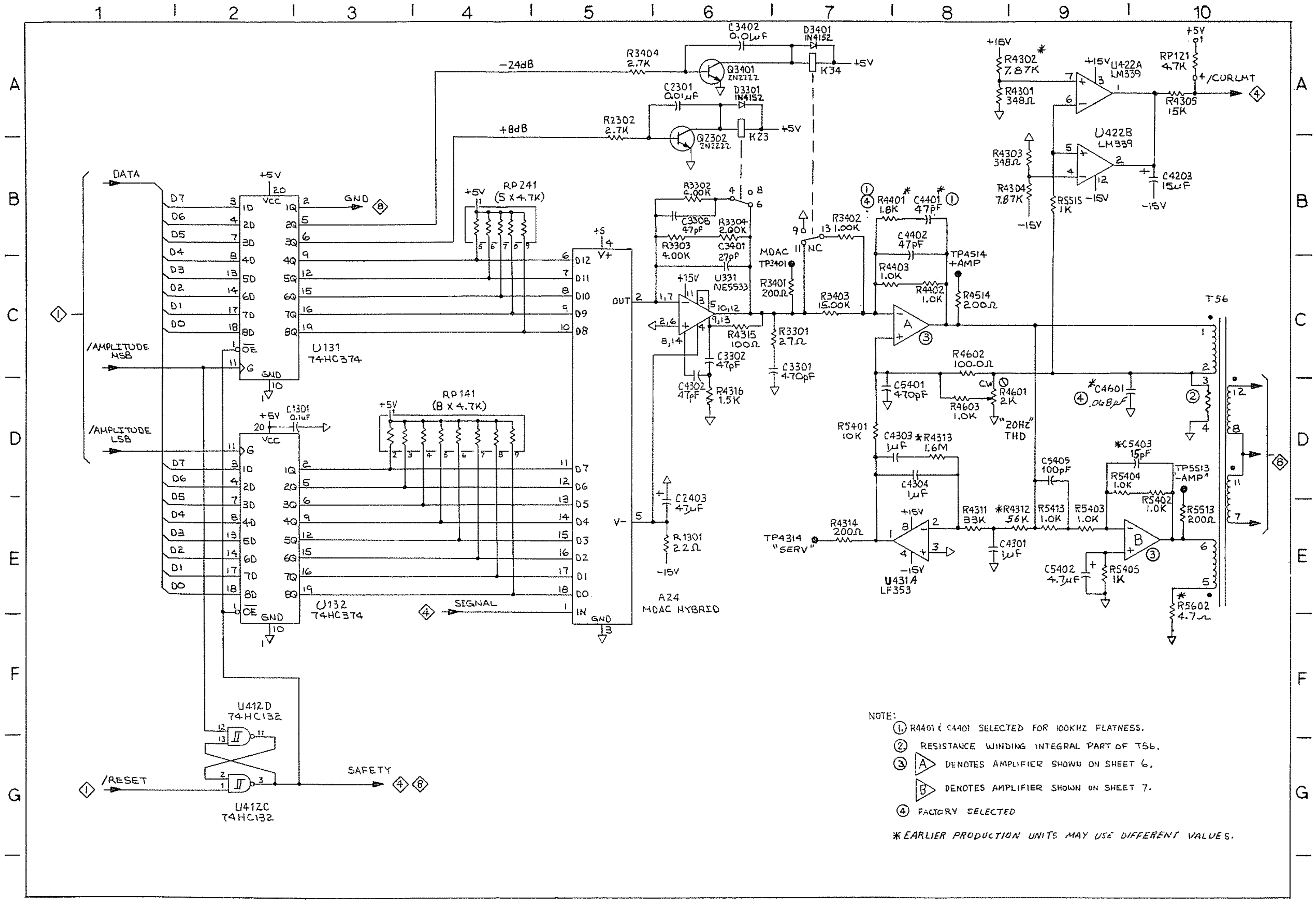


7-11-90 CCB ECO# 89-054

9GEN.1000 DATE: 1-8-91
SHT 4 of 8

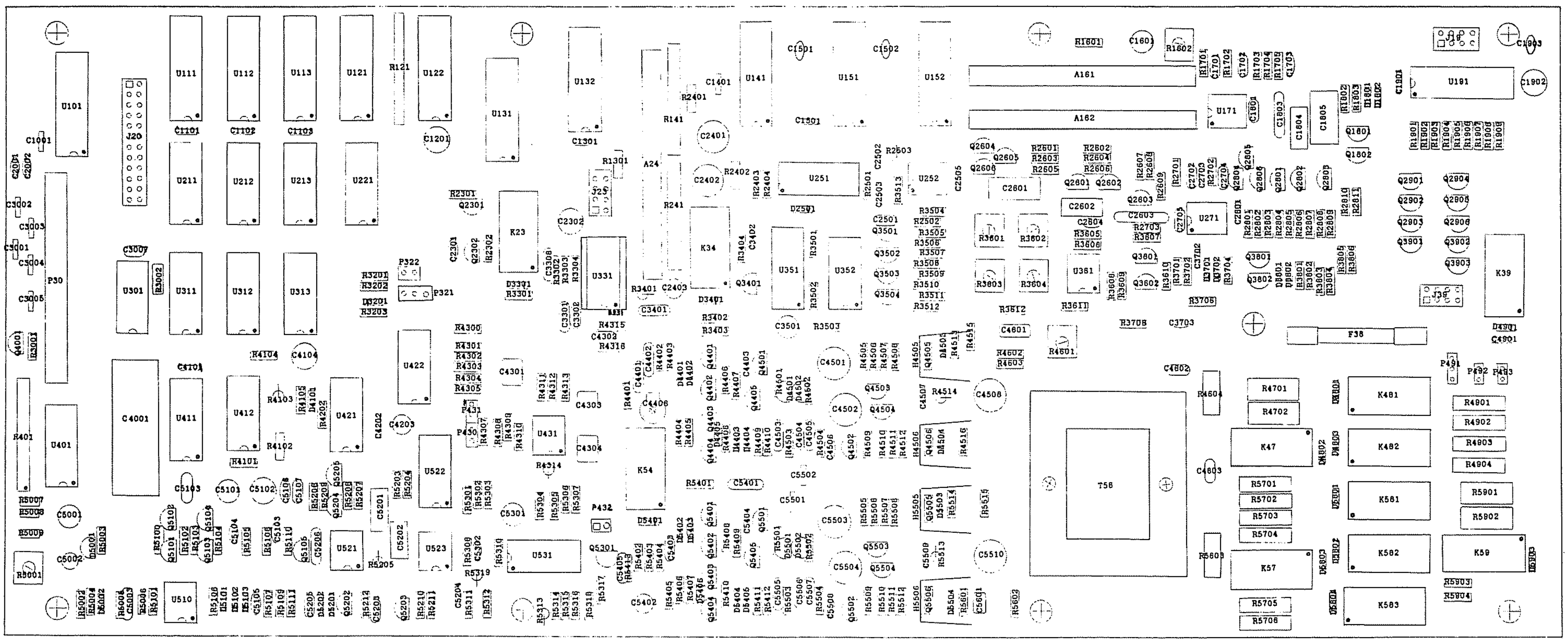


GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)

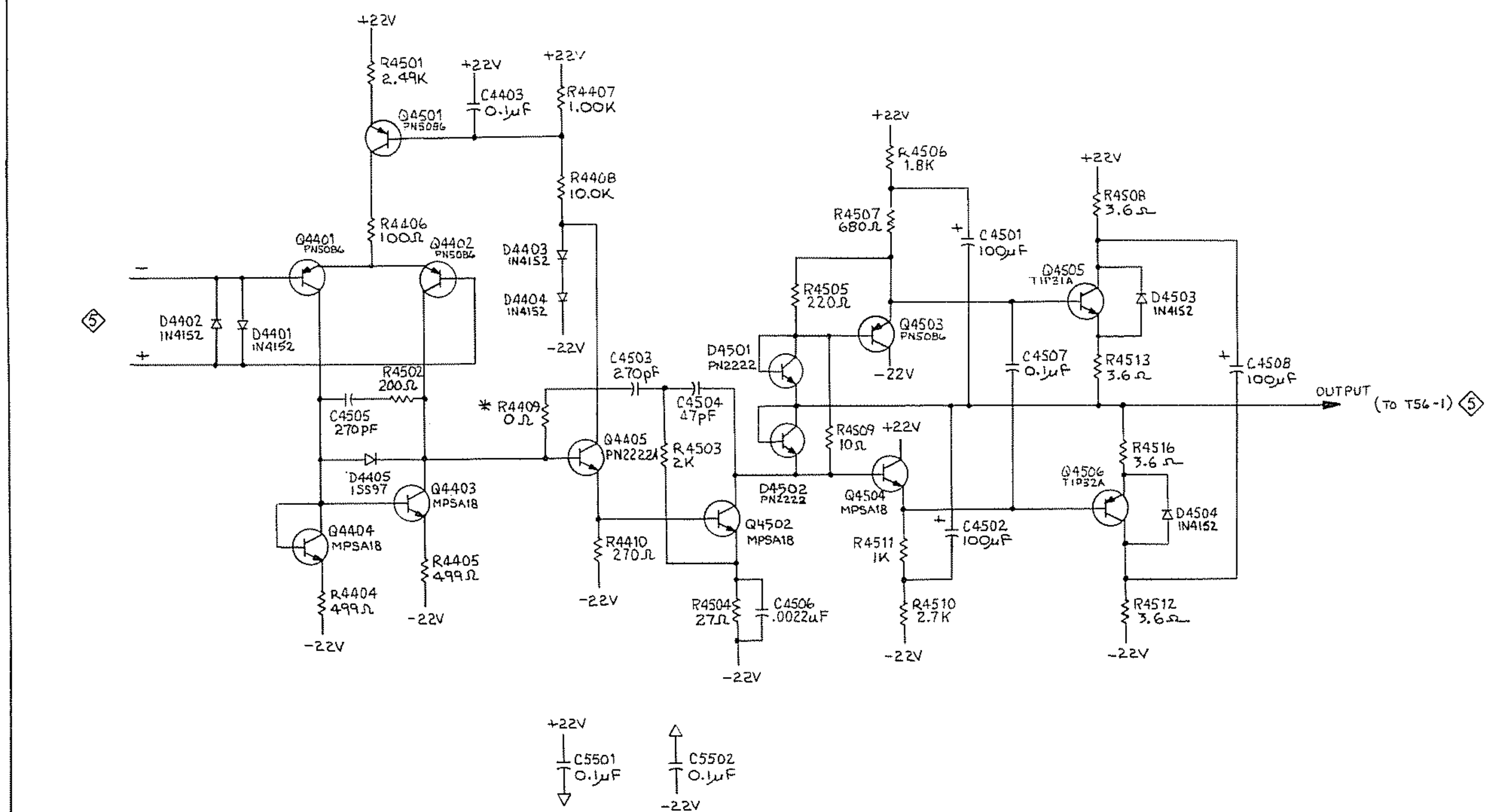


9GEN.1000 DATE: 5-20-92
SHT 5 of 8

7-11-90 CO'B ECO 21033
5-19-92 CJB ECO 16069



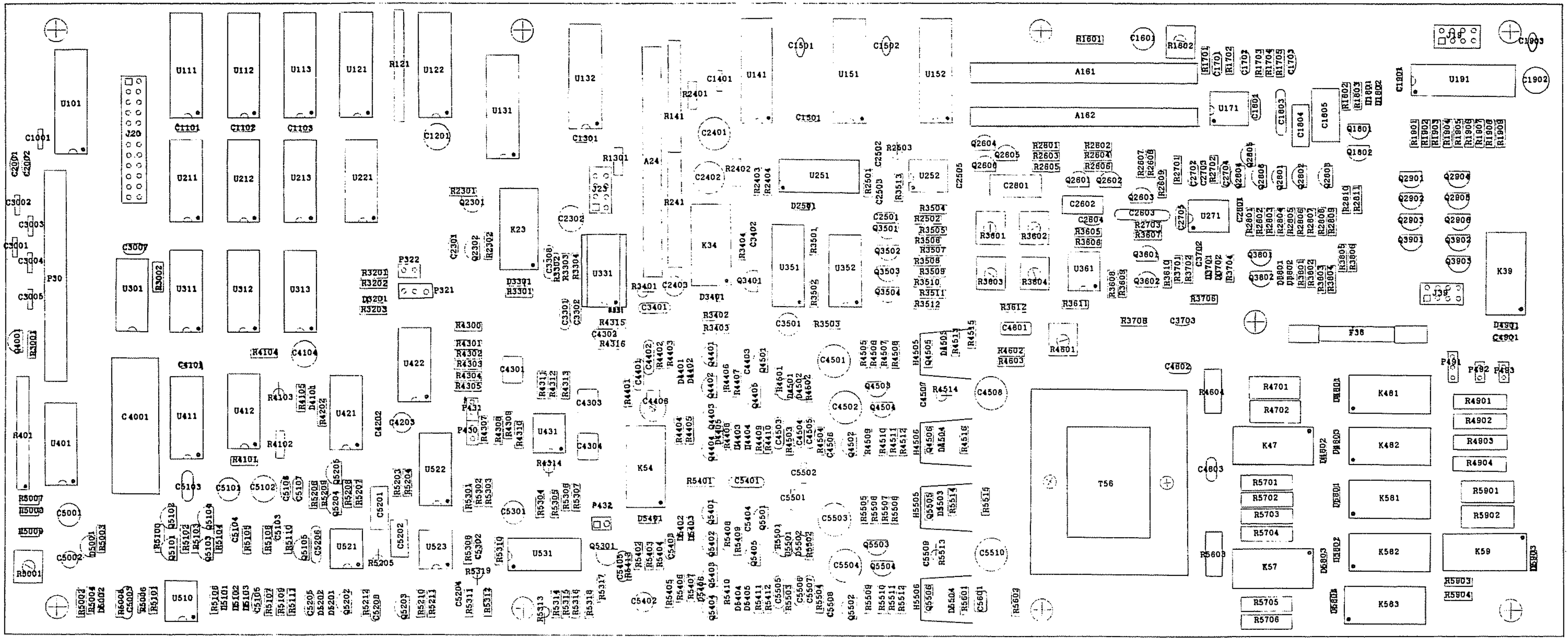
GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)



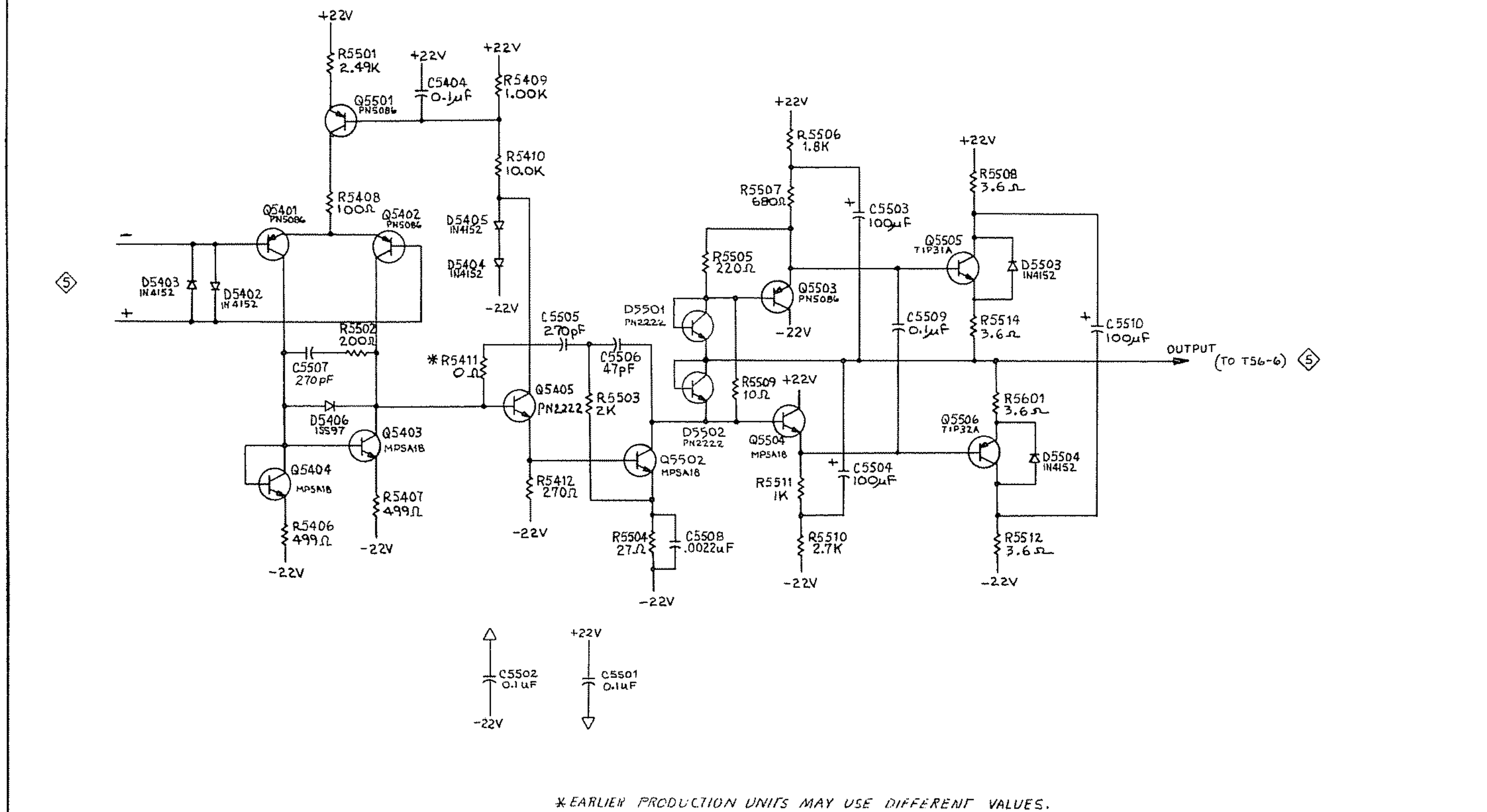
* EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.

9-17-87 DWM ECO 81006
5-19-92 COB ECO 92-009

9GEN.1000
SHT 6 of 8
DATE: 5-20-92

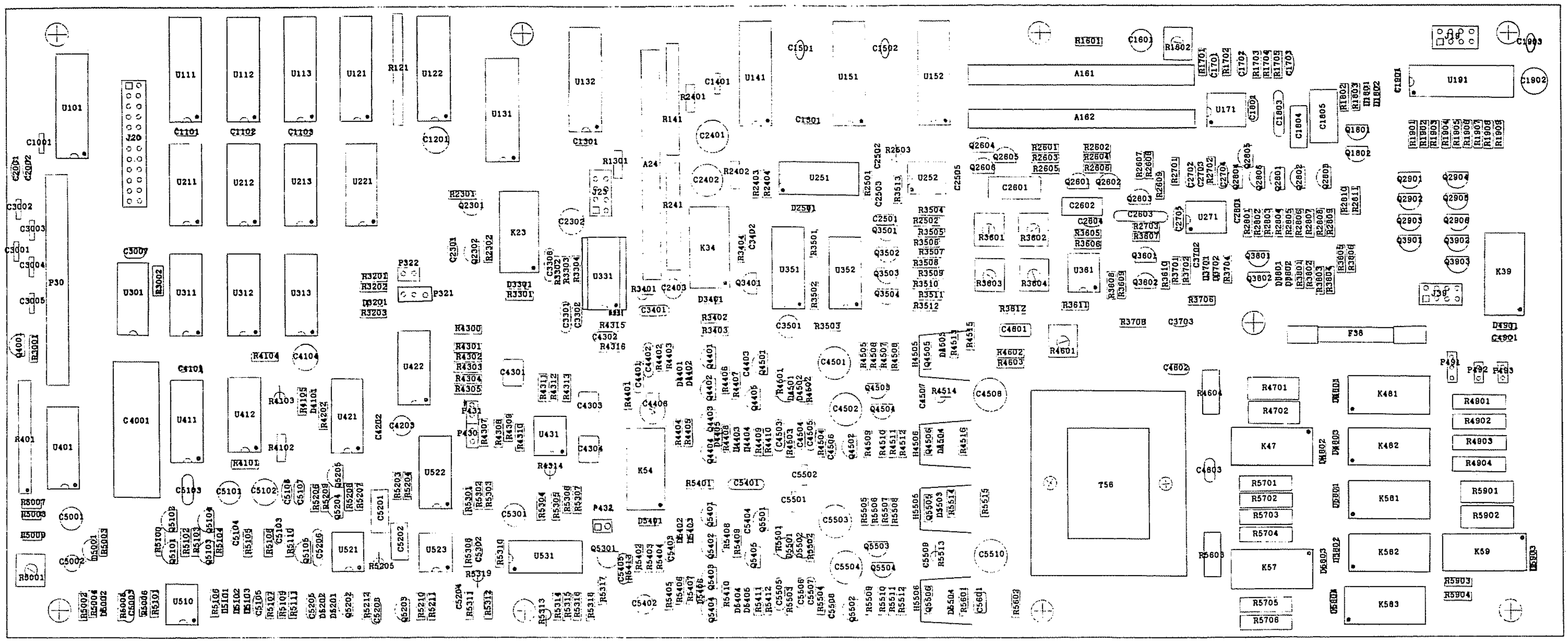


GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)

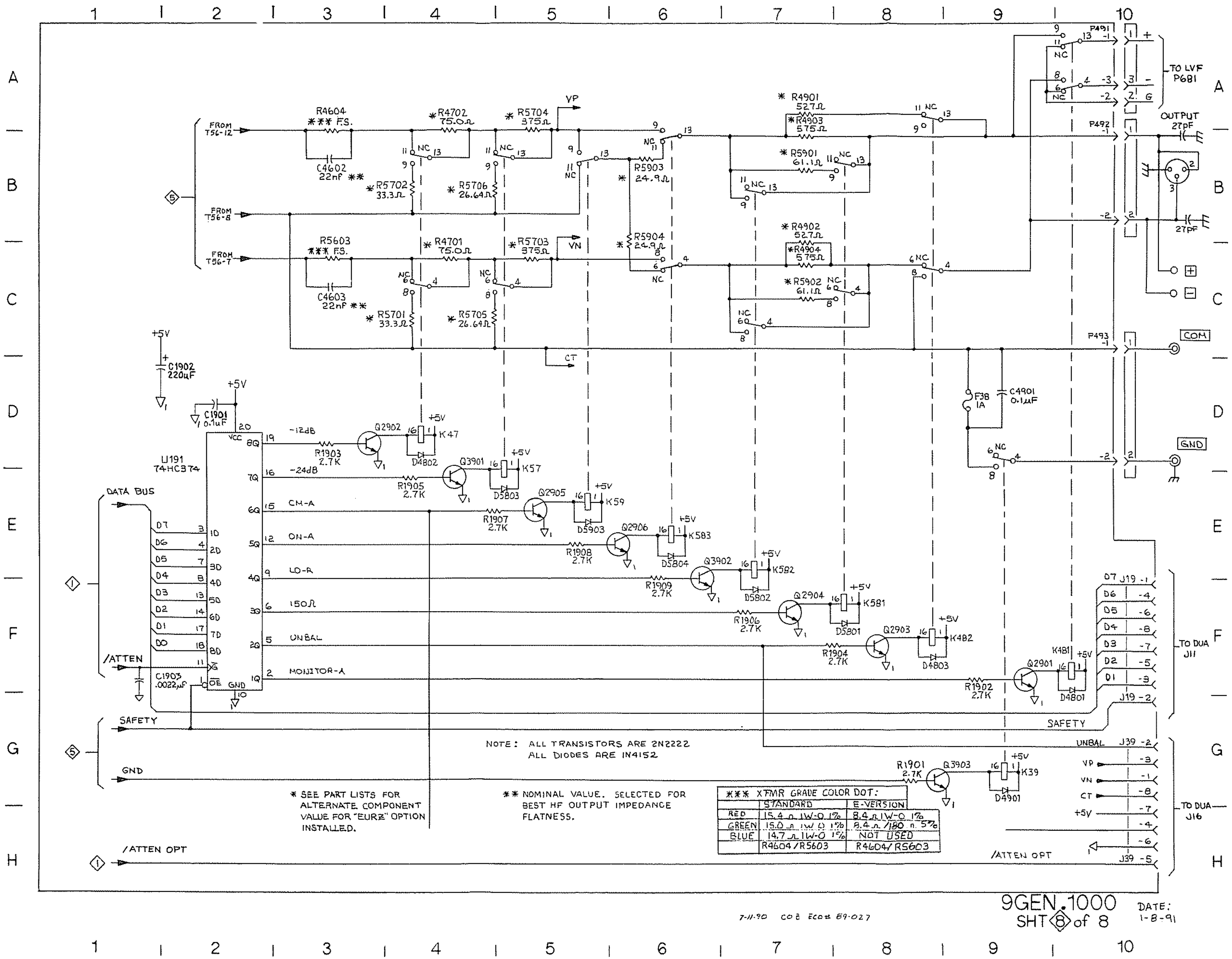


5-19-92 92-009

9GEN.1000
SHT 7 of 8



GENERATOR MODULE 9GEN.1000 (6200.GEN1.5)



9GEN.1000 SHT 8 of 8 DATE: 1-8-91

7-11-90 CO8 ECO# 89-027

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
A161	2B6	9DAC.1000	MDAC ECB ASSEMBLY	
A162	2B9	9DAC.1000	MDAC ECB ASSEMBLY	
A24	5C5	9DAC.1000	MDAC ECB ASSEMBLY	
C1001	1F2	2172.0104	CAP CERAM 100V 20%	.1uF
C1101	1F7	2172.0104	CAP CERAM 100V 20%	.1uF
C1102	1D7	2172.0104	CAP CERAM 100V 20%	.1uF
C1103	1C7	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	4F3	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1301	5D3	2172.0104	CAP CERAM 100V 20%	.1uF
C1401	2D2	2172.0104	CAP CERAM 100V 20%	.1uF
C1501	1A7	2172.0104	CAP CERAM 100V 20%	.1uF
C1502	1A5	2172.0222	CAP CERAM 100V 20%	.0022uF
C1503	1A5	2172.0222	CAP CERAM 100V 20%	.0022uF
C1601	2G9	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1701	2D7	2294.0470	CAP MICA 500V 5%	47pF
C1702	2D8	2294.0470	CAP MICA 500V 5%	47pF
C1703	2F8	2172.0471	CAP CERAM 100V 20%	470pF
C1801	2C8	2296.0331	CAP MICA 500V 1%	330pF
C1803	2C8	2296.0302	CAP MICA 500V 1%	.003uF
C1804	2B8	2675.0333	CAP POLYC 100V 2%	.033uF
C1805	2B8	2675.0334	CAP POLYC 100V 2%	.33uF
C1901	8D2	2172.0104	CAP CERAM 100V 20%	.1uF
C1902	8D1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1903	---	2172.0222	CAP CERAM 100V 20%	.0022uF
C2001	1E2	2172.0471	CAP CERAM 100V 20%	470pF
C2002	1F1	2172.0471	CAP CERAM 100V 20%	470pF
C2301	5A6	2172.0103	CAP CERAM 100V 20%	.01uF
C2302	2G9	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2307	5B6	2294.0270	CAP MICA 500V 5%	27pF
C2401	2E4	2932.0337	CAP AL-EL 25V 20%	330uF
C2402	2E5	2932.0337	CAP AL-EL 25V 20%	330uF
C2403	5E6	2932.0476	CAP AL-EL 25V 20%	47uF
C2501	2C4	2172.0339	CAP CERAM 100V 20%	3.3pF
C2502	2D4	2172.0104	CAP CERAM 100V 20%	.1uF
C2503	2C3	2172.0689	CAP CERAM 100V 20%	6.8pF
C2505	2D4	2172.0104	CAP CERAM 100V 20%	.1uF
C2601	2A10	2675.0334	CAP POLYC 100V 2%	.33uF
C2602	2B10	2675.0333	CAP POLYC 100V 2%	.033uF
C2603	2C10	2296.0302	CAP MICA 500V 1%	.003uF
C2604	2F10	2172.0471	CAP CERAM 100V 20%	470pF
C2702	2D10	2294.0470	CAP MICA 500V 5%	47pF
C2703	2H10	2172.0104	CAP CERAM 100V 20%	.1uF
C2704	2D10	2294.0470	CAP MICA 500V 5%	47pF
C2705	2C10	2296.0331	CAP MICA 500V 1%	330pF
C2801	2H9	2172.0104	CAP CERAM 100V 20%	.1uF
C3001	1B1	2172.0104	CAP CERAM 100V 20%	.1uF
C3002	1C1	2172.0104	CAP CERAM 100V 20%	.1uF
C3003	1A1	2172.0104	CAP CERAM 100V 20%	.1uF
C3004	1A1	2172.0104	CAP CERAM 100V 20%	.1uF
C3005	1B1	2172.0104	CAP CERAM 100V 20%	.1uF
C3007	1G9	2172.0221	CAP CERAM 100V 20%	220pF

REPLACEABLE ELECTRICAL PARTS LIST: 9GEN.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C3301	5C7	2296.0471	CAP MICA 500V 1%	470pF
C3302	5C6	2294.0470	CAP MICA 500V 5%	47pF
C3308	5F6	2294.0470	CAP MICA 500V 5%	47pF
C3401	5G6	2294.0270	CAP MICA 500V 5%	27pF
C3402	5A6	2172.0103	CAP CERAM 100V 20%	.01uF
C3501	2C3	2932.0476	CAP AL-EL 25V 20%	47uF
C3702	2G2	2172.0104	CAP CERAM 100V 20%	.1uF
C3703	2H5	2172.0471	CAP CERAM 100V 20%	470pF
C4001	1E5	2911.0108	CAP AL-EL 10V +80/-20%	1000uF
C4101	1E4	2172.0104	CAP CERAM 100V 20%	.1uF
C4102	3G4	2296.0471	CAP MICA 500V 1%	470pF
C4104	4C7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4202	1G10	2172.0104	CAP CERAM 100V 20%	.1uF
C4203	5B10	2832.0156	CAP TA-EL 25V 20%	15uF
C4301	5E8	2454.0105	CAP POLYE 50V 5%	1uF
C4302	5C6	2294.0470	CAP MICA 500V 5%	47pF
C4303	5D8	2454.0105	CAP POLYE 50V 5%	1uF
C4304	5D8	2454.0105	CAP POLYE 50V 5%	1uF
C4401	5B8	2294.0270	CAP MICA 500V 5%	47pF
C4402	5B8	2294.0470	CAP MICA 500V 5%	47pF
C4403	6C3	2172.0104	CAP CERAM 100V 20%	.1uF
C4501	6D6	2952.0107	CAP AL-EL 50V 20%	100uF
C4502	6E6	2952.0107	CAP AL-EL 50V 20%	100uF
C4503	6D4	2296.0271	CAP MICA 500V 1%	270pF
C4504	6D5	2294.0470	CAP MICA 500V 5%	47pF
C4505	6E3	2296.0271	CAP MICA 500V 1%	270pF
C4506	6F5	2172.0222	CAP CERAM 100V 20%	.0022uF
C4507	6D6	2172.0104	CAP CERAM 100V 20%	.1uF
C4508	6D8	2952.0107	CAP AL-EL 50V 20%	100uF
C4601	5D9	2454.0683	CAP POLYE 50V 5%	.068uF
C4602	8B3	2454.0273	CAP POLYE 50V 5%	.027uF
C4603	8C3	2454.0273	CAP POLYE 50V 5%	.027uF
C46E2	8B3	2454.0563	CAP POLYE 50V 5%	.056uF
C46E3	8C3	2454.0563	CAP POLYE 50V 5%	.056uF
C4901	8D9	2172.0104	CAP CERAM 100V 20%	.1uF
C5001	3A1	2932.0476	CAP AL-EL 25V 20%	47uF
C5002	3B2	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5003	3B3	2172.0689	CAP CERAM 100V 20%	6.8pF
C5101	3E2	2932.0476	CAP AL-EL 25V 20%	47uF
C5102	3G6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5103	1G10	2172.0471	CAP CERAM 100V 20%	470pF
C5105	3F2	2294.0270	CAP MICA 500V 5%	27pF
C5106	3G5	2172.0222	CAP CERAM 100V 20%	.0022uF
C5107	3C5	2294.0150	CAP MICA 500V 5%	15pF
C5201	3B7	2454.0104	CAP POLYE 50V 5%	.1uF
C5202	3B9	2454.0104	CAP POLYE 50V 5%	.1uF
C5204	3B10	2172.0221	CAP CERAM 100V 20%	220pF
C5205	3C7	2294.0150	CAP MICA 500V 5%	15pF
C5206	3B5	2296.0102	CAP MICA 500V 1%	.001uF
C5301	3H9	2932.0476	CAP AL-EL 25V 20%	47uF
C5302	3C10	2172.0221	CAP CERAM 100V 20%	220pF
C5401	5D7	2296.0471	CAP MICA 500V 1%	470pF

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C5402	5E9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5403	5D10	2294.0150	CAP MICA 500V 5%	15pF
C5404	7C3	2172.0104	CAP CERAM 100V 20%	.1uF
C5405	5D9	2296.0101	CAP MICA 500V 1%	100pF
C5501	7G4	2172.0104	CAP CERAM 100V 20%	.1uF
C5502	7G4	2172.0104	CAP CERAM 100V 20%	.1uF
C5503	7D6	2952.0107	CAP AL-EL 50V 20%	100uF
C5504	7E6	2952.0107	CAP AL-EL 50V 20%	100uF
C5505	7D4	2296.0271	CAP MICA 500V 1%	270pF
C5506	7D5	2294.0470	CAP MICA 500V 5%	47pF
C5507	7E4	2296.0271	CAP MICA 500V 1%	270pF
C5508	7F5	2172.0222	CAP CERAM 100V 20%	.0022uF
C5509	7D6	2172.0104	CAP CERAM 100V 20%	.1uF
C5510	7D8	2952.0107	CAP AL-EL 50V 20%	100uF
D1801	2E8	3110.4152	DIODE SIGNAL	4152
D1802	2F8	3110.4152	DIODE SIGNAL	4152
D2501	2D4	3120.0000	DIODE SCHOTTKY	1SS97
D3201	4D7	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D3301	5A6	3110.4152	DIODE SIGNAL	4152
D3401	5A7	3110.4152	DIODE SIGNAL	4152
D3701	2H4	3110.4152	DIODE SIGNAL	4152
D3702	2G2	3110.4152	DIODE SIGNAL	4152
D3801	2F10	3110.4152	DIODE SIGNAL	4152
D3802	2E10	3110.4152	DIODE SIGNAL	4152
D4101	3G6	3120.0000	DIODE SCHOTTKY	1SS97
D4401	6D2	3110.4152	DIODE SIGNAL	4152
D4402	6D2	3110.4152	DIODE SIGNAL	4152
D4403	6D4	3110.4152	DIODE SIGNAL	4152
D4404	6D4	3110.4152	DIODE SIGNAL	4152
D4405	6E3	3120.0000	DIODE SCHOTTKY	1SS97
D4501	6D5	3211.2222	XSTR NPN TO92	PN2222A
D4502	6E5	3211.2222	XSTR NPN TO92	PN2222A
D4503	6D7	3110.4152	DIODE SIGNAL	4152
D4504	6E7	3110.4152	DIODE SIGNAL	4152
D4801	8F10	3110.4152	DIODE SIGNAL	4152
D4802	8D4	3110.4152	DIODE SIGNAL	4152
D4803	8F8	3110.4152	DIODE SIGNAL	4152
D4901	8G9	3110.4152	DIODE SIGNAL	4152
D5001	3A1	3131.0069	DIODE PREC REF ZEN 6.9V	LM329
D5002	3A3	3120.0000	DIODE SCHOTTKY	1SS97
D5101	3F3	3120.0000	DIODE SCHOTTKY	1SS97
D5102	3F2	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D5103	3F3	3120.0000	DIODE SCHOTTKY	1SS97
D5201	3C8	3110.4152	DIODE SIGNAL	4152
D5202	3B6	3110.4152	DIODE SIGNAL	4152
D5401	4G7	3110.4152	DIODE SIGNAL	4152
D5402	7D2	3110.4152	DIODE SIGNAL	4152
D5403	7D2	3110.4152	DIODE SIGNAL	4152
D5404	7D4	3110.4152	DIODE SIGNAL	4152
D5405	7D4	3110.4152	DIODE SIGNAL	4152
D5406	7E3	3120.0000	DIODE SCHOTTKY	1SS97

REPLACEABLE ELECTRICAL PARTS LIST: 9GEN.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION		
D5501	7D5	3211.2222	XSTR NPN TO92		PN2222A
D5502	7E5	3211.2222	XSTR NPN TO92		PN2222A
D5503	7D7	3110.4152	DIODE SIGNAL		4152
D5504	7E7	3110.4152	DIODE SIGNAL		4152
D5801	8F8	3110.4152	DIODE SIGNAL		4152
D5802	8F7	3110.4152	DIODE SIGNAL		4152
D5803	8E5	3110.4152	DIODE SIGNAL		4152
D5804	8E6	3110.4152	DIODE SIGNAL		4152
D5903	8E5	3110.4152	DIODE SIGNAL		4152
E3801	---	4261.0001	FUSE CLIP PC		
E3802	---	4261.0001	FUSE CLIP PC		
F38	8D9	4610.0100	FUSE NORM-BLO 1/4		1A
H4505	---	7210.0001	HEAT SINK PC CLIP		TO220
H4506	---	7210.0001	HEAT SINK PC CLIP		TO220
H5505	---	7210.0001	HEAT SINK PC CLIP		TO220
H5506	---	7210.0001	HEAT SINK PC CLIP		TO220
J19	8F10	4221.1008	JACK PC 2 X .1		8 PIN
J20	4A10	4221.1024	JACK PC 2 X .1		24 PIN
J23	4E10	4221.1008	JACK PC 2 X .1		8 PIN
J39	8G10	4221.1008	JACK PC 2 X .1		8 PIN
K23	5A6	4530.0002	RELAY PC LOW POWER		DPDT
K34	5A7	4530.0002	RELAY PC LOW POWER		DPDT
K39	8G9	4530.0002	RELAY PC LOW POWER		DPDT
K47	8D4	4530.0002	RELAY PC LOW POWER		DPDT
K481	8F10	4530.0002	RELAY PC LOW POWER		DPDT
K482	8F8	4530.0002	RELAY PC LOW POWER		DPDT
K54	4G7	4530.0002	RELAY PC LOW POWER		DPDT
K57	8D5	4530.0002	RELAY PC LOW POWER		DPDT
K581	8F8	4530.0002	RELAY PC LOW POWER		DPDT
K582	8E7	4530.0002	RELAY PC LOW POWER		DPDT
K583	8E6	4530.0002	RELAY PC LOW POWER		DPDT
K59	8E5	4530.0002	RELAY PC LOW POWER		DPDT
P122		4221.0036	PLUG PC	.1 X.43	36 PIN
P30	1A1	4151.1740	CABLE ASSY .05	RBN 17 40 COND	
P321	4D10	4221.0036	PLUG PC	.1 X.43	36 PIN
P322	4D10	4221.0036	PLUG PC	.1 X.43	36 PIN
P430	4D10	4221.0036	PLUG PC	.1 X.43	36 PIN
P431	4D10	4221.0036	PLUG PC	.1 X.43	36 PIN
P432		4221.0036	PLUG PC	.1 X.43	36 PIN
P491	8A10	4221.0036	PLUG PC	.1 X.43	36 PIN
P492	8B10	4221.0036	PLUG PC	.1 X.43	36 PIN
P493	8D10	4221.0036	PLUG PC	.1 X.43	36 PIN
Q1801	2E7	3211.5086	XSTR PNP TO92		PN5086
Q1802	2E7	3211.0018	XSTR NPN TO92		MPSA18
Q2301	4G6	3211.2222	XSTR NPN TO92		PN2222A

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
Q2302	5B6	3211.2222	XSTR NPN TO92	PN2222A
Q2601	2B10	3214.5432	XSTR FET TO92	PN5432
Q2602	2B10	3214.5432	XSTR FET TO92	PN5432
Q2603	2C10	3214.5432	XSTR FET TO92	PN5432
Q2604	2A9	3211.2222	XSTR NPN TO92	PN2222A
Q2605	2A9	3211.2222	XSTR NPN TO92	PN2222A
Q2606	2A10	3211.2222	XSTR NPN TO92	PN2222A
Q2801	2C7	3214.5432	XSTR FET TO92	PN5432
Q2802	2B7	3214.5432	XSTR FET TO92	PN5432
Q2803	2B7	3214.5432	XSTR FET TO92	PN5432
Q2804	2A7	3211.2222	XSTR NPN TO92	PN2222A
Q2805	2A6	3211.2222	XSTR NPN TO92	PN2222A
Q2806	2A7	3211.2222	XSTR NPN TO92	PN2222A
Q2901	8F9	3211.2222	XSTR NPN TO92	PN2222A
Q2902	8D3	3211.2222	XSTR NPN TO92	PN2222A
Q2903	8F8	3211.2222	XSTR NPN TO92	PN2222A
Q2904	8F7	3211.2222	XSTR NPN TO92	PN2222A
Q2905	8E5	3211.2222	XSTR NPN TO92	PN2222A
Q2906	8E6	3211.2222	XSTR NPN TO92	PN2222A
Q3401	5A6	3211.2222	XSTR NPN TO92	PN2222A
Q3501	2B3	3214.4091	XSTR FET TO92	PN4091
Q3502	2C3	3214.4091	XSTR FET TO92	PN4091
Q3503	2A3	3214.4091	XSTR FET TO92	PN4091
Q3504	2B3	3214.4091	XSTR FET TO92	PN4091
Q3601	2H5	3214.4091.H	XSTR FET TO92 HI Vp	PN4091
Q3602	2G3	3214.4091	XSTR FET TO92	PN4091
Q3801	2E10	3211.5086	XSTR PNP TO92	PN5086
Q3802	2F10	3211.0018	XSTR NPN TO92	MPSA18
Q3901	8E4	3211.2222	XSTR NPN TO92	PN2222A
Q3902	8E6	3211.2222	XSTR NPN TO92	PN2222A
Q3903	8G8	3211.2222	XSTR NPN TO92	PN2222A
Q4001	1C1	3211.2222	XSTR NPN TO92	PN2222A
Q4401	6D2	3211.5086	XSTR PNP TO92	PN5086
Q4402	6D3	3211.5086	XSTR PNP TO92	PN5086
Q4403	6E3	3211.0018	XSTR NPN TO92	MPSA18
Q4404	6E2	3211.0018	XSTR NPN TO92	MPSA18
Q4405	6E4	3211.2222	XSTR NPN TO92	PN2222A
Q4501	6C3	3211.5086	XSTR PNP TO92	PN5086
Q4502	6E5	3211.0018	XSTR NPN TO92	MPSA18
Q4503	6D6	3211.5086	XSTR PNP TO92	PN5086
Q4504	6E6	3211.0018	XSTR NPN TO92	MPSA18
Q4505	6D7	3225.0031	XSTR NPN TO220	TIP31C
Q4506	6E7	3225.0032	XSTR PNP TO220	TIP32C
Q5101	3D6	3211.5086	XSTR PNP TO92	PN5086
Q5102	3C6	3211.2222	XSTR NPN TO92	PN2222A
Q5103	3D4	3211.5086	XSTR PNP TO92	PN5086
Q5104	3D4	3211.2222	XSTR NPN TO92	PN2222A
Q5105	3B4	3214.4091	XSTR FET TO92	PN4091
Q5202	3B6	3214.4091	XSTR FET TO92	PN4091
Q5203	3B8	3214.4091	XSTR FET TO92	PN4091
Q5204	3C4	3214.4091	XSTR FET TO92	PN4091
Q5205	3C4	3214.4091	XSTR FET TO92	PN4091

REPLACEABLE ELECTRICAL PARTS LIST: 9GEN.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
Q5301	4F7	3214.5432	XSTR FET TO92	PN5432
Q5401	7D2	3211.5086	XSTR PNP TO92	PN5086
Q5402	7D3	3211.5086	XSTR PNP TO92	PN5086
Q5403	7E3	3211.0018	XSTR NPN TO92	MPSA18
Q5404	7E2	3211.0018	XSTR NPN TO92	MPSA18
Q5405	7E4	3211.2222	XSTR NPN TO92	PN2222A
Q5501	7C3	3211.5086	XSTR PNP TO92	PN5086
Q5502	7E5	3211.0018	XSTR NPN TO92	MPSA18
Q5503	7D6	3211.5086	XSTR PNP TO92	PN5086
Q5504	7E6	3211.0018	XSTR NPN TO92	MPSA18
Q5505	7D7	3225.0031	XSTR NPN TO220	TIP31C
Q5506	7E7	3225.0032	XSTR PNP TO220	TIP32C
R121	4F4,5A10	1984.9472	RES NET SIP 5% B	9 X 4.7K
R1301	5E6	1214.0220	RES 1/4W C FLM 5%	22
R141	5D4	1984.9472	RES NET SIP 5% B	9 X 4.7K
R1601	2G9	1214.0100	RES 1/4W C FLM 5%	10
R1602	2C7	4412.0503	POT TRIM PC ENC	50K
R1701	2C7	1214.0106	RES 1/4W C FLM 5%	10M
R1702	2D7	1214.0561	RES 1/4W C FLM 5%	560
R1703	2D8	1214.0101	RES 1/4W C FLM 5%	100
R1705	2F8	1214.0270	RES 1/4W C FLM 5%	27
R1802	2F8	1214.0104	RES 1/4W/C/FLM 5%	100K
R1803	2E8	1214.0104	RES 1/4W/C/FLM 5%	100K
R1901	8G8	1214.0272	RES 1/4W C FLM 5%	2.7K
R1902	8F9	1214.0272	RES 1/4W C FLM 5%	2.7K
R1903	8D3	1214.0272	RES 1/4W C FLM 5%	2.7K
R1904	8F7	1214.0272	RES 1/4W C FLM 5%	2.7K
R1905	8E4	1214.0272	RES 1/4W C FLM 5%	2.7K
R1906	8F7	1214.0272	RES 1/4W C FLM 5%	2.7K
R1907	8E4	1214.0272	RES 1/4W C FLM 5%	2.7K
R1908	8E5	1214.0272	RES 1/4W C FLM 5%	2.7K
R1909	8E6	1214.0272	RES 1/4W C FLM 5%	2.7K
R2301	4G6	1214.0512	RES 1/4W C FLM 5%	5.1K
R2302	5B5	1214.0272	RES 1/4W C FLM 5%	2.7K
R2401	2E4	1214.0100	RES 1/4W C FLM 5%	10
R2402	2E5	1214.0100	RES 1/4W C FLM 5%	10
R2403	2F3	1136.1101	RES 1/8W M FLM 1%	1.10K
R2404	2D3	1136.1103	RES 1/8W M FLM 1%	110K
R241	5B4	1984.9472	RES NET SIP 5% B	9 X 4.7K
R2501	2D3	1139.5001	RES 1/8W M FLM .1%	5.00K
R2502	2C4	1214.0623	RES 1/4W C FLM 5%	62K
R2503	2A10	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R2601	2B9	1214.0104	RES 1/4W/C/FLM 5%	100K
R2602	2B9	1214.0104	RES 1/4W/C/FLM 5%	100K
R2603	2A10	1214.0104	RES 1/4W/C/FLM 5%	100K
R2604	2B10	1214.0104	RES 1/4W/C/FLM 5%	100K
R2605	2B10	1214.0103	RES 1/4W C FLM 5%	10K
R2606	2B10	1214.0103	RES 1/4W C FLM 5%	10K
R2607	2C10	1214.0103	RES 1/4W C FLM 5%	10K
R2608	2C10	1214.0203	RES 1/4W C FLM 5%	20K
R2609	2C10	1214.0203	RES 1/4W C FLM 5%	20K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R2701	2D10	1214.0561	RES 1/4W C FLM 5%	560
R2702	2D10	1214.0101	RES 1/4W C FLM 5%	100
R2703	2F10	1214.0270	RES 1/4W C FLM 5%	27
R2801	2C7	1214.0203	RES 1/4W C FLM 5%	20K
R2802	2C7	1214.0203	RES 1/4W C FLM 5%	20K
R2803	2C7	1214.0103	RES 1/4W C FLM 5%	10K
R2804	2B7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2805	2B7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2806	2B7	1214.0103	RES 1/4W C FLM 5%	10K
R2807	2B6	1214.0104	RES 1/4W/C/FLM 5%	100K
R2808	2A7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2809	2B7	1214.0103	RES 1/4W C FLM 5%	10K
R2810	2E7	1136.1002	RES 1/8W M FLM 1%	10.0K
R2811	2E7	1136.1002	RES 1/8W M FLM 1%	10.0K
R3001	1C1	1214.0203	RES 1/4W C FLM 5%	20K
R3002	1G9	1214.0472	RES 1/4W C FLM 5%	4.7K
R3201	4C7	1214.0561	RES 1/4W C FLM 5%	560
R3202	4D7	1214.0510	RES 1/4W C FLM 5%	51
R3301	5C7	1214.0270	RES 1/4W C FLM 5%	27
R3302	5B6	1139.4001	RES 1/8W M FLM .1%	4.00K
R3303	5B6	1139.4001	RES 1/8W M FLM .1%	4.00K
R3304	5B6	1139.2001	RES 1/8W M FLM .1%	2.00K
R3401	5C7	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R3402	5B7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3403	5C7	1139.1502	RES 1/8W M FLM .1%	15.0K
R3404	5A5	1214.0272	RES 1/4W C FLM 5%	2.7K
R3501	2E6	1214.0103	RES 1/4W C FLM 5%	10K
R3502	2E6	1214.0103	RES 1/4W C FLM 5%	10K
R3503	2C2	1214.0101	RES 1/4W C FLM 5%	100
R3504	2C4	1139.6001	RES 1/8W M FLM .1%	6.00K
R3505	2B4	1136.4222	RES 1/8W M FLM 1%	42.2K
R3506	2B3	1214.0103	RES 1/4W C FLM 5%	10K
R3507	2C4	1136.4222	RES 1/8W M FLM 1%	42.2K
R3508	2C3	1214.0103	RES 1/4W C FLM 5%	10K
R3509	2A4	1136.4222	RES 1/8W M FLM 1%	42.2K
R3510	2A3	1214.0103	RES 1/4W C FLM 5%	10K
R3511	2B4	1136.4222	RES 1/8W M FLM 1%	42.2K
R3512	2B3	1214.0103	RES 1/4W C FLM 5%	10K
R3513	2A4	1214.0226	RES 1/4W C FLM 5%	22M
R3601	2C4	4412.0503	POT TRIM PC ENC	50K
R3602	2B4	4412.0503	POT TRIM PC ENC	50K
R3603	2B4	4412.0503	POT TRIM PC ENC	50K
R3604	2A4	4412.0503	POT TRIM PC ENC	50K
R3605	2G5	1136.2551	RES 1/8W M FLM 1%	2.55K
R3606	2G4	1136.2000	RES 1/8W M FLM 1%	200
R3608	2G6	1136.1500	RES 1/8W M FLM 1%	150
R3609	2G6	1136.1002	RES 1/8W M FLM 1%	10.0K
R3610	2G4	1136.2673	RES 1/8W M FLM 1%	267K
R3611	2G3	1136.1002	RES 1/8W M FLM 1%	10.0K
R3612	2G4	1136.1002	RES 1/8W M FLM 1%	10.0K
R3701	2G4	1214.0203	RES 1/4W C FLM 5%	20K
R3702	2G4	1214.0103	RES 1/4W C FLM 5%	10K

REPLACEABLE ELECTRICAL PARTS LIST: 9GEN.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R3704	2H4	1214.0103	RES 1/4W C FLM 5%	10K
R3706	2H3	1139.2001	RES 1/8W M FLM .1%	2.00K
R3708	2G5	1214.0221	RES 1/4W C FLM 5%	220
R3801	2E10	1214.0104	RES 1/4W/C/FLM 5%	100K
R3802	2F10	1214.0104	RES 1/4W/C/FLM 5%	100K
R3803	2F10	1136.3321	RES 1/8W M FLM 1%	3.32K
R3804	2E10	1136.3321	RES 1/8W M FLM 1%	3.32K
R3805	2E8	1214.0391	RES 1/4W C FLM 5%	390
R3806	2E8	1214.0391	RES 1/4W C FLM 5%	390
R401	1A2,1E3	1984.9472	RES NET SIP 5% B	9 X 4.7K
R4101	3F6	1214.0101	RES 1/4W C FLM 5%	100
R4102	1H1	1214.0102	RES 1/4W C FLM 5%	1K
R4103	3G7	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4104	4C7	1214.0220	RES 1/4W C FLM 5%	22
R4105	3G5	1214.0203	RES 1/4W C FLM 5%	20K
R4202	1C9	1214.0102	RES 1/4W C FLM 5%	1K
R4300	3D2	1214.0220	RES 1/4W C FLM 5%	22
R4301	5A8	1136.3480	RES 1/8W M FLM 1%	348
R4302	5A8	1136.7871	RES 1/8W M FLM 1%	7.87K
R4303	5B9	1136.3480	RES 1/8W M FLM 1%	348
R4304	5B9	1136.1002	RES 1/8W M FLM 1%	7.87K
R4305	5A10	1214.0153	RES 1/4W C FLM 5%	15K
R4307	4E9	1214.0510	RES 1/4W C FLM 5%	51
R4308	4E9	1214.0561	RES 1/4W C FLM 5%	560
R4309	4E8	1136.3831	RES 1/8W M FLM 1%	3.83K
R4310	4E7	1136.1002	RES 1/8W M FLM 1%	10.0K
R4311	5E8	1214.0333	RES 1/4W C FLM 5%	33K
R4312	5E9	1214.0563	RES 1/4W C FLM 5%	56K
R4313	5D8	1214.0165	RES 1/4W C FLM 5%	1.6M
R4314	5E7	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4315	5C6	1214.0101	RES 1/4W C FLM 5%	100
R4316	5D6	1214.0152	RES 1/4W C FLM 5%	1.5K
R4401	5C8	1214.0182	RES 1/4W C FLM 5%	1.8K
R4402	5C8	1139.1001	RES 1/8W M FLM .1%	1.00K
R4403	5C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R4404	6F3	1136.4990	RES 1/8W M FLM 1%	499
R4405	6F3	1136.4990	RES 1/8W M FLM 1%	499
R4406	6D3	1214.0101	RES 1/4W C FLM 5%	100
R4407	6C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R4408	6C4	1136.1002	RES 1/8W M FLM 1%	10.0K
R4409	6E4	1214.0510	RES 1/4W C FLM 5%	0
R4410	6E4	1214.0271	RES 1/4W C FLM 5%	270
R4501	6C3	1136.2491	RES 1/8W M FLM 1%	2.49K
R4502	6E3	1214.0201	RES 1/4W C FLM 5%	200
R4503	6E4	1214.0202	RES 1/4W C FLM 5%	2.0K
R4504	6F5	1214.0270	RES 1/4W C FLM 5%	27
R4505	6D5	1214.0221	RES 1/4W C FLM 5%	220
R4506	6C6	1214.0182	RES 1/4W C FLM 5%	1.8K
R4507	6D6	1214.0681	RES 1/4W C FLM 5%	680
R4508	6C7	1214.0369	RES 1/4W C FLM 5%	3.6
R4509	6E5	1214.0100	RES 1/4W C FLM 5%	10
R4510	6F6	1214.0272	RES 1/4W C FLM 5%	2.7K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4511	6E6	1214.0102	RES 1/4W C FLM 5%	1K
R4512	6F7	1214.0369	RES 1/4W C FLM 5%	3.6
R4513	6D7	1214.0369	RES 1/4W C FLM 5%	3.6
R4514	5C8	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4515	2G2	1214.0202	RES 1/4W C FLM 5%	2.0K
R4516	6E7	1214.0369	RES 1/4W C FLM 5%	3.6
R4601	5D8	4412.0202	POT TRIM PC ENC	2K
R4602	5C8	1136.1000	RES 1/8W M FLM 1%	100
R4603	5D8	1139.1001	RES 1/8W M FLM .1%	1.00K
R4604	8B3	1456.1509	RES 1W W WND 1%	15.0
R46E4	8B3	1336.8008	RES 1/2W M FLM 1%	8.0
R46E5		1214.0161	RES 1/4W C FLM 5%	160
R4701	8C4	1339.7509	RES 1/2W M FLM .1%	75.0
R4702	8A4	1339.7509	RES 1/2W M FLM .1%	75.0
R47E1	8C4	1339.5409	RES 1/2W M FLM .1%	54.0
R47E2	8A4	1339.5409	RES 1/2W M FLM .1%	54.0
R4901	8A7	1239.5270	RES 1/4W M FLM .1%	527
R4902	8B7	1239.5270	RES 1/4W M FLM .1%	527
R4903	8B7	1239.5750	RES 1/4W M FLM .1%	575
R4904	8C7	1239.5750	RES 1/4W M FLM .1%	575
R49E1	8A7	1239.5470	RES 1/4W M FLM .1%	547.1
R49E2	8B7	1239.5470	RES 1/4W M FLM .1%	547.1
R49E3	8B7	1239.5820	RES 1/4W M FLM .1%	582
R49E4	8C7	1239.5820	RES 1/4W M FLM .1%	582
R5001	3A1	4412.0503	POT TRIM PC ENC	50K
R5002	3A2	1214.0823	RES 1/4W C FLM 5%	82K
R5003	3A2	1214.0102	RES 1/4W C FLM 5%	1K
R5004	3A2	1136.1002	RES 1/8W M FLM 1%	10.0K
R5005	3A3	1214.0203	RES 1/4W C FLM 5%	20K
R5006	3A2	1214.0472	RES 1/4W C FLM 5%	4.7K
R5007	1E3	1214.0000	JUMPER .4 X.25	00
R5008	1F3	1214.0000	JUMPER .4 X.25	00
R5009	1F3	1214.0000	JUMPER .4 X.25	00
R5100	3D6	1214.0182	RES 1/4W C FLM 5%	1.8K
R5101	3B2	1139.5001	RES 1/8W M FLM .1%	5.00K
R5102	3C7	1214.0182	RES 1/4W C FLM 5%	1.8K
R5103	3D4	1214.0182	RES 1/4W C FLM 5%	1.8K
R5104	3D4	1214.0182	RES 1/4W C FLM 5%	1.8K
R5105	3G3	1214.0101	RES 1/4W C FLM 5%	100
R5106	3G3	1214.0473	RES 1/4W C FLM 5%	47K
R5107	3G1	1214.0102	RES 1/4W C FLM 5%	1K
R5108	1G10	1214.0391	RES 1/4W C FLM 5%	390
R5109	3G2	1214.0472	RES 1/4W C FLM 5%	4.7K
R5110	3B3	1214.0103	RES 1/4W C FLM 5%	10K
R5111	3G2	1214.0204	RES 1/4W C FLM 5%	200K
R5203	3D10	1214.0103	RES 1/4W C FLM 5%	10K
R5204	3D10	1214.0303	RES 1/4W C FLM 5%	30K
R5205	3C7	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R5206	3C4	1214.0271	RES 1/4W C FLM 5%	270
R5207	3C3	1214.0103	RES 1/4W C FLM 5%	10K
R5208	3C3	1214.0103	RES 1/4W C FLM 5%	10K
R5209	3C4	1214.0102	RES 1/4W C FLM 5%	1K

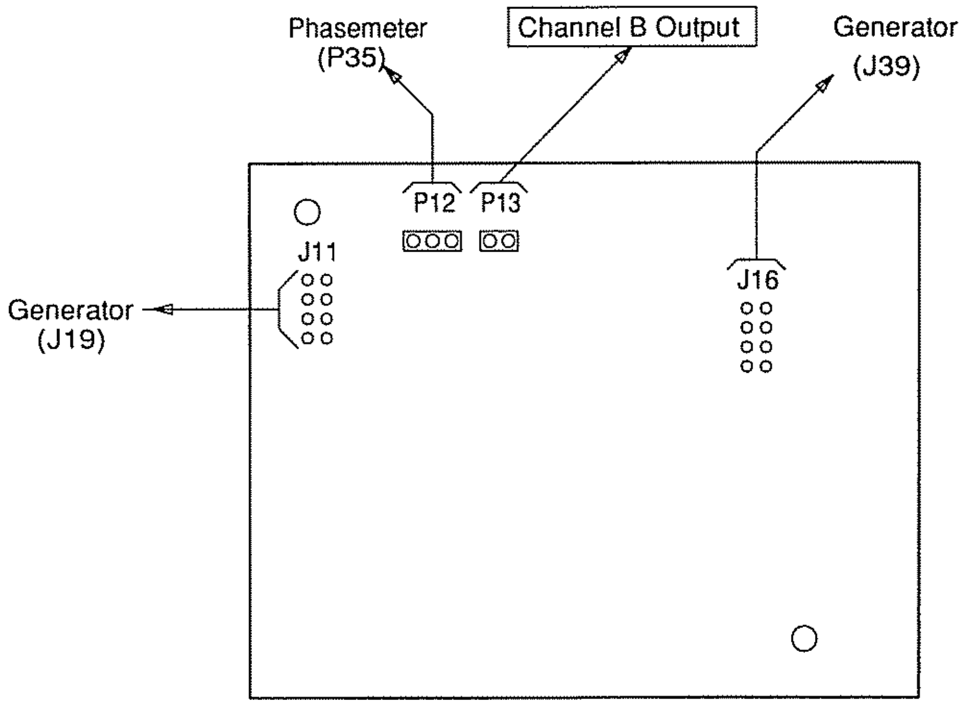
REPLACEABLE ELECTRICAL PARTS LIST: 9GEN.1000

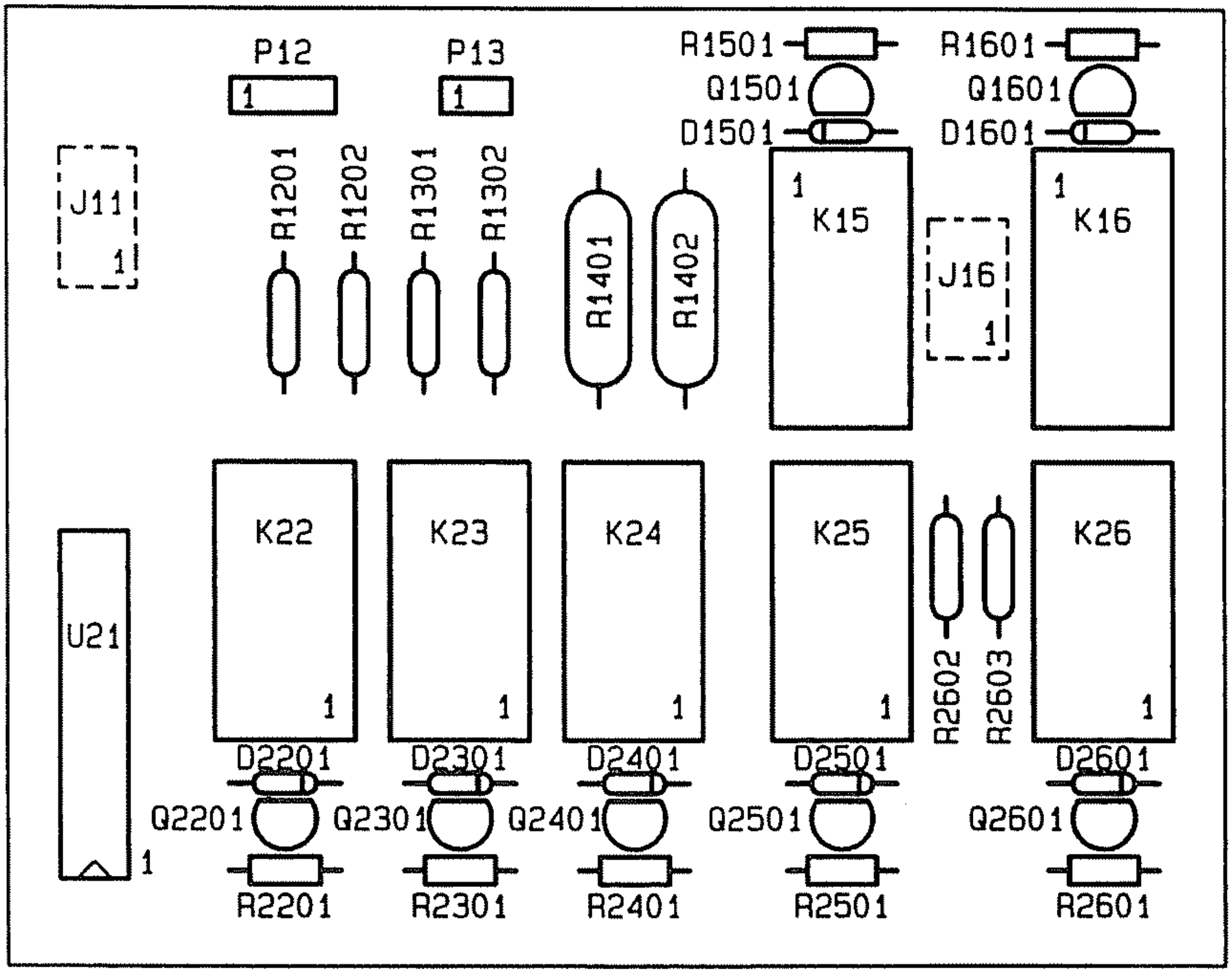
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R5210	3B8	1214.0104	RES 1/4W/C/FLM 5%	100K
R5211	3B8	1214.0182	RES 1/4W C FLM 5%	1.8K
R5212	3B6	1214.0203	RES 1/4W C FLM 5%	20K
R5301	3G8	1214.0101	RES 1/4W C FLM 5%	100
R5302	3F8	1136.1871	RES 1/8W M FLM 1%	1.87K
R5303	3E8	1136.1002	RES 1/8W M FLM 1%	10.0K
R5304	3H9	1214.0220	RES 1/4W C FLM 5%	22
R5305	3E8	1214.0101	RES 1/4W C FLM 5%	100
R5306	3F8	1136.1871	RES 1/8W M FLM 1%	1.87K
R5307	3G8	1136.1002	RES 1/8W M FLM 1%	10.0K
R5308	3B9	1214.0103	RES 1/4W C FLM 5%	10K
R5310	3C9	1214.0103	RES 1/4W C FLM 5%	10K
R5311	3B10	1214.0103	RES 1/4W C FLM 5%	10K
R5312	3C9	1214.0153	RES 1/4W C FLM 5%	15K
R5313	3G10	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R5314	3G7	1214.0621	RES 1/4W C FLM 5%	620
R5315	3G8	1214.0103	RES 1/4W C FLM 5%	10K
R5316	3G10	1214.0103	RES 1/4W C FLM 5%	10K
R5317	4F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5318	2G2	1214.0391	RES 1/4W C FLM 5%	390
R5319	3B10	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R5401	5D7	1214.0103	RES 1/4W C FLM 5%	10K
R5402	5D10	1139.1001	RES 1/8W M FLM .1%	1.00K
R5403	5E9	1139.1001	RES 1/8W M FLM .1%	1.00K
R5404	5D9	1139.1001	RES 1/8W M FLM .1%	1.00K
R5405	5E9	1214.0102	RES 1/4W C FLM 5%	1K
R5406	7F3	1136.4990	RES 1/8W M FLM 1%	499
R5407	7F3	1136.4990	RES 1/8W M FLM 1%	499
R5408	7D3	1214.0101	RES 1/4W C FLM 5%	100
R5409	7C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R5410	7C4	1136.1002	RES 1/8W M FLM 1%	10.0K
R5411	7E4	1214.0510	RES 1/4W C FLM 5%	0
R5412	7E4	1214.0271	RES 1/4W C FLM 5%	270
R5413	5E9	1139.1001	RES 1/8W M FLM .1%	1.00K
R5501	7C3	1136.2491	RES 1/8W M FLM 1%	2.49K
R5502	7E3	1214.0201	RES 1/4W C FLM 5%	200
R5503	7E4	1214.0202	RES 1/4W C FLM 5%	2.0K
R5504	7F5	1214.0270	RES 1/4W C FLM 5%	27
R5505	7D5	1214.0221	RES 1/4W C FLM 5%	220
R5506	7C6	1214.0182	RES 1/4W C FLM 5%	1.8K
R5507	7D6	1214.0681	RES 1/4W C FLM 5%	680
R5508	7C7	1214.0369	RES 1/4W C FLM 5%	3.6
R5509	7E5	1214.0100	RES 1/4W C FLM 5%	10
R5510	7F6	1214.0272	RES 1/4W C FLM 5%	2.7K
R5511	7E6	1214.0102	RES 1/4W C FLM 5%	1K
R5512	7F7	1214.0369	RES 1/4W C FLM 5%	3.6
R5513	5E10	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R5514	7D7	1214.0369	RES 1/4W C FLM 5%	3.6
R5515	5B9	1214.0102	RES 1/4W C FLM 5%	1K
R5601	7E7	1214.0369	RES 1/4W C FLM 5%	3.6
R5602	5E10	1214.0479	RES 1/4W C FLM 5%	4.7
R5603	8C3	1456.1509	RES 1W W WND 1%	15.0

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R56E3	8C3	1336.8008	RES 1/2W M FLM 1%	8.0
R5701	8C4	1239.3339	RES 1/4W M FLM .1%	33.3
R5702	8B4	1239.3339	RES 1/4W M FLM .1%	33.3
R5703	8C5	1239.3750	RES 1/4W M FLM .1%	375
R5704	8A5	1239.3750	RES 1/4W M FLM .1%	375
R5705	8C4	1239.2669	RES 1/4W M FLM .1%	26.64
R5706	8B4	1239.2669	RES 1/4W M FLM .1%	26.64
R57E1	8C4	1239.2399	RES 1/4W M FLM .1%	23.97
R57E2	8B4	1239.2399	RES 1/4W M FLM .1%	23.97
R57E3	8C5	1239.2700	RES 1/4W M FLM .1%	270
R57E4	8A5	1239.2700	RES 1/4W M FLM .1%	270
R57E5	8C4	1239.1919	RES 1/4W M FLM .1%	19.17
R57E6	8B4	1239.1919	RES 1/4W M FLM .1%	19.17
R5901	8B7	1338.6119	RES 1/2W M FLM .25%	61.1
R5902	8C7	1338.6119	RES 1/2W M FLM .25%	61.1
R5903	8B6	1136.2499	RES 1/8W M FLM 1%	24.9
R5904	8B6	1136.2499	RES 1/8W M FLM 1%	24.9
R59E1	8B7	1239.1150	RES 1/4W M FLM .1%	115.6
R59E2	8C7	1239.1150	RES 1/4W M FLM .1%	115.6
R59E3	8B6	1136.1789	RES 1/8W M FLM 1%	17.8
R59E4	8B6	1136.1789	RES 1/8W M FLM 1%	17.8
T56	5C10	4521.0005	TRANSFORMER SIGNAL	GEN-1
U101	1G2	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U111	1G7	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U112	1E7	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U113	1C7	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U121	4C3	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U122	4G3	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U131	5B2	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U132	5E2	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U141	2E2	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U151	1A7	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U152	1A10	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U171	2D7	3411.5534	OP AMP SINGLE	5534A
U191	8D2	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U211	1F8	3323.4040	COUNTER 12-STAGE	74HC4040
U212	1D8	3323.4040	COUNTER 12-STAGE	74HC4040
U213	1E10	3323.4040	COUNTER 12-STAGE	74HC4040
U221	1D10	3324.0251	MULTIPLEXER TRI-ST	74HCT251
U251	2E3	3510.7523	MDAC 8 BIT	AD7523
U252	2D4	3411.5534	OP AMP SINGLE	5534A
U271	2D10	3411.5534	OP AMP SINGLE	5534A
U301	1F9,1G9,1H9	3323.0132	GATE 4X2-IN NAND SCHMT	74HC132
U311	1C3	3324.0138	DECODER 3LINE/8LINE	74HCT138
U312	1A3	3324.0138	DECODER 3LINE/8LINE	74HCT138
U313	4C6	3324.0251	MULTIPLEXER TRI-ST	74HCT251
U331	5C6	3412.5533	OP AMP DUAL	5533A
U351	2B2	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
U352	2A2,2B2,2C2	3424.0339	COMPARATOR QUAD	LM339
U361	2G5	3411.5534	OP AMP SINGLE	5534A

REPLACEABLE ELECTRICAL PARTS LIST: 9GEN.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U401	1E2	3324.0085	COMPARATOR 4 BIT MAG	74HCT85
U411	1E4,1D5	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
U412	3G4,3G6,5G2	3323.0132	GATE 4X2-IN NAND SCHMT	74HC132
U421	1G10,1H10	3324.0074	FLIP-FLOP 2X D	74HCT74
U422	3C2,5A9,5B9	3424.0339	COMPARATOR QUAD	LM339
U431	4E8,5E8	3412.0353	OP AMP DUAL	TL072/LF353
U510	3B2,3G3	3412.5532	OP AMP DUAL	5532
U521	3B5,3B7	3412.0353	OP AMP DUAL	TL072/LF353
U522	3D9,4E6,4F6	3424.0339	COMPARATOR QUAD	LM339
U523	3B9,3B10	3412.0353	OP AMP DUAL	TL072/LF353
U531	3E9,3F9,3G9	3424.0339	COMPARATOR QUAD	LM339


Phasemeter
(P35)
Channel B Output
Generator
(J39)
P12
P13
J11
J16
Generator
(J19)



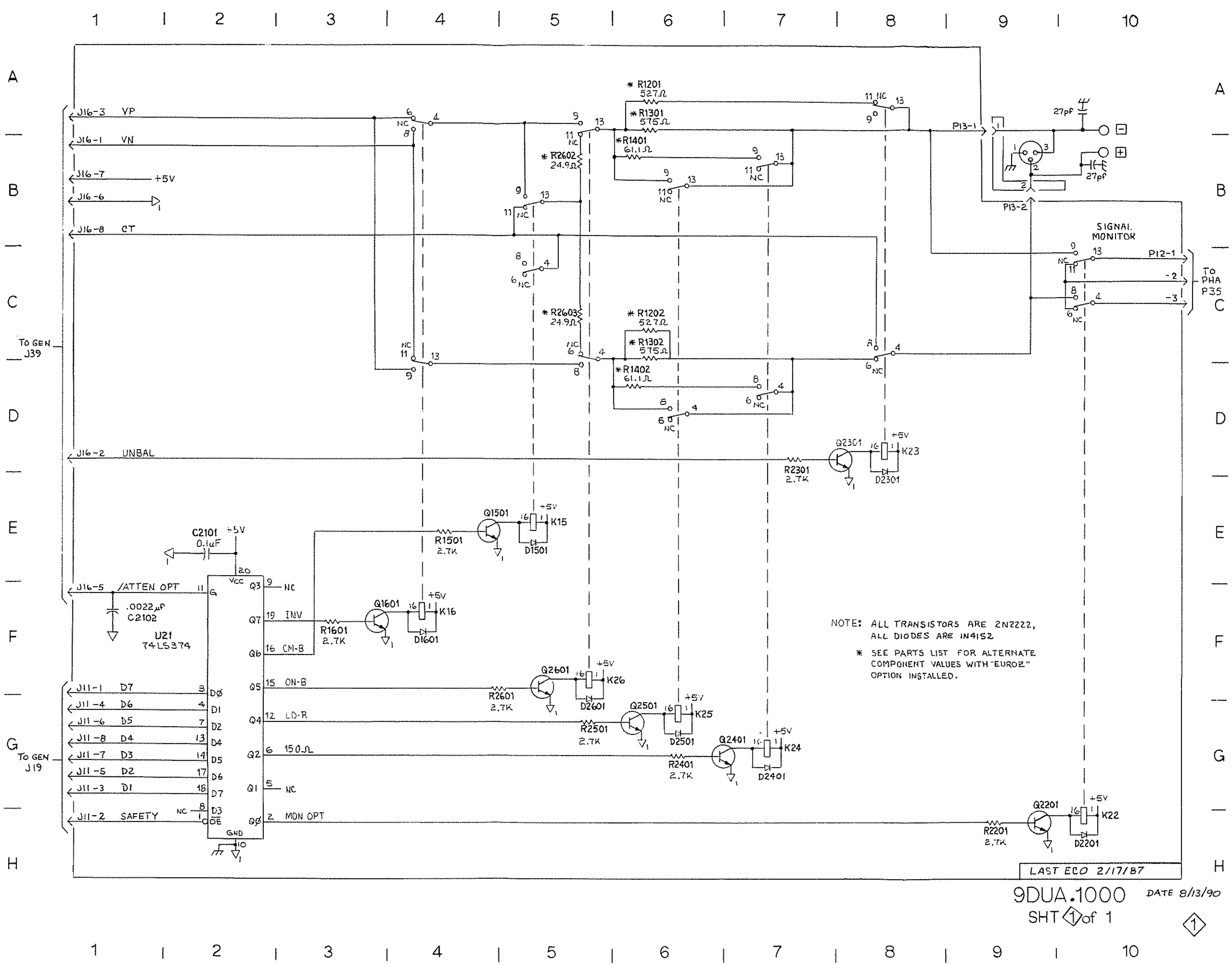
DUAL OUTPUT GENERATOR OPTION 9DUA.1000 (6200.DUA1.4)

DUA-1, GENERATOR DUAL OUTPUT

The signals VP and VN enter the channel B output board via J19 from J39 on the GEN-1 board. They are connected to the relay K16 which can swap their connections to invert the phase of the B channel output. From here they pass through the output on/off relay K26 to the output impedance selection circuitry. When K26 is off, the output is connected to back-terminating resistors R2601 and R2602. K24, K25, R1201, R1201, R1202, R1301, R1302, R1401, and R1402 select the desired buildout resistances. When both K24 and K25 are off the output resistance is 600 Ohms. If K25 is on, the output resistance drops to 150 Ohms (200 Ohms in units with option **EURZ** installed).

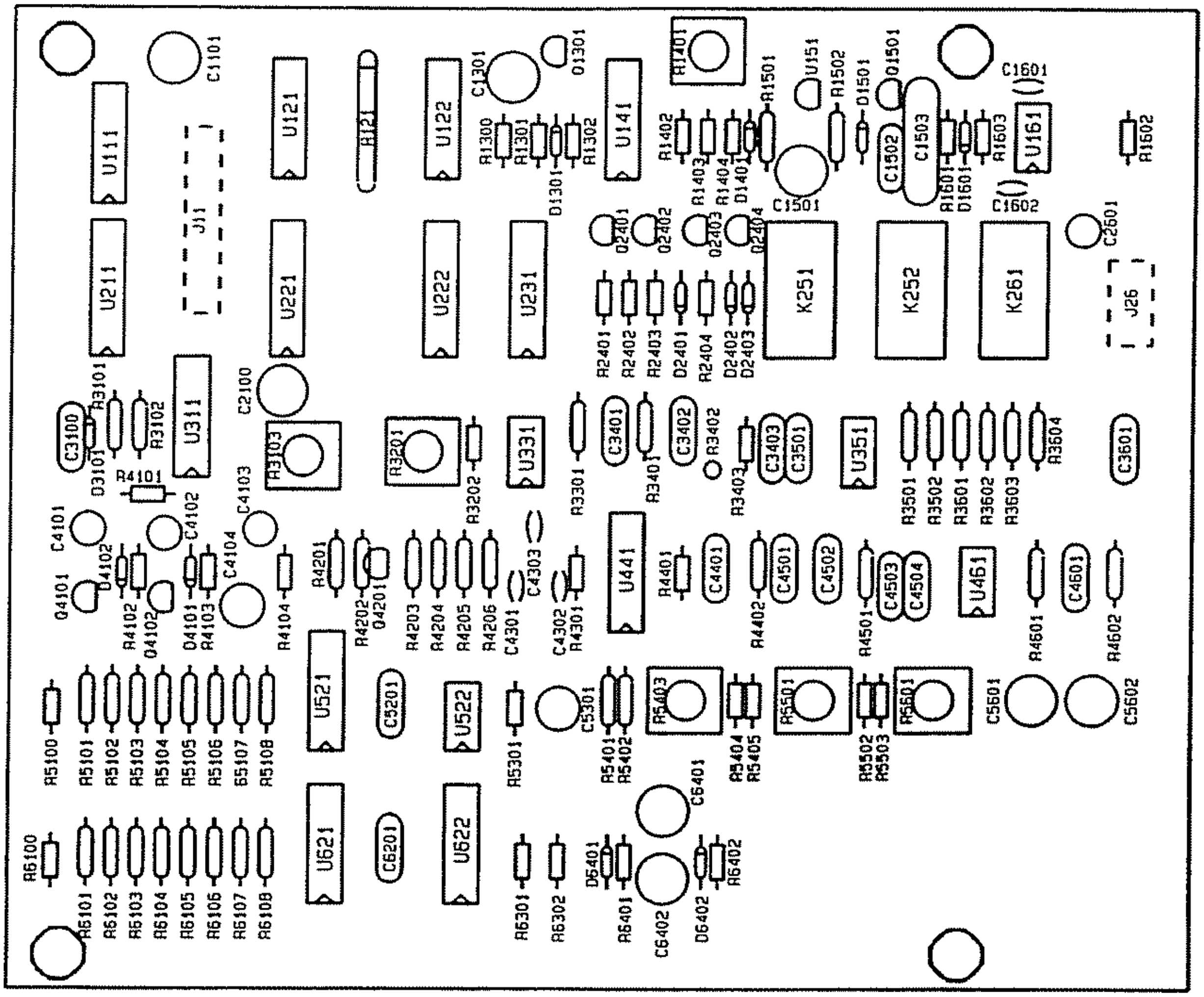
If K15 is energized, the center tap of the resistors will be driven from one half of the transformer, creating a common mode test connection. The unbalanced output configuration is selected by K23 which taps one half of the transformer and lifts R1201 to correct the output impedance. The output feeds the front panel connectors and is also connected to generator monitor relay K22. When energized this relay connects a cable to carry the signal to the PHA board for measurement of the generator channel B output level.

Data is latched by U21 to drive the relays. Resistor, transistor and diode networks (for example R1601-Q1601-D1601) provide the current capability to drive the relays. When a power on reset occurs the output of U21 is shut down via the SAFETY line, tri-stating the outputs and shutting off all relays.


J16-3 VP
J16-1 VN
J16-7 +5V
J16-6
J16-8 CT
TO GEN J39
J16-2 UNBAL
J16-5 /ATTEN OPT
∗ R1201 527Ω
∗ R1301 575Ω
∗ R1401 61.1Ω
∗ R2602 24.9Ω
∗ R2603 24.9Ω
∗ R1202 527Ω
∗ R1302 575Ω
∗ R1402 61.1Ω
P13-1
P13-2
27pF
SIGNAL MONITOR
P12-1
-2
-3
TO PHA P35
Q2301 R2301 2.7K K23 D2301
Q1501 R1501 2.7K K15 D1501
C2101 0.1uF +5V
.0022μF C2102
U21 74LS374
Q1601 R1601 2.7K K16 D1601
INV
CM-B
ON-B
LO-R
150Ω
MON OPT
J11-1 D7
J11-4 D6
J11-6 D5
J11-8 D4
J11-7 D3
J11-5 D2
J11-3 D1
J11-2 SAFETY
TO GEN J19
Q2601 R2601 2.7K K26 D2601
Q2501 R2501 2.7K K25 D2501
Q2401 R2401 2.7K K24 D2401
Q2201 R2201 2.7K K22 D2201
NOTE: ALL TRANSISTORS ARE 2N2222, ALL DIODES ARE IN4152
∗ SEE PARTS LIST FOR ALTERNATE COMPONENT VALUES WITH "EURO2" OPTION INSTALLED.
LAST ECO 2/17/87
9DUA.1000
DATE 8/13/90
SHT 1 of 1

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C2101	1E2	2172.0104	CAP CERAM 100V 20%	.1uF
C2102	1C1	2172.0222	CAP CERAM 100V 20%	.0022uF
D1501	1E5	3110.4152	DIODE SIGNAL	4152
D1601	1F4	3110.4152	DIODE SIGNAL	4152
D2201	1H10	3110.4152	DIODE SIGNAL	4152
D2301	1D8	3110.4152	DIODE SIGNAL	4152
D2401	1G7	3110.4152	DIODE SIGNAL	4152
D2501	1G6	3110.4152	DIODE SIGNAL	4152
D2601	1G5	3110.4152	DIODE SIGNAL	4152
J11	1G1	4221.1008	JACK PC 2 X .1	8 PIN
J16	1A1	4221.1008	JACK PC 2 X .1	8 PIN
K15	1E5	4530.0002	RELAY PC LOW POWER	DPDT
K16	1F4	4530.0002	RELAY PC LOW POWER	DPDT
K22	1H10	4530.0002	RELAY PC LOW POWER	DPDT
K23	1D8	4530.0002	RELAY PC LOW POWER	DPDT
K24	1G7	4530.0002	RELAY PC LOW POWER	DPDT
K25	1G6	4530.0002	RELAY PC LOW POWER	DPDT
K26	1F5	4530.0002	RELAY PC LOW POWER	DPDT
P11	---	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P12	1C10	4221.0036	PLUG PC .1 X.43	36 PIN
P13	1B9	4221.0036	PLUG PC .1 X.43	36 PIN
P16	---	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
Q1501	1E4	3211.2222	XSTR NPN TO92	PN2222A
Q1601	1F3	3211.2222	XSTR NPN TO92	PN2222A
Q2201	1H9	3211.2222	XSTR NPN TO92	PN2222A
Q2301	1D8	3211.2222	XSTR NPN TO92	PN2222A
Q2401	1G7	3211.2222	XSTR NPN TO92	PN2222A
Q2501	1G6	3211.2222	XSTR NPN TO92	PN2222A
Q2601	1F5	3211.2222	XSTR NPN TO92	PN2222A
R1201	1A6	1239.5270	RES 1/4W M FLM .1%	527
R1202	1C6	1239.5270	RES 1/4W M FLM .1%	527
R12E1	1A6	1239.5470	RES 1/4W M FLM .1%	547.1
R12E2	1C6	1239.5470	RES 1/4W M FLM .1%	547.1
R1301	1A6	1239.5750	RES 1/4W M FLM .1%	575
R1302	1C6	1239.5750	RES 1/4W M FLM .1%	575
R13E1	1A6	1239.5820	RES 1/4W M FLM .1%	582
R13E2	1C6	1239.5820	RES 1/4W M FLM .1%	582
R1401	1B6	1338.6119	RES 1/2W M FLM .25%	61.1
R1402	1D6	1338.6119	RES 1/2W M FLM .25%	61.1
R14E1	1B6	1239.1150	RES 1/4W M FLM .1%	115.6
R14E2	1D6	1239.1150	RES 1/4W M FLM .1%	115.6
R1501	1E4	1214.0272	RES 1/4W C FLM 5%	2.7K
R1601	1F3	1214.0272	RES 1/4W C FLM 5%	2.7K
R2201	1H9	1214.0272	RES 1/4W C FLM 5%	2.7K
R2301	1D7	1214.0272	RES 1/4W C FLM 5%	2.7K
R2401	1G6	1214.0272	RES 1/4W C FLM 5%	2.7K
R2501	1G5	1214.0272	RES 1/4W C FLM 5%	2.7K
R2601	1F4	1214.0272	RES 1/4W C FLM 5%	2.7K
R2602	1B5	1136.2499	RES 1/8W M FLM 1%	24.9
R2603	1C5	1136.2499	RES 1/8W M FLM 1%	24.9
R26E2	1B5	1136.1789	RES 1/8W M FLM 1%	17.8
R26E3	1C5	1136.1789	RES 1/8W M FLM 1%	17.8
U21	1F2	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374

IMG-1 IMD GENERATOR OPTION



IMD GENERATOR OPTION 9IMG.1000 (6200.IMG1.6)

IMG-1, GENERATOR IMD OPTION

Control Logic <1>

The data bytes from the host computer enter the IMG-1 board via the 24-pin connector J11. This is connected by pins to the 24-pin connector J20 on the GEN board. Two data bytes are latched on the board by U222 and U221. However only the most significant six bits of each are latched and not all of these are used. U121A and U231B decode the write strobes for the two latches, placing U222 at board address 9 and U221 at board address 10.

U222 latches the four bits which provide selection of IM mode. Its outputs drive U121B which is used as an OR gate and decoder U231A. The decoded outputs drive relays via drive transistors. The output of OR gate U121B enables the sync output via U121D. The decoded DIM mode line is used to enable the squarewave generator through inverter Q1301.

The IM frequency information is latched in U221. The most significant bit selects between squarewave frequencies for the DIM mode. The next three bits (F2, F1, F0) set the frequency of the second oscillator used for the SMPTE and CCIF modes. These three bits select one of seven frequencies. An additional bit (F3) is used to shut down the IM oscillator in other modes. The least significant bit is used to select the 30 kHz or 100 kHz bandwidth limiting of the DIM squarewave.

DIM Squarewave Generator <1>

The DIM squarewave is generated by a counter/comparator which divides the 20 MHz signal down to either 3.15 kHz or 2.96 kHz. The counter consists of a 12-bit ripple counter U211 and, for later serial number units, a pair of flip-flops U311. The two flip-flops in U311 prescale the clock to 5 MHz to drive U211. They count the 20 MHz clock and output the count to AND gates U111. Suppose the 3.15 kHz line is low so that U111A's output will never go high. The counter will count up until 1's appear on the Q12, Q11, Q9, Q6, and Q5 outputs. When this occurs the output of U121C (used as an OR gate) will go high, placing a high level at the "D" input of U122B. The next clock cycle will clock this into U122B, setting its Q output high and resetting the counter. The count sequence begins again, and outputs a pulse train from U122B. This pulse train is sent to U122A which divides the frequency in half, producing a 2.96 kHz squarewave. If the 3.15/2.96 kHz line is high U111A will be enabled and the counter will reset when Q12, Q11, Q7, Q6 all go high. This will occur before the previous pattern does and will produce an output at approximately 3.15 kHz.

Power to the squarewave flip-flop U122 is supplied by a 5 V regulator U151 which provides a source of noise free power whose voltage is independent of the System One mainframe. The amplitude of the squarewave directly impacts the DIM amplitude calibration so it is important that this be stable. Adjustment of this voltage is provided by R1401.

The output of the flip-flop U122A is coupled through a resistor-diode-capacitor network to buffer U161B. The capacitors C1503 and C1502 lowpass filter the squarewave at either 30 kHz or 100 kHz as required for the appropriate standard. The selection of lowpass frequency is accomplished by JFET Q1501. Diode D1601 and R1603 equalize the rise and fall times of the squarewave to compensate for the asymmetrical output impedance of the flip-flop. The /Q output of the flip-flop is coupled to the sync circuits by diode D1301. The state of other generator sync output is overridden by comparator U141D which pulls R1302 low in DIM mode. This provides the necessary level for D1301 to work against.

IM Oscillator <2>

The IM oscillator is a conventional state variable design consisting of integrators U522A and U522B and inverter U331B. The frequency is controlled by changing the input resistors to the integrators. This is accomplished by U521 and U621 and their associated resistors. Selection of the seven frequencies is provided by bits F2, F1, and F0. The fourth bit, F3, is used to shut down the oscillator in modes where it is not used. When F3 goes high U521 and U621 are opened, removing the input resistor from the integrators. U622 is also turned on, shorting out the feedback capacitor with 1 kOhm resistors. R6303 serves to precharge C5201 for faster starting of the oscillator. Power for the CMOS switches (±6 Vdc) is provided by zener regulators D6401 and D6402. Adjustment for integrator capacitor tolerances is provided by R3201.

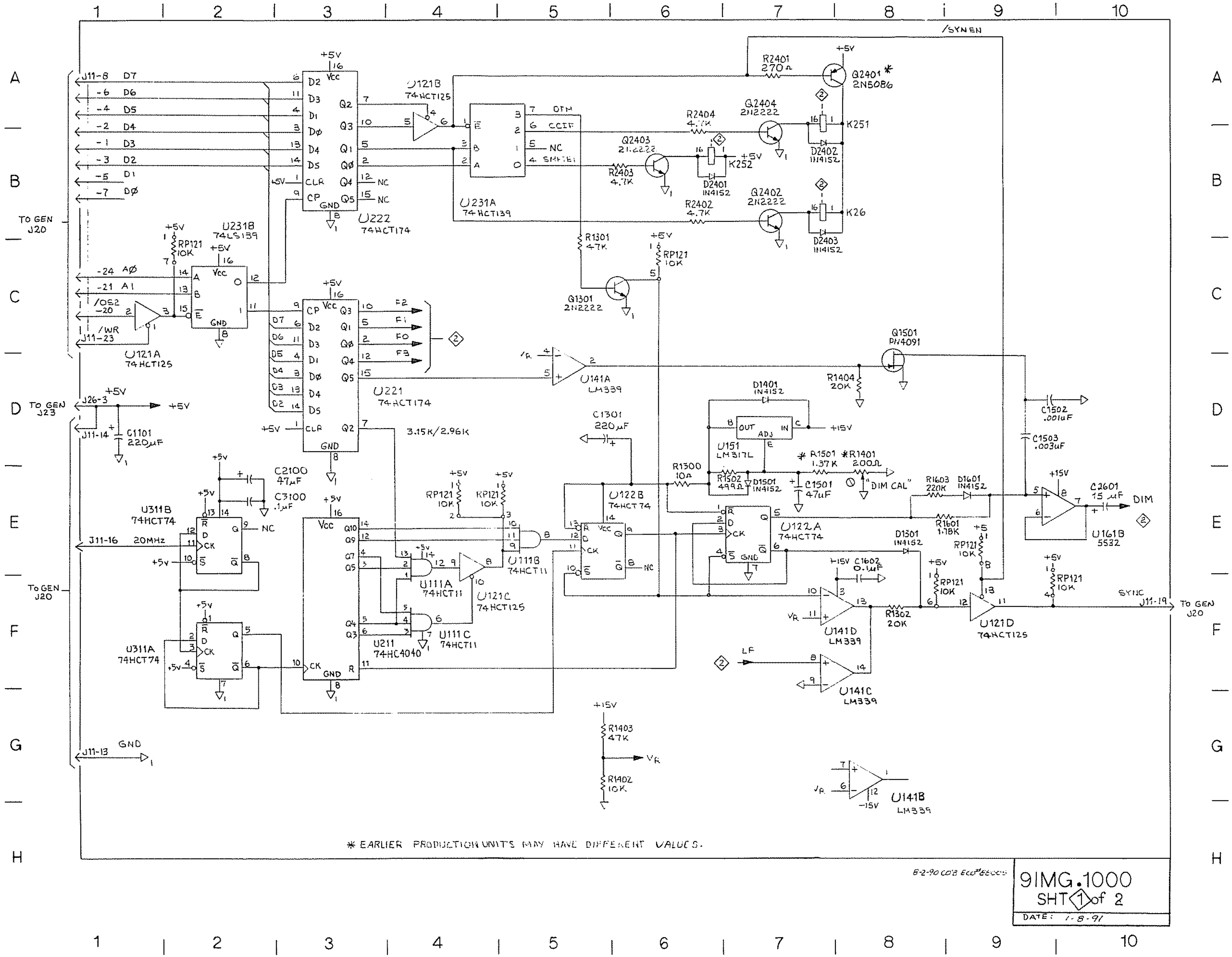
Leveling of the oscillator amplitude is provided by JFET Q4201 acting as a voltage controlled resistance. Its gate drive is provided by half wave rectifier D3101, integrator Q4101 and peak detector Q4102. C4102, D4101, and Q4102 form a peak detector which charges C4103 based on the peak amplitude of the signal at the output of U331B. The output of the oscillator at U522A is rectified by D3101 and compared to a reference current through R3102. The difference is integrated by Q4101 and C4101 and used to change the dc bias on the peak detector. This adjusts the voltage on C4103 which drives the gate of the JFET to set the oscillator amplitude. R3101 adjusts the reference current for exactly the correct output voltage from the loop.

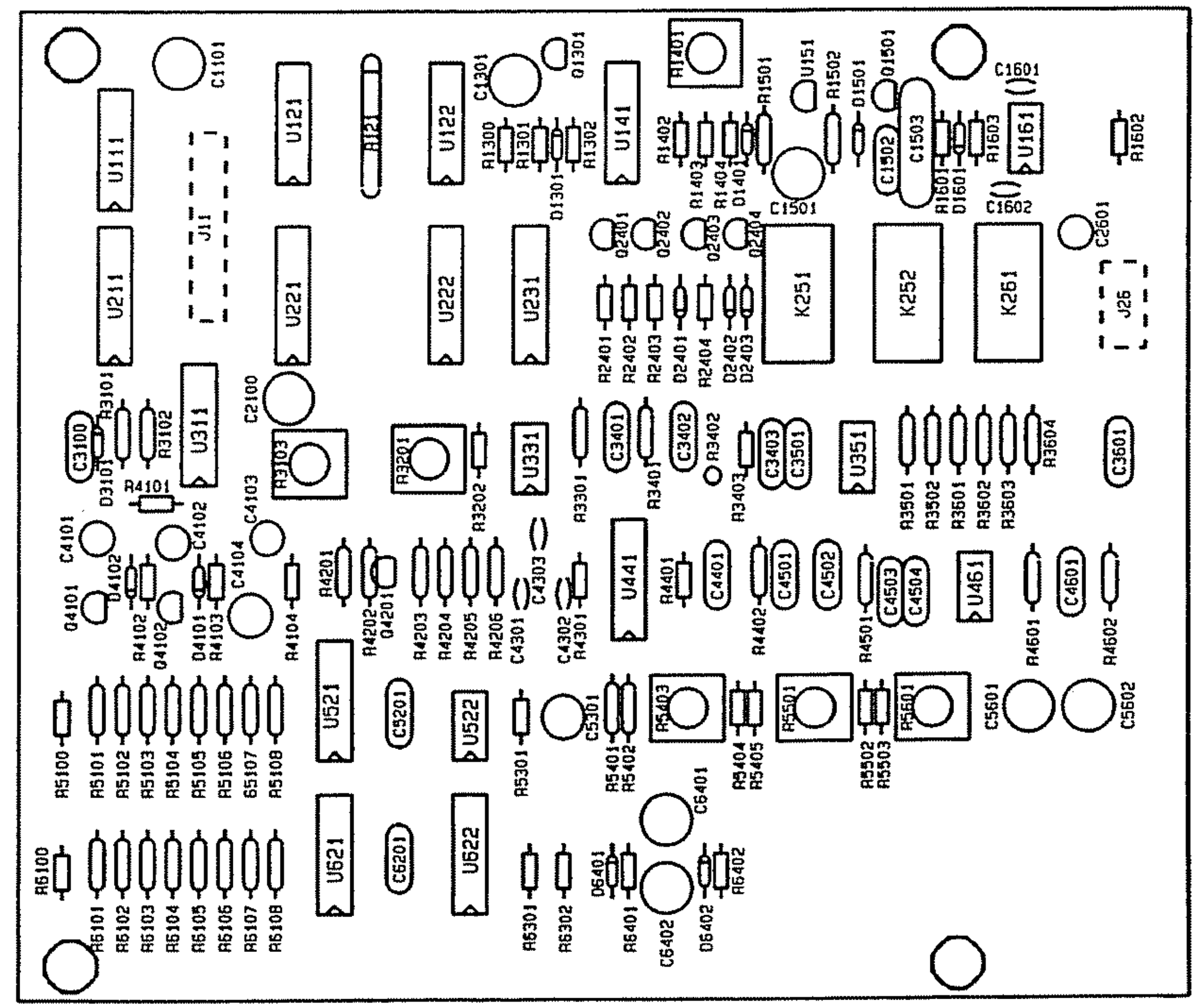
CCIF Signal Generator <2>

The low frequency output from the IM oscillator and the output from the main oscillator are multiplied together by U441. R5501 and R5601 adjust the offsets of the multiplier for minimum leakage of the two original tones into the output. R5403 provides overall gain adjustment and serves as the calibration for CCIF amplitude. The output signal is passed through a 5-pole highpass filter to remove any remaining low frequency energy that would interfere with the CCIF difference tone measurement. A test point is provided ahead of the highpass filter to simplify setting of the multiplier offset adjustments during calibration.

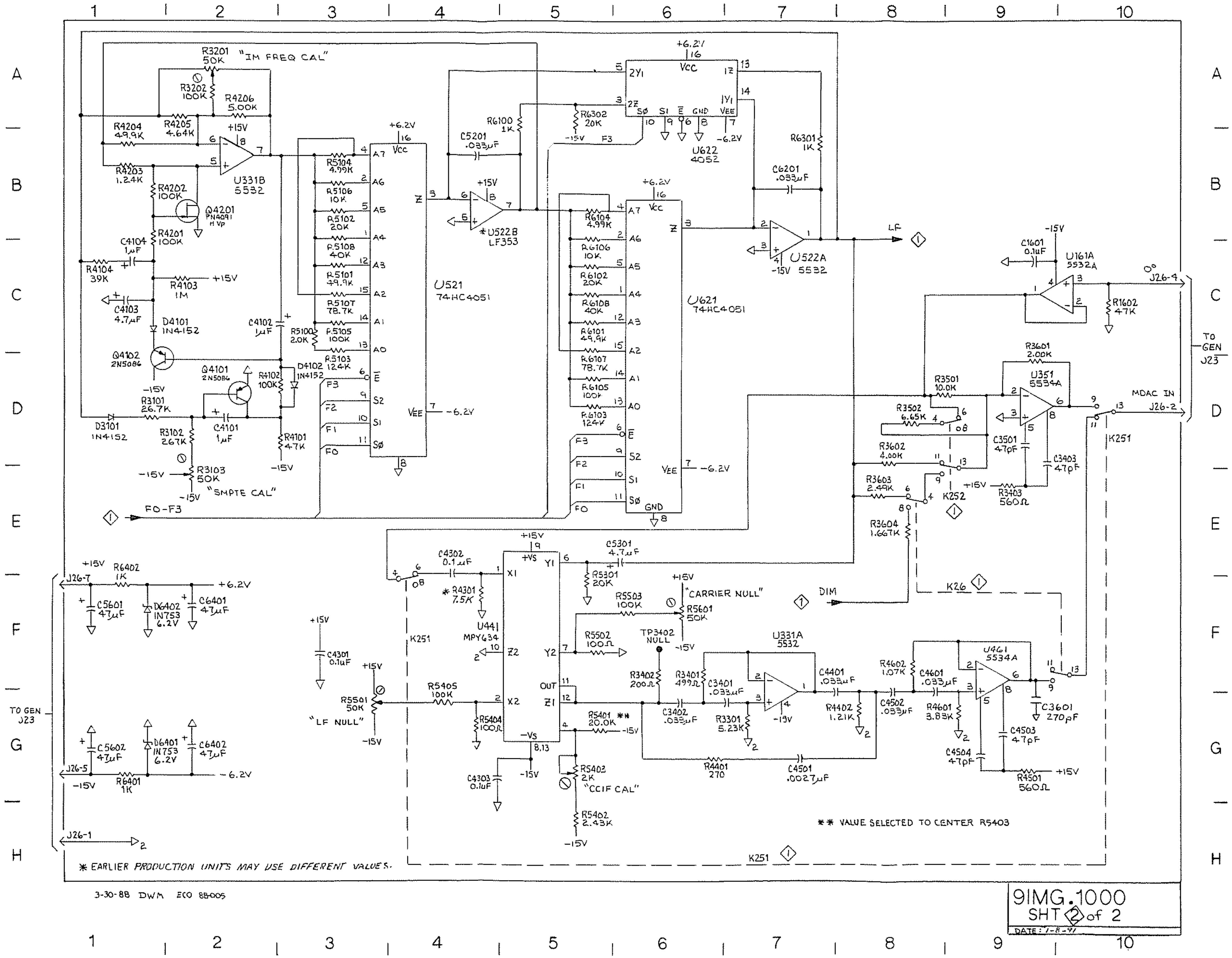
IMD Signal Selection <2>

The output of the IM oscillator or the DIM squarewave generator is mixed with the main oscillator in U351. Selection between them is made by one section of K26. The signal thus selected is summed with the main oscillator signal through R3501 into U351. Resistors R3502 and R3602 are switched in by relay K252 to change the gain ratio for the SMPTE 1:1 mode. If any IMD mode except CCIF is selected K251 connects the output of U351 to the MDAC input. If CCIF is selected or if the IMG-1 board functions are not being used relay K251 switches to the other state which connects the output of U461 to the MDAC input. If none of the IMD test signals are selected, relay K26 opens and disconnects the option board from the amplitude control MDAC on the GEN module board.


/SYNEN
J11-8 D7
-6 D6
-4 D5
-2 D4
-1 D3
-3 D2
-5 D1
-7 DØ
TO GEN J20
U222 74HCT174
U121B 74HCT125
U231A 74HCT139
DTM
CCIF
NC
SMRTEI
R2401 270Ω
Q2401 * 2N5086
Q2404 2N2222
R2404 4.7K
Q2403 2N2222
R2403 4.7K
K251
K252
K26
D2402 1N4152
D2401 1N4152
D2403 1N4152
Q2402 2N2222
R2402 4.7K
R1301 47K
RP121 10K
Q1301 2N2222
-24 AØ
-21 A1
/OS2 -20
/WR J11-23
U231B 74LS139
U121A 74HCT125
U221 74HCT174
F2
F1
F0
F3
U141A LM339
Q1501 PN4091
R1404 20K
TO GEN J23
J26-3 +5V
J11-14
C1101 220µF
C1301 220µF
D1401 1N4152
U151 LM317L
C1502 .001uF
C1503 .003uF
3.15K/2.96K
C2100 47µF
C3100 .1µF
U311B 74HCT74
J11-16 20MHz
U211 74HC4040
U111A 74HCT11
U121C 74HCT125
U111B 74HCT11
U111C 74HCT11
U122B 74HCT74
R1300 10Ω
R1502 499Ω
D1501 1N4152
* R1501 1.37K
* R1401 200Ω
C1501 47uF
"DIM CAL"
R1603 220K
D1601 1N4152
R1601 1.78K
C2601 15µF
DIM
U161B 5532
U122A 74HCT74
D1301 1N4152
C1602 0.1µF
U141D LM339
R1302 20K
U121D 74HCT125
SYNC J11-19
TO GEN J20
U311A 74HCT74
LF
U141C LM339
R1403 47K
R1402 10K
VR
U141B LM339
J11-13 GND
* EARLIER PRODUCTION UNITS MAY HAVE DIFFERENT VALUES.
8-2-90 CO'B ECO#88005
9IMG.1000
SHT 1 of 2
DATE: 1-8-91



IMD GENERATOR OPTION 9IMG.1000 (6200.IMG1.6)



3-30-88 DWM ECO 88-005

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	1D1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1301	IE5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1501	1E7	2932.0476	CAP AL-EL 25V 20%	47uF
C1502	1D9	2276.0102	CAP MICA 100V 1%	.001uF
C1503	1D9	2296.0302	CAP MICA 500V 1%	.003uF
C1601	2C9	2172.0104	CAP CERAM 100V 20%	.1uF
C1602	1F8	2172.0104	CAP CERAM 100V 20%	.1uF
C2100	1E2	2932.0476	CAP AL-EL 25V 20%	47uF
C2601	1E10	2832.0156	CAP TA-EL 25V 20%	15uF
C3100	1E2	2172.0104	CAP CERAM 100V 20%	.1uF
C3401	2G7	2675.0333	CAP POLYC 100V 2%	.033uF
C3402	2G6	2675.0333	CAP POLYC 100V 2%	.033uF
C3403	2D9	2294.0470	CAP MICA 500V 5%	47pF
C3501	2D9	2294.0470	CAP MICA 500V 5%	47pF
C3601	2G9	2296.0271	CAP MICA 500V 1%	270pF
C4101	2D2	2952.0105	CAP AL-EL 50V 20%	1uF
C4102	2C3	2952.0105	CAP AL-EL 50V 20%	1uF
C4103	2C1	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4104	2C1	2952.0105	CAP AL-EL 50V 20%	1uF
C4301	2F3	2172.0104	CAP CERAM 100V 20%	.1uF
C4302	2E4	2172.0104	CAP CERAM 100V 20%	.1uF
C4303	2G4	2172.0104	CAP CERAM 100V 20%	.1uF
C4401	2G7	2675.0333	CAP POLYC 100V 2%	.033uF
C4501	2G7	2675.0272	CAP POLYC 100V 2%	.0027uF
C4502	2G8	2675.0333	CAP POLYC 100V 2%	.033uF
C4503	2G9	2294.0470	CAP MICA 500V 5%	47pF
C4504	2G9	2294.0470	CAP MICA 500V 5%	47pF
C4601	2G8	2675.0333	CAP POLYC 100V 2%	.033uF
C5201	2B4	2675.0333	CAP POLYC 100V 2%	.033uF
C5301	2E6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5601	2F1	2932.0476	CAP AL-EL 25V 20%	47uF
C5602	2G1	2932.0476	CAP AL-EL 25V 20%	47uF
C6201	2B7	2675.0333	CAP POLYC 100V 2%	.033uF
C6401	2F2	2932.0476	CAP AL-EL 25V 20%	47uF
C6402	2G2	2932.0476	CAP AL-EL 25V 20%	47uF
D1301	1E8	3110.4152	DIODE SIGNAL	4152
D1401	1D7	3110.4152	DIODE SIGNAL	4152
D1501	1E7	3110.4152	DIODE SIGNAL	4152
D1601	1E9	3110.4152	DIODE SIGNAL	4152
D2401	1B6	3110.4152	DIODE SIGNAL	4152
D2402	1B7	3110.4152	DIODE SIGNAL	4152
D2403	1B7	3110.4152	DIODE SIGNAL	4152
D3101	2D1	3110.4152	DIODE SIGNAL	4152
D4101	2C1	3110.4152	DIODE SIGNAL	4152
D4102	2D3	3110.4152	DIODE SIGNAL	4152
D6401	2G1	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
D6402	2F1	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
J11	1A1,1F1,1F10	4221.1024	JACK PC 2 X .1	24 PIN
J26	1D1	4221.1008	JACK PC 2 X .1	8 PIN

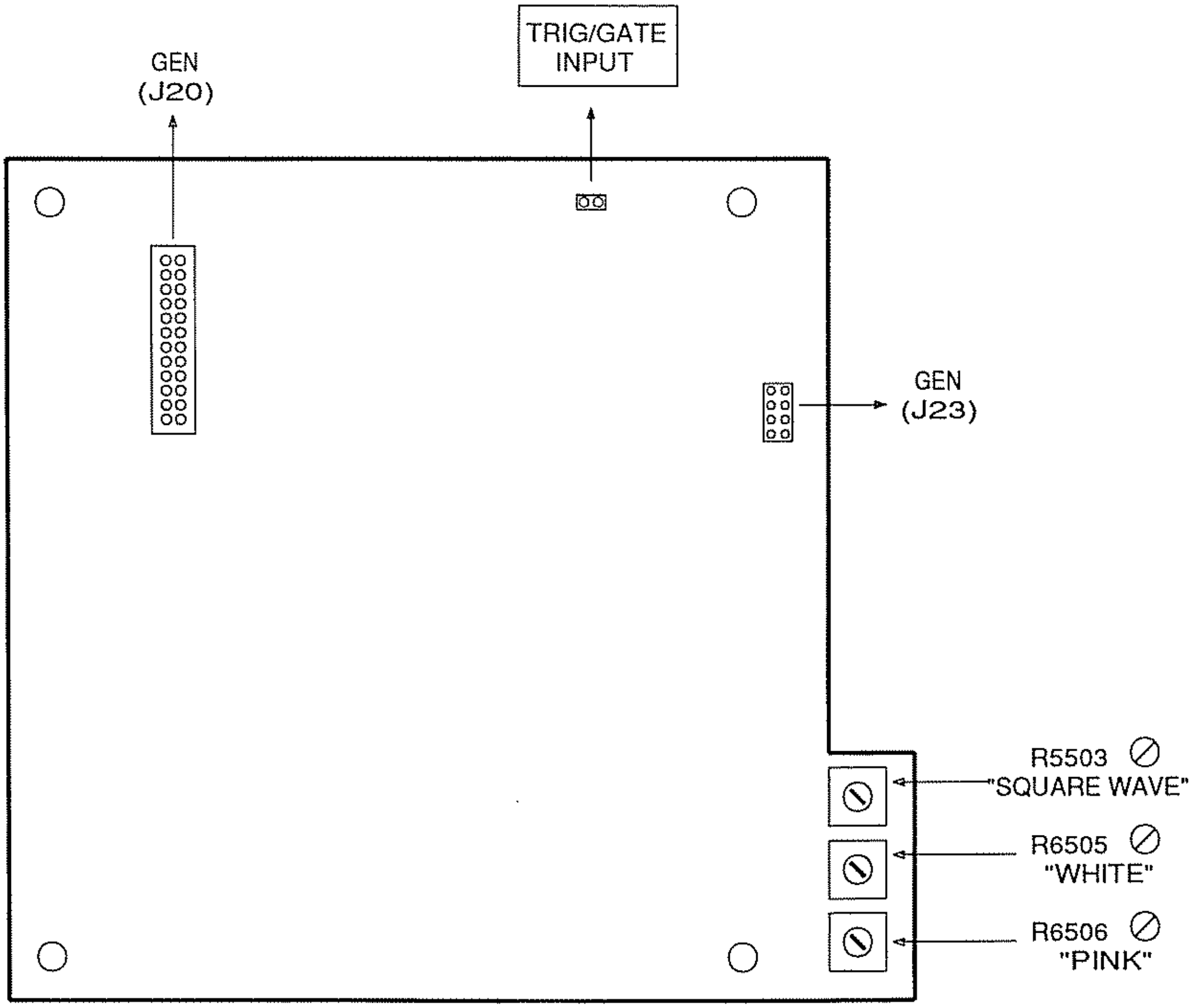
REPLACEABLE ELECTRICAL PARTS LIST: 9IMG.1000

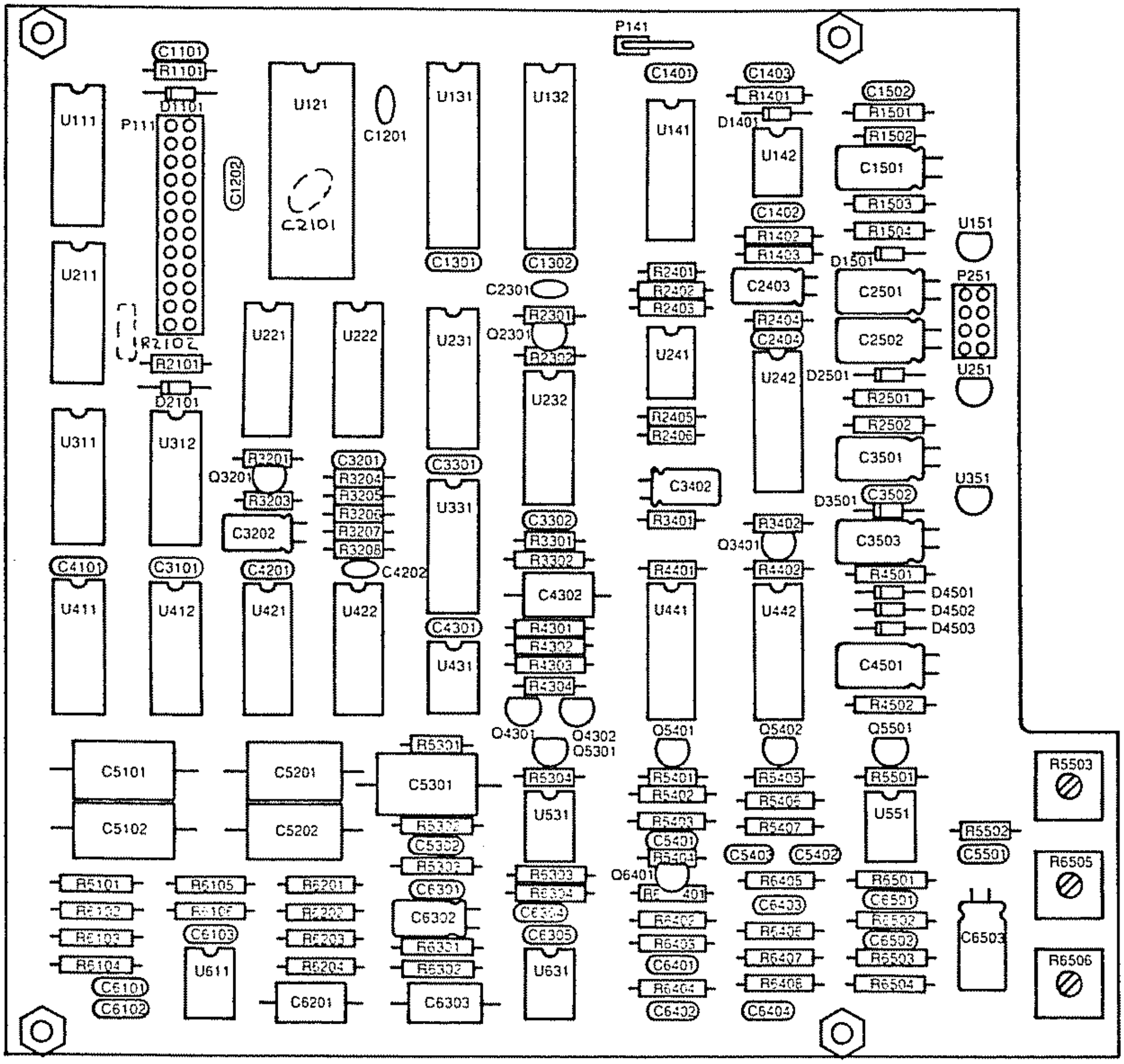
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
K251	1A7	4530.0002	RELAY PC LOW POWER	DPDT
K252	1B6	4530.0002	RELAY PC LOW POWER	DPDT
K26	1B7	4530.0002	RELAY PC LOW POWER	DPDT
P11	---	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P26	---	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
Q1301	1C6	3211.2222	XSTR NPN TO92	PN2222A
Q1501	1D8	3214.4091	XSTR FET TO92	PN4091
Q2401	1A7	3211.5086	XSTR PNP TO92	PN5086
Q2402	1B7	3211.2222	XSTR NPN TO92	PN2222A
Q2403	1B6	3211.2222	XSTR NPN TO92	PN2222A
Q2404	1B7	3211.2222	XSTR NPN TO92	PN2222A
Q4101	2D2	3211.5086	XSTR PNP TO92	PN5086
Q4102	2D1	3211.5086	XSTR PNP TO92	PN5086
Q4201	2B2	3214.4091.H	XSTR FET TO92 HI Vp	PN4091
R121	1C2,1C6,1E5,1E9,1F8	1984.9103	RES NET SIP 5% B	9 X 10K
R1300	1E6	1214.0100	RES 1/4W C FLM 5%	10
R1301	1C5	1214.0473	RES 1/4W C FLM 5%	47K
R1302	1F8	1214.0203	RES 1/4W C FLM 5%	20K
R1401	1E8	4412.0201	POT TRIM PC ENC	200
R1402	1G5	1214.0103	RES 1/4W C FLM 5%	10K
R1403	1G5	1214.0473	RES 1/4W C FLM 5%	47K
R1404	1D8	1214.0203	RES 1/4W C FLM 5%	20K
R1501	1E7	1136.1371	RES 1/8W M FLM 1%	1.37K
R1502	1E7	1136.4990	RES 1/8W M FLM 1%	499
R1601	1E8	1136.1781	RES 1/8W M FLM 1%	1.78K
R1602	2C10	1214.0473	RES 1/4W C FLM 5%	47K
R1603	1E8	1214.0224	RES 1/4W M FLM 5%	220K
R2401	1A7	1214.0271	RES 1/4W C FLM 5%	270
R2402	1B6	1214.0472	RES 1/4W C FLM 5%	4.7K
R2403	1B6	1214.0472	RES 1/4W C FLM 5%	4.7K
R2404	1B6	1214.0472	RES 1/4W C FLM 5%	4.7K
R3101	2D1	1136.2672	RES 1/8W M FLM 1%	26.7K
R3102	2D2	1136.2673	RES 1/8W M FLM 1%	267K
R3103	2E2	4412.0503	POT TRIM PC ENC	50K
R3201	2A2	4412.0503	POT TRIM PC ENC	50K
R3202	2A2	1214.0104	RES 1/4W/C/FLM 5%	100K
R3301	2G7	1136.5231	RES 1/8W M FLM 1%	5.23K
R3401	2F6	1136.4990	RES 1/8W M FLM 1%	499
R3402	2F6	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R3403	2E9	1214.0561	RES 1/4W C FLM 5%	560
R3501	2D8	1136.1002	RES 1/8W M FLM 1%	10.0K
R3502	2D8	1136.6651	RES 1/8W M FLM 1%	6.65K
R3601	2D9	1139.2001	RES 1/8W M FLM .1%	2.00K
R3602	2D8	1139.4001	RES 1/8W M FLM .1%	4.00K
R3603	2E8	1136.2491	RES 1/8W M FLM 1%	2.49K
R3604	2E8	1139.1671	RES 1/8W M FLM .1%	1.667K
R4101	2D3	1214.0473	RES 1/4W C FLM 5%	47K
R4102	2D3	1214.0104	RES 1/4W/C/FLM 5%	100K
R4103	2C2	1214.0105	RES 1/4W C FLM 5%	1M

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4104	2C1	1214.0393	RES 1/4W C FLM 5%	39K
R4201	2B1	1136.1003	RES 1/8W M FLM 1%	100K
R4202	2B1	1136.1003	RES 1/8W M FLM 1%	100K
R4203	2B1	1136.1241	RES 1/8W M FLM 1%	1.24K
R4204	2B1	1136.4992	RES 1/8W M FLM 1%	49.9K
R4205	2A2	1136.4641	RES 1/8W M FLM 1%	4.64K
R4206	2A2	1139.5001	RES 1/8W M FLM .1%	5.00K
R4301	2F4	1214.0752	RES 1/4W C FLM 5%	7.5K
R4401	2G6	1214.0271	RES 1/4W C FLM 5%	270
R4402	2G8	1136.1211	RES 1/8W M FLM 1%	1.21K
R4501	2G9	1214.0561	RES 1/4W C FLM 5%	560
R4601	2G9	1136.3831	RES 1/8W M FLM 1%	3.83K
R4602	2F8	1136.1071	RES 1/8W M FLM 1%	1.07K
R5100	2C3	1214.0202	RES 1/4W C FLM 5%	2.0K
R5101	2C3	1136.4992	RES 1/8W M FLM 1%	49.9K
R5102	2B3	1139.2002	RES 1/8W M FLM .1%	20.0K
R5103	2C3	1136.1243	RES 1/8W M FLM 1%	124K
R5104	2B3	1136.4991	RES 1/8W M FLM 1%	4.99K
R5105	2C3	1136.1003	RES 1/8W M FLM 1%	100K
R5106	2B3	1136.1002	RES 1/8W M FLM 1%	10.0K
R5107	2C3	1136.7872	RES 1/8W M FLM 1%	78.7K
R5108	2B3	1139.4002	RES 1/8W M FLM .1%	40.0K
R5301	2F5	1214.0203	RES 1/4W C FLM 5%	20K
R5401	2G5	1136.2002	RES 1/8W M FLM 1%	20.0K
R5402	2H5	1136.2431	RES 1/8W M FLM 1%	2.43K
R5403	2G5	4412.0202	POT TRIM PC ENC	2K
R5404	2G4	1214.0101	RES 1/4W C FLM 5%	100
R5405	2G4	1214.0104	RES 1/4W/C/FLM 5%	100K
R5501	2G3	4412.0503	POT TRIM PC ENC	50K
R5502	2F5	1214.0101	RES 1/4W C FLM 5%	100
R5503	2F6	1214.0104	RES 1/4W/C/FLM 5%	100K
R5601	2F6	4412.0503	POT TRIM PC ENC	50K
R6100	2B5	1214.0102	RES 1/4W C FLM 5%	1K
R6101	2C5	1136.4992	RES 1/8W M FLM 1%	49.9K
R6102	2C5	1139.2002	RES 1/8W M FLM .1%	20.0K
R6103	2D5	1136.1243	RES 1/8W M FLM 1%	124K
R6104	2B5	1136.4991	RES 1/8W M FLM 1%	4.99K
R6105	2D5	1136.1003	RES 1/8W M FLM 1%	100K
R6106	2B5	1136.1002	RES 1/8W M FLM 1%	10.0K
R6107	2C5	1136.7872	RES 1/8W M FLM 1%	78.7K
R6108	2C5	1139.4002	RES 1/8W M FLM .1%	40.0K
R6301	2B7	1214.0102	RES 1/4W C FLM 5%	1K
R6302	2A5	1214.0203	RES 1/4W C FLM 5%	20K
R6401	2G1	1214.0102	RES 1/4W C FLM 5%	1K
R6402	2F1	1214.0102	RES 1/4W C FLM 5%	1K
U111	1E4,1E5,1F4	3324.0011	GATE 3X 3-IN AND	74HCT11
U121	1A4,1C1,1E4,1F9	3324.0125	BUFFER 4X TRI-ST	74HCT125
U122	1E5,1E7	3324.0074	FLIP-FLOP 2X D	74HCT74
U141	1D5,1F7,1G8	3424.0339	COMPARATOR QUAD	LM339
U151	1D7	3430.1317	VOLT REG POS VAR TO92	LM317L
U161	1E9,2C10	3412.5532	OP AMP DUAL	5532

REPLACEABLE ELECTRICAL PARTS LIST: 9IMG.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U211	1E2	3323.4040	COUNTER 12-STAGE	74HC4040
U221	1C3	3324.0174	FLIP-FLOP 6X D W/CLR	74HCT174
U222	1A3	3324.0174	FLIP-FLOP 6X D W/CLR	74HCT174
U231	1C2,1A4	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
U311	2E2,2F2	3324.0074	FLIP-FLOP 2X D	74HCT74
U331	2B2,2F7	3412.5532	OP AMP DUAL	5532
U351	2D9	3411.5534	OP AMP SINGLE	5534A
U441	2F5	3441.0634	MULTIPLIER	MPY634K
U461	2F9	3411.5534	OP AMP SINGLE	5534A
U521	2B4	3323.4051	MULTIPLEX 8X	HC4051
U522	2B4,2B7	3412.0353	OP AMP DUAL	TL072/LF353
U621	2C6	3323.4051	MULTIPLEX 8X	HC4051
U622	2A6	3321.4052	MULTIPLEX 4X DIFF	4052


TRIG/GATE
INPUT
GEN
(J20)
GEN
(J23)
R5503
"SQUARE WAVE"
R6505
"WHITE"
R6506
"PINK"



BURST-NOISE-SQUAREWAVE GENERATOR OPTION 9BUR.1000 (6200.BUR1.4)

BUR-1, BURST GENERATOR OPTION

Control Logic <1>

The data bytes from the host computer enter the BUR-1 board via the 24-pin connector P111. This is connected by pins to the 24-pin connector J20 on the GEN board. Two data bytes are latched on the board by U131 and U132. 1-of-8 decoder U211 decodes the write strobes for the two latches, placing U131 at board address 8 and U132 at board address 10.

U131 latches the six bits which provide selection of mode. Four bits are used to drive 1-of-8 decoder U231. Its outputs drive the enable lines for each operational mode of the board. The major operating modes of the BUR-1 board may be grouped as burst, noise, and squarewave.

Triple 3-input AND gate U222 combines several of these mode select lines to obtain other enables as needed. The output of U222C will go low in either bandpass noise mode or USASI noise mode. This enables the input to the bandpass filter. AND gate U222B goes low in bandpass noise, white noise and pink noise modes. This enables U221B which buffers the noise generator sync to the output. The output of U222B is combined with the USASI noise enable line by NAND gate U311B, allowing operation of the noise generator. U222A enables the burst counter circuits, including the burst sync output, in the USASI noise and sine burst modes.

Burst Generator <1>

The burst generator counts the sinewave oscillator output and gates the sinewave on and off as necessary. The burst counters are implemented with two sections of U121, an 82C54 triple 16-bit counter. Counter 1 is used to set the number of cycles between the start of successive bursts. Counter 2 is used to set the number of cycles that the signal is on during a burst. The main oscillator sync signal is used as the clock for the counters. This signal is 90 degrees out of phase with the sinewave, allowing sufficient setup time for the logic circuits. It directly drives counter 2 and drives counter 1 through inverter U312A.

When counter 2 is triggered its output goes low for the programmed number of counts. This signal is inverted by U312C and used to drive the data input of flip-flop U232B. The clock to the flip-flop is provided by comparator U331B and is coincident with the zero crossing of the sinewave. When the data input goes high the /Q output will go low, selecting the full amplitude signal via the CMOS switch U242C. At the end of the on cycle count the data input will go low and the switch will select the off amplitude from the MDAC and attenuators.

The Q output of flip-flop U232B is buffered by tri-state buffer U221D to provide the sync output. This buffer is enabled by AND gate U222A which also enables the output JFET Q3401. This signal is inverted by Q2301 to enable flip-flop U232B.

At the end of the programmed number of counts for the desired repetition interval the output of counter 1 pulses low for one cycle. This triggers counter 2 through tri-state buffer U221A.

NAND gate U311A buffers the front panel TRIGGER/GATE INPUT (from P141). With no input applied the NAND gate input is pulled high, driving the output low. This enables buffer U221A, allowing the repetition rate counter to trigger the burst on counter. If the TRIGGER/GATE INPUT is pulled low U311A's output will go high, shutting off U221A and shutting off the output. When U221A is disabled, the gate input of counter 2 is pulled low. When the input to U311A is returned high U221A is re-enabled, driving the gate input of U121 counter 2 high and triggering a burst of sinewave.

Eight bits of burst off-amplitude information are latched in U132. These drive 8-bit multiplying D/A converter U141. This is used to control the off amplitude of the burst over a 20 dB range. The off range is then extended by the two least significant bits of U131. These control 20 dB and 40 dB step attenuators.

±6 V power for the CMOS switches and their associated op-amps is provided by U151 and U251. These are internally current limited at approximately 150 mA.

Noise Generator <2>

The random noise is created by a pseudo-random sequence generator consisting of shift registers U411, U412 and U421, and parity generator U422. The shift registers form a 20-bit long chain with feedback taps from the outputs of stages 2, 3, 4, 7, 10, 14, 17 and 20. These drive the parity generator U422 whose even parity output is returned to the input of the register chain. This ring is clocked with a 4 MHz signal from U312D. Divide-by-5 counter U111B is used to create 4 MHz from the 20 MHz master clock. The NOR gate U312D shifts the edges as necessary to satisfy the setup timing requirements of U121.

An all-high condition of the register outputs would produce a high at the output of parity generator U422. This would continue to feed ones into the shift register ring and the generator would lock up. NAND gates U311C and U311D and counters U111A and U111C are used to sense this condition. The outputs of stages 16 and 24 drive the inputs of U311C. When both inputs are high the output goes low enabling a divide-by-10 counter U111C. The counter is clocked by U111A which divides the 4 MHz noise generator clock by 2. If both stages 16 and 24 are high for 20 clock cycles of the noise generator the output of U311D will go low. This low level drives the second input of shift register U421, placing a low into the ring and starting the generator. This can happen only under fault conditions where the generator had locked up with all ones.

Transistor Q3201 and op-amp U431A and comparator U331A provide a true random noise from the pseudo-random sequence generator when desired. The op-amp U431 amplifies noise from Q3201 to produce a source of truly random noise. Comparator U331A converts this to a TTL level and drives an input of the parity generator U422. This causes a random inversion of the data in the shift register ring, effectively convolving the spectrum of the pseudo-random noise with that of the transistor noise. However the amplitude of the noise is stable with temperature and component tolerances because of the digital nature of the pseudo-random ring.

NAND gate U311B is used to shut down the noise generator ring if the board is not in any of the noise modes. If both of its inputs are high its output goes low, driving the shift register reset inputs low.

The pink, white, and bandpass noise modes derive the sync signal from the noise generator. This signal is designed to occur once per repetition of the pseudo-random sequence. The sequence will have all 20 active locations in the shift registers filled with zeroes only once during a cycle. To sense this state one section of the triple counter U121 is used to count the number of zeros occurring in a row. The odd output of the parity generator U422 drives the gate input of triple counter U121. This allows U121 to count when it is high, corresponding to a low at the even parity output which drives the shift registers.

The counter clock is a 4 MHz signal from U111B which provides one pulse for each clock of the shift registers. If the gate input stays high for 20 clock cycles the output of the U121 will go low for one clock cycle. This output is coupled to the sync output line by tri-state buffer U221B. Whenever the gate input goes low the counter is reset. Counting begins again when the gate input rises. When the true random mode is selected the sequence does not repeat so no output is provided by the counter.

Weighting Filters <2>

The output of the shift registers is passed through a 250 kHz lowpass filter and a 10 Hz highpass filter, both implemented by U611A. This converts the binary noise to Gaussian distributed white noise. This is further band limited to approximately 22 kHz by a 2-pole lowpass filter consisting of U531A and its associated parts. R6505 provides adjustment of gain to set calibration of the white noise amplitude.

Pink noise is obtained from the wideband white noise with a -3 dB per octave filter. U611B, U631A, U631B and their associated resistors and capacitors form a 7-pole, 6-zero active lowpass filter whose response is -3 dB per octave from 10 Hz to 200 kHz. R6506 provides gain control.

Bandpass pink noise is created by filtering the wideband pink noise through the main oscillator loop. The oscillator leveler is shut down and the Q is adjusted to give a 1/3-octave wide bandpass response. This is accomplished by U531B, which mixes some of the oscillator output with the pink noise and applies it to the bandpass input. The amount of oscillator output signal mixed with the noise adjusts the Q of the filter response. The leveler shutdown is accomplished on the GEN board by appropriate mode control bits.

The USASI and pulsed-USASI noise is obtained by filtering the wideband white noise with a single pole highpass and single pole lowpass filter. This noise is applied to the main oscillator loop which is configured as a lowpass filter for this operating mode. The lowpass output of the oscillator is the signal applied to the burst circuits. The burst circuits are used to select the appropriate noise on time, off time and off amplitude.

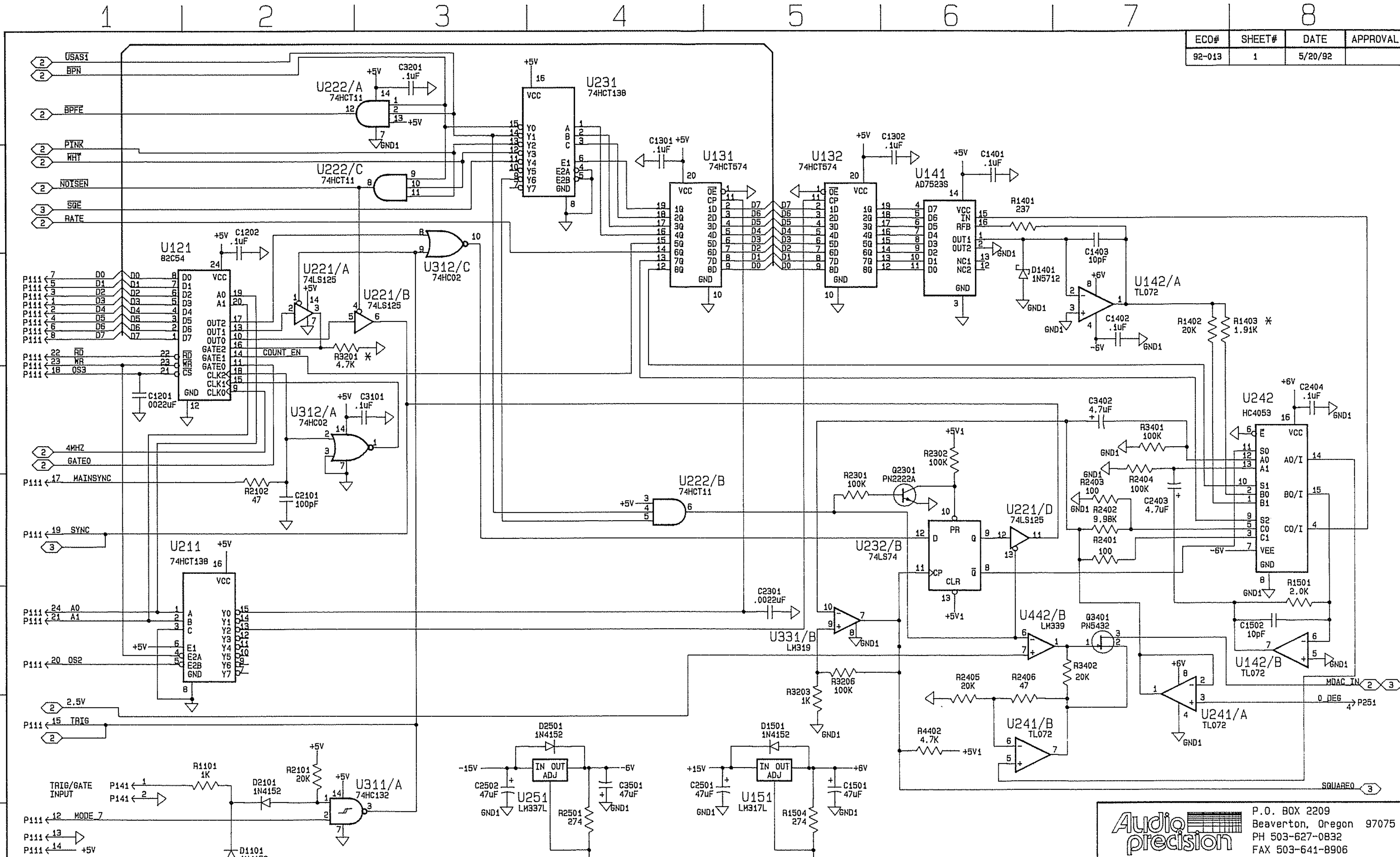
Squarewave Generator <3>

The squarewave is generated by dividing the sinewave sync signal from the main oscillator by 2 in flip-flop U232A. The two outputs of the flip-flop are combined in a differential to single ended converter stage U551A. This amplifier and U551B comprise a 3-pole bandwidth limiting filter. R3302 compensates for asymmetrical loading of the flip-flop. The /Q output of the flip-flop is coupled to the sync circuits by tri-state buffer U221C. U312B shuts down the flip-flop when squarewave mode is not selected.

Power to the squarewave flip-flop and part of the noise generator is supplied by a 5 V regulator U351. It provides a source of noise free power whose voltage is independent of the System One mainframe. Adjustment of this voltage is provided by R5503, the squarewave calibration potentiometer.

IMD Signal Selection

The desired signal from the appropriate filter output is connected to the input of the MDAC stage by JFET switches. The JFETs have their gates pulled to their source potential by a resistor. An open collector output from one section of quad comparators U441 and U442 pulls the gate low to turn the JFET off. U441 and U442 compare the appropriate logic line to a +2.5V reference voltage. Comparators which have their positive inputs connected to the +2.5V reference will turn their JFET on when their inverting input is low. If the +2.5V reference drives the inverting input the JFET will be off when the logic line is low.



ECO#	SHEET#	DATE	APPROVAL
92-013	1	5/20/92	

NOTE: * EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.

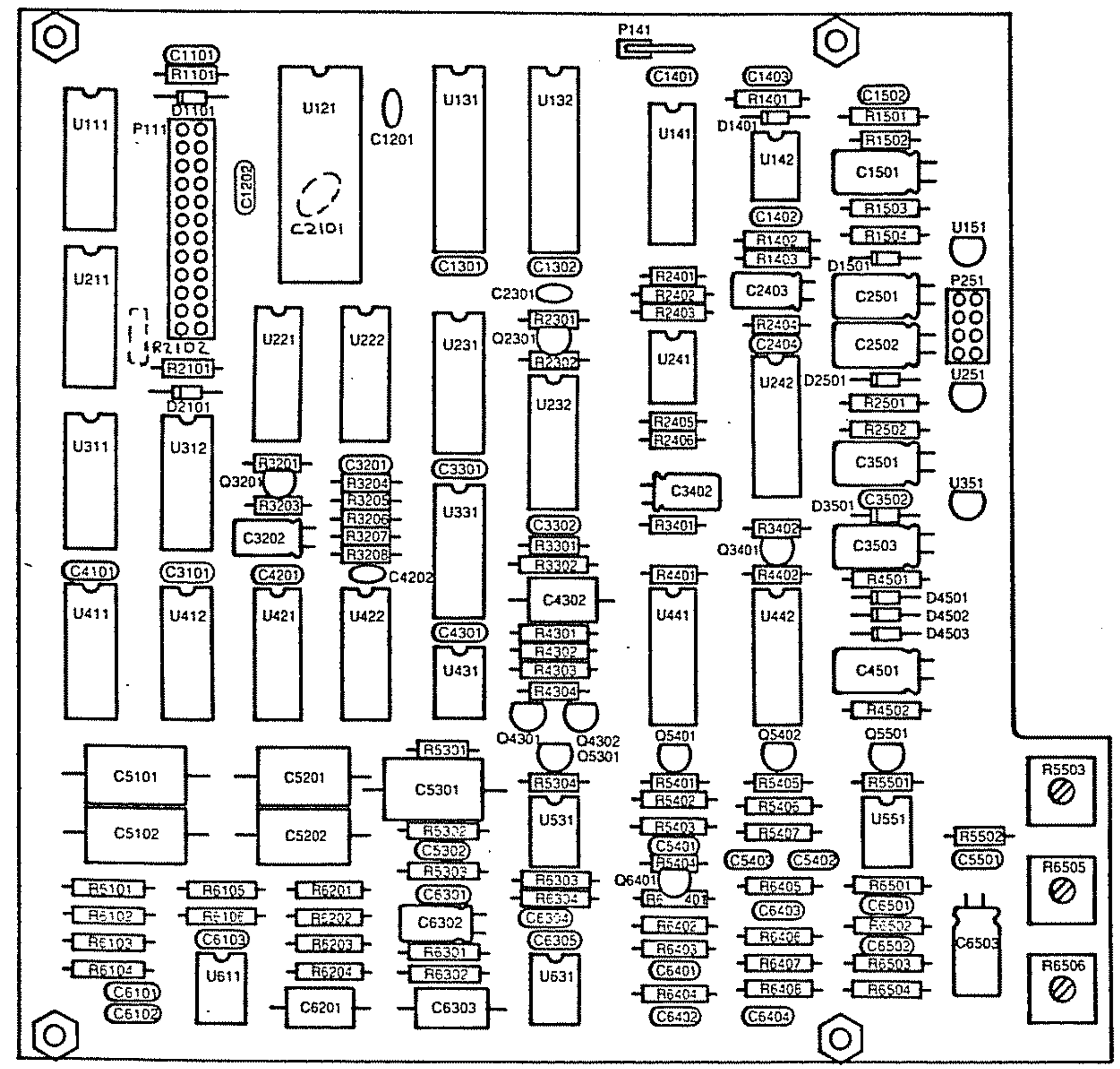
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 12/28/92

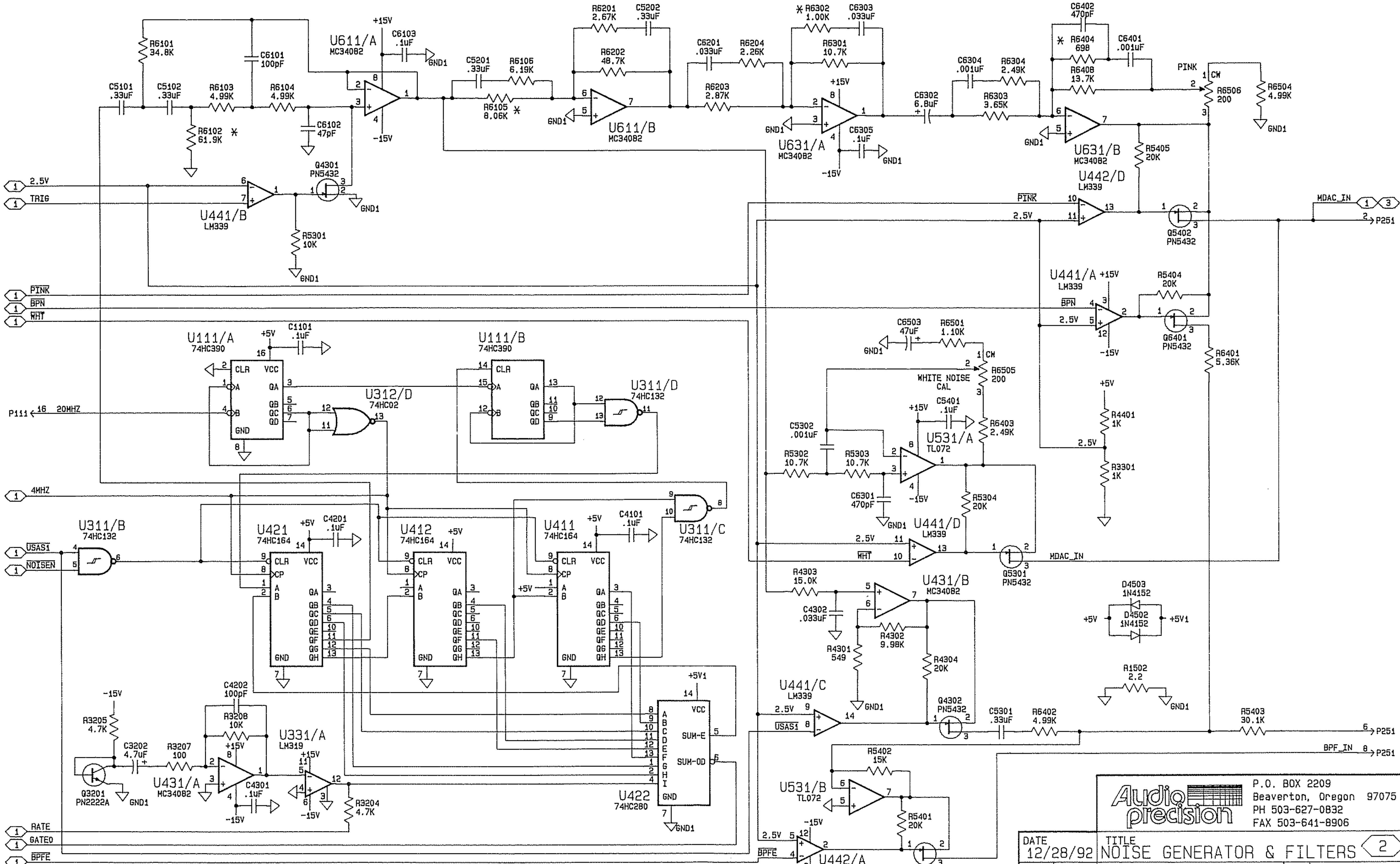
TITLE BURST GENERATOR & LOGIC (1)

SCALE | SIZE B | DRAWING NO. 9BUR.1000 | REV 4 | SHEET 1 OF 3

FILE: BUR1.SCH



BURST-NOISE-SQUAREWAVE GENERATOR OPTION 9BUR.1000 (6200.BUR1.4)

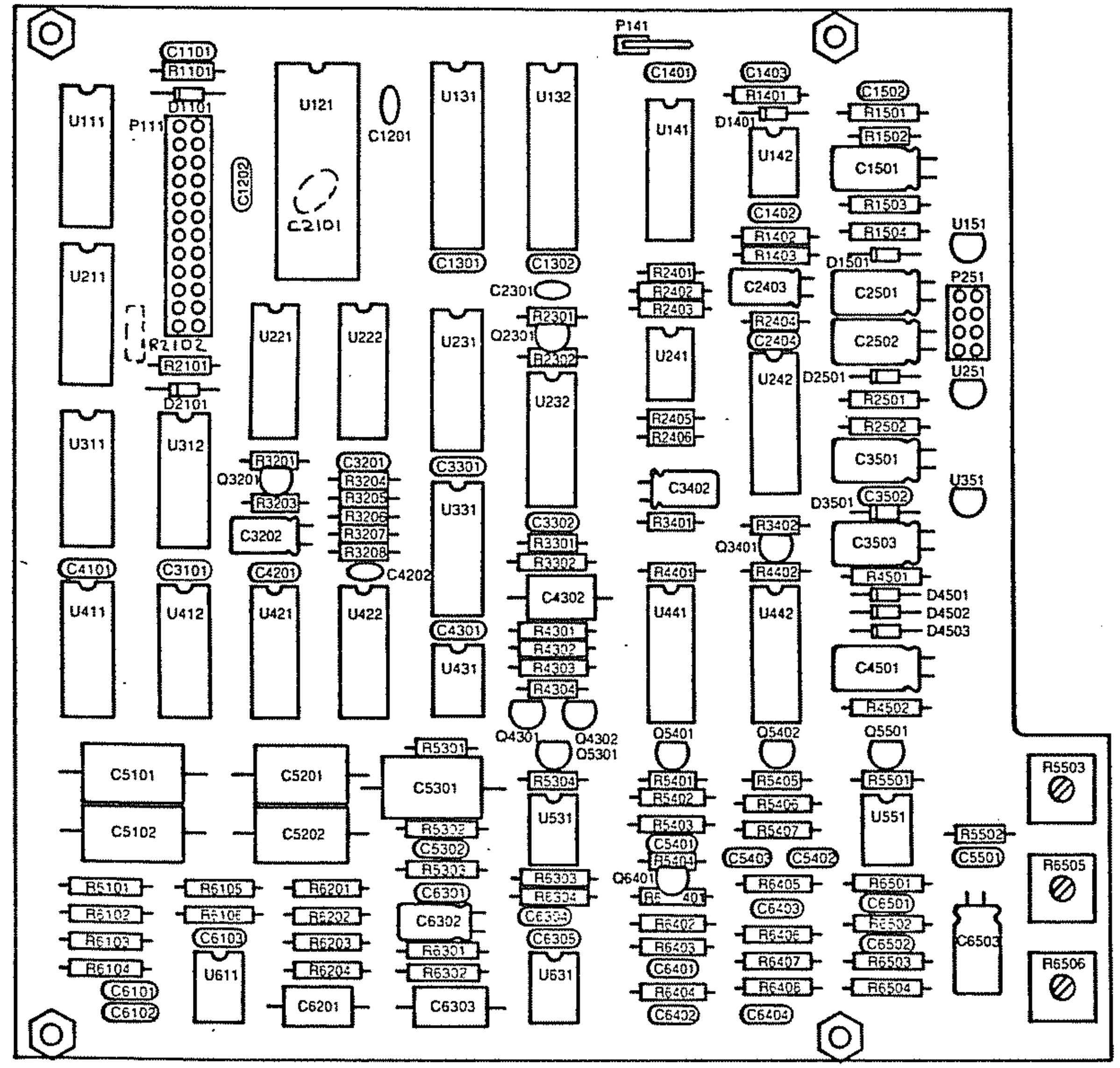


NOTE: * EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.

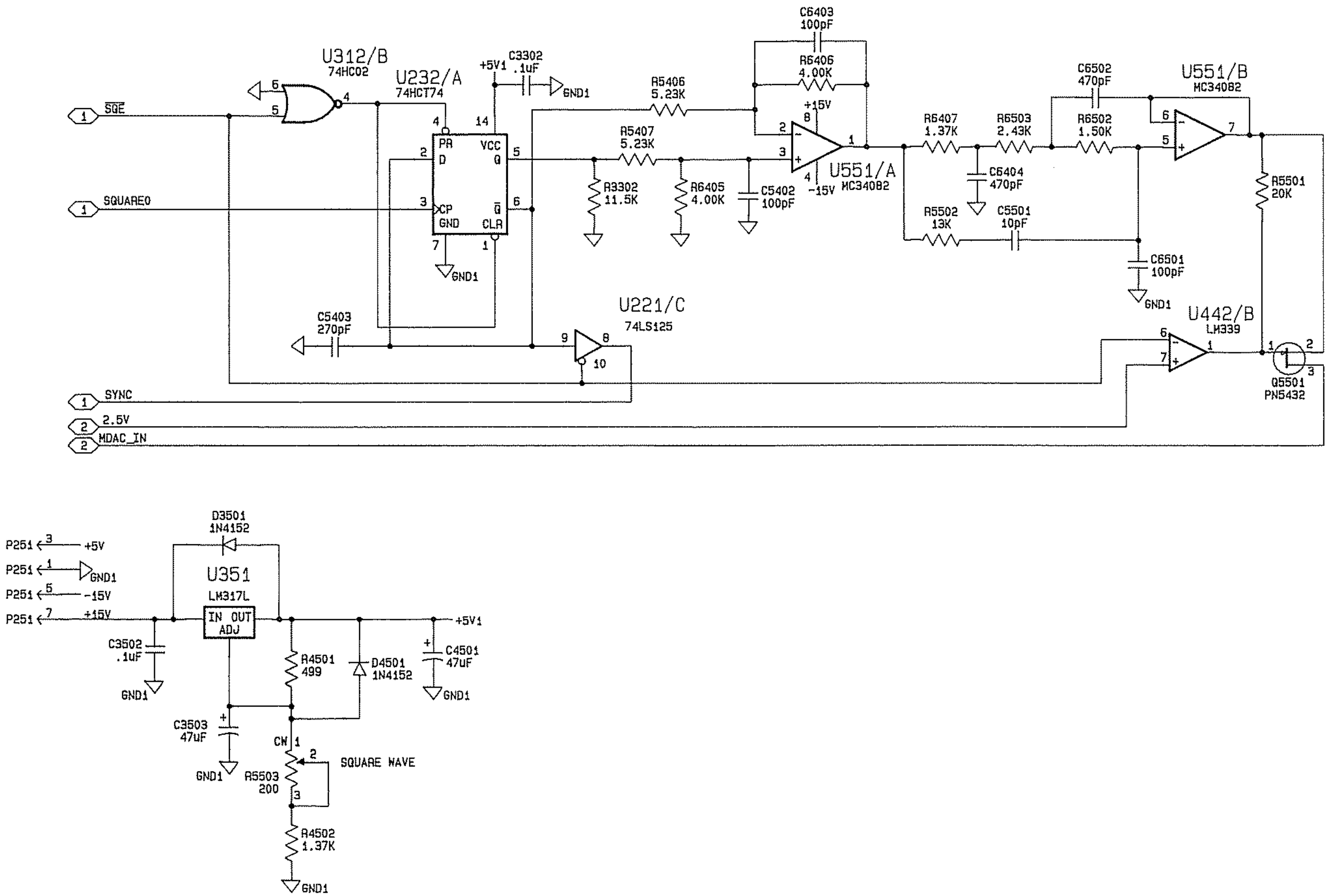
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE		
12/28/92	NOISE GENERATOR & FILTERS	2	
SCALE / SIZE B	DRAWING NO. 9BUR.1000	REV 4	SHEET 2 OF 3

FILE: BUR2.SCH



BURST-NOISE-SQUAREWAVE GENERATOR OPTION 9BUR.1000 (6200.BUR1.4)



NOTE: * EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 12/28/92

TITLE SQUARE WAVE GENERATOR 3

SCALE | SIZE B | DRAWING NO. 9BUR.1000 | REV 4 | SHEET 3 OF 3

FILE: BUR3.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	1D2	2172.0104	CAP CERAM 100V L 20%	.1uF
C1201	1D1	2172.0222	CAP CERAM 100V 20%	.0022uF
C1202	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C1301	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C1302	1B6	2172.0104	CAP CERAM 100V 20%	.1uF
C1401	1C7	2172.0104	CAP CERAM 100V 20%	.1uF
C1402	1C7	2172.0104	CAP CERAM 100V 20%	.1uF
C1403	1C7	2294.0100	CAP MICA 500V 5%	10pF
C1501	1H5	2932.0476	CAP AL-EL 25V 20%	47uF
C1502	1F8	2294.0100	CAP MICA 500V 5%	10pF
C2101	1E2	2296.0101	CAP MICA 500V 1%	100pF
C2301	1F5	2172.0222	CAP CERAM 100V 20%	.0022uF
C2403	1E7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C2404	1D8	2172.0104	CAP CERAM 100V 20%	.1uF
C2501	1H5	2932.0476	CAP AL-EL 25V 20%	47uF
C2502	1H3	2932.0476	CAP AL-EL 25V 20%	47uF
C3101	1D3	2171-0104	CAP CERAM 100V 20%	.1uF
C3201	13A	2172.0104	CAP CERAM 100V 20%	.1uF
C3202	2G1	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3301	1D3	2172.0104	CAP CERAM 100V 20%	.1uF
C3302	1E6	2172.0104	CAP CERAM 100V 20%	.1uF
C3402	1D7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3501	1H4	2932.0476	CAP AL-EL 25V 20%	47uF
C3502	3G1	2172.0104	CAP CERAM 100V 20%	.1uF
C3503	3G1	2932.0476	CAP AL-EL 25V 20%	47uF
C4101	2F4	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	2F2	2172.0104	CAP CERAM 100V 20%	.1uF
C4202	2G2	2296.0101	CAP MICA 500V 1%	100pF
C4301	2H2	2172.0104	CAP CERAM 100V 20%	.1uF
C4302	2F5	2675.0333	CAP POLYC 100V 2%	.033uF
C4501	3G2	2932.0476	CAP AL-EL 25V 20%	47uF
C5101	2B1	2675.0334	CAP POLYC 100V 2%	.33uF
C5102	2B1	2675.0334	CAP POLYC 100V 2%	.33uF
C5201	2B3	2675.0334	CAP POLYC 100V 2%	.33uF
C5202	2A4	2675.0334	CAP POLYC 100V 2%	.33uF
C5301	2G6	2675.0334	CAP POLYC 100V 2%	.33uF
C5302	2E5	2276.0102	CAP MICA 100V 1%	.001uF
C5401	2D6	2172.0104	CAP CERAM 100V 20%	.1uF
C5402	3D4	2296.0101	CAP MICA 500V 1%	100pF
C5403	3D2	2296.0271	CAP MICA 500V 1%	270pF
C5501	3D5	2294.0100	CAP MICA 500V 5%	10pF
C6101	2A2	2296.0101	CAP MICA 500V 1%	100pF
C6102	2B2	2294.0470	CAP MICA 500V 5%	47pF
C6103	2B3	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	2B5	2675.0333	CAP POLYC 100V 2%	.033uF
C6301	2E5	2296.0471	CAP MICA 500V 1%	470pF
C6302	2B6	2832.0685	CAP TA-EL 25V 20%	6.8uF
C6303	2A5	2675.0333	CAP POLYC 100V 2%	.033uF
C6304	2B6	2276.0102	CAP MICA 100V 1%	.001uF
C6305	2B5	2172.0104	CAP CERAM 100V 20%	.1uF
C6401	2B7	2276.0102	CAP MICA 100V 1%	.001uF
C6402	2A7	2296.0471	CAP MICA 500V 1%	470pF

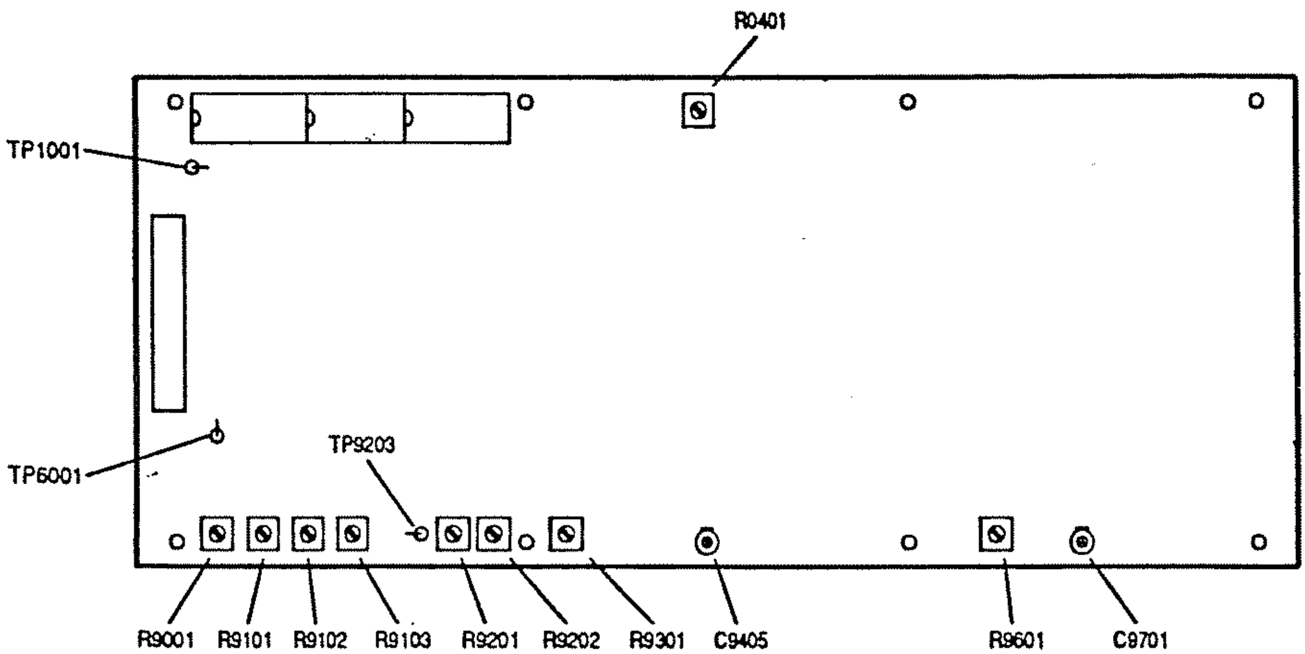
REPLACEABLE ELECTRICAL PARTS LIST: 9BUR.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C6403	3C4	2296.0101	CAP MICA 500V 1%	100pF
C6404	3C5	2296.0471	CAP MICA 500V 1%	470pF
C6501	3D5	2296.0101	CAP MICA 500V 1%	100pF
C6502	3C5	2296.0471	CAP MICA 500V 1%	470pF
C6503	2D6	2932.0476	CAP AL-EL 25V 20%	47uF
D1101	1H2	3110.4152	DIODE SIGNAL	4152
D1401	1C7	3120.0000	DIODE SCHOTTKY	1SS97
D1501	1G5	3110.4152	DIODE SIGNAL	4152
D2101	1G2	3110.4152	DIODE SIGNAL	4152
D2501	1H5	3110.4152	DIODE SIGNAL	4152
D3501	3F2	3110.4152	DIODE SIGNAL	4152
D4501	3G2	3110.4152	DIODE SIGNAL	4152
D4502	2F7	3110.4152	DIODE SIGNAL	4152
D4503	2F7	3110.4152	DIODE SIGNAL	4152
P111	1C1-1H1	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P141	1G1	4221.0172	PLUG PC 90' 2X.1 X.39	72 PIN
P251	1G8,2C8,3F1	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
Q2301	1E6	3211.2222	XSTR NPN TO92	PN2222A
Q3201	2H1	3211.2222	XSTR NPN TO92	PN2222A
Q3401	1F7	3214.5432	XSTR FET TO92	PN5432
Q4301	2A2	3214.5432	XSTR FET TO92	PN5432
Q4302	2G6	3214.5432	XSTR FET TO92	PN5432
Q5301	2F6	3214.5432	XSTR FET TO92	PN5432
Q5401	2H6	3214.5432	XSTR FET TO92	PN5432
Q5402	2C7	3214.5432	XSTR FET TO92	PN5432
Q5501	3E6	3214.5432	XSTR FET TO92	PN5432
Q6401	2D7	3214.5432	XSTR FET TO92	PN5432
R1101	1G2	1214.0102	RES 1/4W C FLM 5%	1K
R1401	1B6	1136.2370	RES 1/8W M FLM 1%	237
R1402	1C7	1136.2002	RES 1/8W M FLM 1%	20.0K
R1403	1C8	1136.1961	RES 1/8W M FLM 1%	1.96K
R1501	1F8	1139.2001	RES 1/8W M FLM .1%	2.00K
R1502	2G7	1214.0229	RES 1/4W C FLM 5%	2.2
R1503	1H5	1139.1001	RES 1/8W M FLM .1%	1.00K
R1504	1H5	1136.2740	RES 1/8W M FLM 1%	274
R2101	1G2	1214.0203	RES 1/4W C FLM 5%	20K
R2102	1E2	1214.0470	RES 1/4W C FLM 5%	47
R2301	1E5	1214.0103	RES 1/4W C FLM 5%	10K
R2302	1E6	1214.0104	RES 1/4W/C/FLM 5%	100K
R2401	1E7	1214.0101	RES 1/4W C FLM 5%	100
R2402	1E7	1139.9981	RES 1/8W M FLM .1%	9.98K
R2403	1E7	1136.1000	RES 1/8W M FLM 1%	100
R2404	1E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2405	1G6	1214.0203	RES 1/4W C FLM 5%	20K
R2406	1G6	1214.0470	RES 1/4W C FLM 5%	47
R2501	1H4	1136.2740	RES 1/8W M FLM 1%	274
R2502	1H4	1136.1211	RES 1/8W M FLM 1%	1.21K
R3201	1E5	1214.0472	RES 1/4W C FLM 5%	10K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R3203	1F5	1214.0102	RES 1/4W C FLM 5%	1K
R3204	2H3	1214.0472	RES 1/4W C FLM 5%	4.7K
R3205	2G1	1214.0472	RES 1/4W C FLM 5%	4.7K
R3206	1G5	1214.0104	RES 1/4W/C/FLM 5%	100K
R3207	2G1	1214.0101	RES 1/4W C FLM 5%	100
R3208	2G2	1214.0103	RES 1/4W C FLM 5%	10K
R3301	2F8	1214.0102	RES 1/4W C FLM 5%	1K
R3302	3D3	1136.1152	RES 1/8W M FLM 1%	11.5K
R3401	1D7	1214.0104	RES 1/4W/C/FLM 5%	100K
R3402	1F7	1214.0203	RES 1/4W C FLM 5%	20K
R4301	2F5	1136.5490	RES 1/8W M FLM 1%	549
R4302	2F6	1139.9981	RES 1/8W M FLM .1%	9.98K
R4303	2F5	1139.1502	RES 1/8W M FLM .1%	15.0K
R4304	2F6	1214.0203	RES 1/4W C FLM 5%	20K
R4401	2F8	1214.0102	RES 1/4W C FLM 5%	1K
R4402	1G6	1214.0472	RES 1/4W C FLM 5%	4.7K
R4501	3G2	1136.4990	RES 1/8W M FLM 1%	499
R4502	3H2	1136.1371	RES 1/8W M FLM 1%	1.37K
R5301	2C2	1214.0103	RES 1/4W C FLM 5%	10K
R5302	2E5	1136.1072	RES 1/8W M FLM 1%	10.7K
R5303	2E5	1136.1072	RES 1/8W M FLM 1%	10.7K
R5304	2E6	1214.0203	RES 1/4W C FLM 5%	20K
R5401	2H6	1214.0203	RES 1/4W C FLM 5%	20K
R5402	2G6	1139.1502	RES 1/8W M FLM .1%	15.0K
R5403	2G8	1136.3012	RES 1/8W M FLM 1%	30.1K
R5404	2C7	1214.0203	RES 1/4W C FLM 5%	20K
R5405	2B7	1214.0203	RES 1/4W C FLM 5%	20K
R5406	3D3	1136.5231	RES 1/8W M FLM 1%	5.23K
R5407	3D3	1136.5231	RES 1/8W M FLM 1%	5.23K
R5501	3D6	1214.0203	RES 1/4W C FLM 5%	20K
R5502	3D4	1214.0133	RES 1/4W C FLM 5%	13K
R5503	3G2	4412.0201	POT TRIM PC ENC	200
R6101	2A1	1136.3482	RES 1/8W M FLM 1%	34.8K
R6102	2B2	1136.6192	RES 1/8W M FLM 1%	61.9K
R6103	2B2	1136.4991	RES 1/8W M FLM 1%	4.99K
R6104	2B2	1136.4991	RES 1/8W M FLM 1%	4.99K
R6105	2B3	1136.8061	RES 1/8W M FLM 1%	8.06K
R6106	2A3	1136.6191	RES 1/8W M FLM 1%	6.19K
R6201	2A4	1136.2671	RES 1/8W M FLM 1%	2.67K
R6202	2B4	1136.4872	RES 1/8W M FLM 1%	48.7K
R6203	2A4	1136.2871	RES 1/8W M FLM 1%	2.87K
R6204	2A5	1136.2261	RES 1/8W M FLM 1%	2.26K
R6301	2A5	1136.1072	RES 1/8W M FLM 1%	10.7K
R6302	2A5	1139.1001	RES 1/8W M FLM .1%	1.00K
R6303	2B6	1136.3651	RES 1/8W M FLM 1%	3.65K
R6304	2B6	1136.2491	RES 1/8W M FLM 1%	2.49K
R6401	2B6	1136.5361	RES 1/8W M FLM 1%	5.36K
R6402	2G6	1136.4991	RES 1/8W M FLM 1%	4.99K
R6403	2D6	1136.2491	RES 1/8W M FLM 1%	2.49K
R6404	2A7	1136.6980	RES 1/8W M FLM 1%	698
R6405	3D3	1139.4001	RES 1/8W M FLM .1%	4.00K
R6406	3D4	1139.4001	RES 1/8W M FLM .1%	4.00K

REPLACEABLE ELECTRICAL PARTS LIST: 9BUR.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R6407	3D4	1136.1371	RES 1/8W M FLM 1%	1.37K
R6408	2A7	1136.1372	RES 1/8W M FLM 1%	13.7K
R6501	2D6	1136.1101	RES 1/8W M FLM 1%	1.10K
R6502	3D5	1136.1501	RES 1/8W M FLM 1%	1.50K
R6503	3D5	1136.2431	RES 1/8W M FLM 1%	2.43K
R6504	2A8	1136.4991	RES 1/8W M FLM 1%	4.99K
R6505	2D6	4412.0201	POT TRIM PC ENC	200
R6506	2A7	4412.0201	POT TRIM PC ENC	200
U111	2D1,2D3	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U121	1C1	3332.8254	TIMER INTERVAL PROG	82C54
U131	1B5	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U132	1B5	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U141	1B6	3510.7523	MDAC 8 BIT	AD7523
U142	1C7,1F8	3412.0353	OP AMP DUAL	TL072/LF353
U151	1H5	3430.1317	VOLT REG POS VAR TO92	LM317L
U211	1F2	3324.0138	DECODER 3LINE/8LINE	74HCT138
U221	1C2,1C3,1E6,3E3	3313.0125	BUFFER 4X TRI-STATE	74LS125
U222	1A3,1B3,1E4	3324.0011	GATE 3X 3-IN AND	74HCT11
U231	1A4	3324.0138	DECODER 3LINE/8LINE	74HCT138
U232	1E5,3C2	3324.0074	FLIP-FLOP 2X D	74HCT74
U241	1G6,1G7	3412.0353	OP AMP DUAL	TL072/LF353
U242	2D7	3323.4053	MULTILPLEX 2X TRIP	HC4053
U251	1H3	3431.1337	VOLT REG NEG VAR TO92	LM337L
U311	1H2,2D4,2E4,2F1	3323.0132	GATE4X2-IN NAND SCHMT	74HC132
U312	1C3,1D2,2E3,3C2	3323.0002	GATE 4X2-IN NAND	74HC02
U331	1G2,1F5	3422.0319	COMPARATOR	LM319
U351	3G2	3430.1317	VOLT REG POS VAR TO92	LM317L
U411	2F4	3323.0164	SHFT REG SERIAL-PARA	74HC164
U412	2F3	3323.0164	SHFT REG SERIAL-PARA	74HC164
U421	2F2	3323.0164	SHFT REG SERIAL-PARA	74HC164
U422	2G4	3323.0280	PARITY CHECKER 9 BIT	74HC280
U431	2F6,2H1	3412.0082	OP AMP DUAL	MC34082
U441	2C2,2C7,2E6,2G5	3424.0339	COMPARATOR QUAD	LM339
U442	1F6,2B7,2C7,2H5,3E5F7	3424.0339	COMPARATOR QUAD	LM339
U531	2D6,2H6	3412.0353	OP AMP DUAL	TL072/LF353
U551	3D4,3D5	3412.0082	OP AMP DUAL	MC34082
U611	2B2,2B4	3412.0082	OP AMP DUAL	MC34082
U631	2B5,2C7	3412.0082	OP AMP DUAL	MC34082


R0401
TP1001
TP6001
TP9203
R9001
R9101
R9102
R9103
R9201
R9202
R9301
C9405
R9601
C9701

LVF-2, ANALYZER MODULE

The LVF-2 module contains the Channel-A input stage, bandwidth limiting filters, option filter sockets, "Reading" meter with selectable detectors, and frequency counter. The ranging circuits, voltmeter readings, and frequency counter are controlled by a 6805 microprocessor.

Interface Logic <1>

The data bus from the host computer enters via the 40-pin cable connector and is buffered by U101. After buffering the data bus is designated the "D" bus. The data bus of the 6805 microprocessor is designated the "C" bus to distinguish it from the host data bus. Address information also enters via the 40-pin cable connector and drives the appropriate decoding circuits. The address lines from the host are labeled "A" and the 6805 address lines are labeled "B".

The D bus drives the data latches on the board which receive settings information for filters, detectors, and input configuration. The D bus is also connected to a dual port RAM constructed by eight 4-bit-by-4 register files, U111, U211, U311, U411, U112, U212, U312, U412. These contain four 4-bit latches and address decoding logic so that the inputs of the four latches may be written to independently of the reading of the outputs at the other side. Inputs are labeled "xD", outputs are labeled "xQ". The RAM is allocated as follows:

TABLE LVF2.1
DUAL PORT RAM ALLOCATION

IC#	ADDRESS	FUNCTION
111, 212	0 - 3	range information to host
211, 312	4 - 7	frequency reading
311, 412	8 - 11	measure and phase readings
411	12 - 15	readings counters
112	0 - 3	reading rate & range info to 6805

The module address, normally set to 0, is decoded by a 4-bit comparator U601. When a match is found the output goes high, driving the output of Q4101 low and signaling the host that the board is present. The output of U601 also drives U221, a dual 2-to-4 line decoder. The upper half decodes the read addresses of the dual port RAM (pins 9-12). The other half decodes the write addresses, one bank of four enables RAM U112 while another bank of four goes to U241 for further decoding. The first three outputs of U241A drive the settings latches. The fourth, labeled /INT, drives the 6805 interrupt line. Whenever this is strobed the processor will abandon its current task and begin a new reading cycle.

Power-on resets are latched by U181A so that correct range and reading rate information may be written to the dual port RAM before the 6805 begins its readings cycle. The reset state is cleared by the strobing of the /INT line.

U141 latches the input relay settings, A/B selection and phasemeter range from the host. Only six of the eight bits are latched. The remaining two are used to enable the input 600 Ohm or 150 Ohm termination resistors. These are latched in individual flip-flops so they may be reset by an input overload condition without affecting the other seven bits.

Microprocessor <2>

The 20 MHz master clock is divided down by U121 to provide both a 4 MHz clock to the 6805 and a 5 MHz clock to the frequency counter. The 6805 microprocessor contains onboard EPROM and RAM and does not use the external pins for address or data information. All of the pins are latched and are used only for accessing peripheral ICs for reading or writing data. The eight lines on pins 12 through 19 are used as a bidirectional data bus and are labeled C0 through C7. Pins 20 through 24 are used as an address bus and are labeled B0 through B4. Read and write strobes appear on pins 26 and 25 respectively. They go low to read or write data on the C bus from or to the address selected by the B bus.

The 6805 executes a program loop which involves a sequence of steps which are always executed in the same order. When the processor finishes the steps in the loop it waits until it is time to begin the loop again. This timing is set by an internal counter which divides the master clock and interrupts the processor. This occurs at approximately 32.77 msec intervals, corresponding to the fastest reading rate of the voltmeters. This also sets the rate at which the ranging comparators are sampled and all other tasks are completed.

When the processor is busy performing operations it sets the CYCLE test point (pin 27) high. When it is waiting for another timer interrupt it sets the CYCLE test point low. Many of the tasks the 6805 must perform are not performed every time through the loop. For example, at reading rates slower than 32 rdg/sec the voltmeters and frequency counter will not be serviced every time through the loop. At 16 rdg/sec the voltmeters will be serviced once every two times through the loop. At 8 rdg/sec they will be handled every four times and at 4 rdg/sec it will be every eight times.

The frequency counter is slightly more complicated because it must also wait for zero crossings of the input signal before it may be serviced. At input frequencies above approximately 2 kHz the processor will not have to wait for zero crossings. At lower frequencies there may be an additional loop service required to obtain a counter reading. These factors make the signal at the CYCLE test point vary with reading rate and input signal. However, for diagnostic purposes the reading rate may be set to 32 and a high frequency input signal applied. The display should be a stable pulse train at a 32.8 msec rate. As the reading rate is reduced the display should show a change in pulse width every 2, 4 or 8 pulses at 16, 8 and 4 rdg/sec, respectively.

All voltmeters are implemented with voltage to frequency (V-F) converters whose outputs are counted to obtain the reading. This counting is performed by a triple counter peripheral IC U022. It contains three 16-bit counters which may be programmed and read by the processor. They count the number of pulses at their clock inputs during the time that their gate inputs are high. To read them the processor sets PC3 low which drives the gate low and stops the counting. When the read operation is finished they are reset and the gate is returned high. The count thus obtained for any given input voltage will vary by factors of two depending on the reading rate selected. This is corrected by the 6805 before the data is passed to the host.

The frequency counter is a reciprocating period based counter. The input signal and a master clock are counted for the desired number of 32.77 msec intervals. The resulting counts are divided and scaled to produce the frequency value. These counters are also implemented with a triple 16-bit counter peripheral IC, U021. One section is used to count the input signal and two are cascaded to count the 5 MHz master clock. A 16-bit counter is not large enough to handle all the counts at maximum frequency and the slowest reading rates. The overflow is counted by U121D.

Flip-flop U251B is used to synchronize the two counters to guarantee that the master clock is counted between an integer number of input signal cycles. Its output drives the gate input of the two counter chains and an status input (PC1) on the processor. The input signal is applied to the appropriate counter and to the clock input of the flip-flop.

Autorange Comparators <3>

The signal from the channel A input amplifier is fed through the preemphasis network R4512, R4511, C4501. This compensates for the slew rate limitations of the op-amps in the preamplifier, reducing amplitude of signal at high frequencies before an up-range occurs. This signal feeds four comparators, two sense the need to up-range and two sense the need to downrange. The two comparators in each pair are used to sense the positive peak value and negative peak value of the signal.

Consider the operation of U361B. Its negative input is connected to the signal input and its positive input is connected to a +1.75 V reference. The output of the comparator will go low when positive signal peak exceeds this reference. U361A performs the same comparison function for negative peaks. The outputs of the two comparators are wired together. Since these are open collector outputs, if either comparator senses too large a peak value the output line will go low. R3504 and RP261 level shift the -15 V output of the comparators to the +5 V logic of U271A. When the comparator output goes low it will set the flip-flop U271A. The microprocessor reads the output of this flip-flop through tri-state buffer U151 and knows if an overrange condition occurred. When the microprocessor reads this information the clock input of U271A is strobed, clearing the overrange indication. The flip-flop allows momentary signal overloads to be detected with infrequent monitoring by the microprocessor.

Comparators U361C and U361D perform the same comparison function on the signal at a 6 dB lower amplitude. If the signal is below this level the microprocessor knows that the input gain must be increased. When the correct input range is achieved the upper comparator output will be high and the lower comparator output will be low. Any change of state in the comparators causes an uprange or downrange as appropriate. Quad comparators U351 and dual flip-flop U261 perform the same level comparison functions on the range amplifier signal.

Comparators U371C and U371D monitor the signal level against a 100 mV reference. This is used to sense when the signal is of insufficient amplitude to guarantee accurate phasemeter operation. When this occurs the output of the comparators will rise. This signal must remain under this minimum level until C3601 charges for the processor to shut down the phasemeter reading.

Tri-state buffer U151 allows the microprocessor to read the state of various logic signals on the phasemeter board. In addition to the three range comparison signals described above, the state of the Channel A input termination resistors (/TERMA) and the channel selection signal (A/B) are monitored.

Frequency Counter Comparator <3>

The Channel A signal enters through R4408. When line LB goes to 0 V, JFET switch Q4402 connects the grounded capacitor C4406 and forms a lowpass filter to reduce the effects of noise and interfering components above 100 kHz. These signals are buffered by U544 which drives the comparators and peak detectors.

Diodes D4403 and D4404 cause the output of U544 to be offset from the input by one diode drop. For positive signal voltages the output will be 0.6 V higher than the input, for negative voltages the output will be 0.6 V lower than the input. This output signal is rectified by diodes D4401 and D4402. The positive voltage from D4402 is stored on capacitor C4404 and serves as the positive threshold reference for the comparators. The negative voltage from D4401 is stored on capacitor C4405 and serves as the negative reference for the comparators. The input signal is developed across RP341 and fed to the two comparators in U342. Each comparator compares the signal to a different reference, one to each of the two references discussed above.

Series resistor-capacitor networks R4404-C4408 and R4403-C4407 provide hysteresis to prevent oscillation on the comparator transitions without disturbing the dc value of the reference voltage. The outputs of the comparators are used to drive flip-flop U251A. The use of separate comparators to compare the zero crossing and the peak provides a large amount of hysteresis and reduces the sensitivity of the counter to interfering noise.

Lowpass filter R3501 and C3501 create the average value of the comparator output. This is compared to TTL thresholds by buffer U151. This creates a duty cycle comparison and is used to derive the polarity information for the polarity function of the analyzer.

Input Circuit <4>

The input signal is derived from the panel connectors or the internal generator monitor path via relays K481 and K581. Relays K481 and K581 are ganged together to provide optimum input isolation when monitoring the generator output. P681 connects to a shielded cable originating on the channel A output of the generator.

Relay K891 selects the 600 Ohm and 150 Ohm terminations. Its control bit originates from the Q output of flip-flop U181B. When a termination is selected the flip-flop Q output clocks high and causes relay K891 to be energized through Q3802. Relay K591 provides 600/150 Ohm selection. In the 600 Ohm selection, relay K591 is open and the termination is composed of resistors R7902-R7904 and R4902. R7901 shunts the 600 Ohm termination to obtain the 150 Ohm termination (300 Ohms in units with option EURZ).

The terminations are protected against excessive power dissipation by sensing a small portion of the total input voltage through the divider action of R7903, R4902, and R7904 and the ac optocoupler U491. An input level greater than approximately +32 dBu (30 Vrms) will forward bias the light-emitting diodes inside U491. This causes the phototransistor inside U491 to conduct, thus clearing the control flip-flop U181B and de-energizing relay K891.

The selected input signal passes through RF suppression filters composed of R6801, C6801, R6802, and C6802. In some units C6801 or C6802 may be shunted with a small capacitor to balance the total input capacitance. The signal is then ac-coupled to the input attenuators through C8801 and C8802. C8801 and C8802 are matched for optimum low frequency common mode rejection and must be replaced as a set.

The input attenuators provide four 12 dB steps from 0 dB to -36 dB. Relay K571 is energized in the 0 dB state, K572 for -12 dB, and K672 for -24 dB. -36 dB is the default range with all relays off. Refer to TABLE LVF2.2 for information concerning attenuator selection versus input voltage. C9701 adjusts the attenuator high frequency flatness above approximately 10 kHz. R7705 and R8709 trim the total input resistance to be 100 kOhms, each side to ground.

Signal Preamp <5>

The selected and attenuated input signal is buffered and amplified by U762, U761, U752, and U551. Diodes D5601-5604, and D5607-5610 provide overload protection by clamping the op-amp input voltage to approximately ±13 V, determined by zener diodes D5605 and D5606. High frequency distortion due to the non-linear capacitance of the diodes is minimized by the inherent bootstrap action of this configuration.

NOTE: The residual leakage current of the input clamping diodes can exhibit significant optical modulation. Exposure to fluorescent lighting with the top cover removed may cause an increase in input hum products due to this effect!

When no attenuation has been selected the incandescent lamps R471 and R472, located on schematic <4>, limit input current during an overload condition. Normally the lamps present a low resistance (typically 100-130 Ohms) to the input circuit. During an overload the lamp resistance rises dramatically.

The pre-amplifier gain is controlled by relays K671 and K771, providing +12 dB and +6 dB steps respectively. If both are energized the preamp gain is +18 dB. K651 switches an additional +12 dB gain stage comprising U551, R5501, and R5502 for higher sensitivity. See TABLE LVF2.2 for more information.

TABLE LVF2.2
CHANNEL-A INPUT RANGES & SYSTEM GAIN

RANGE[1]	ATTENUATION	K571	K572	K672	PREAMP GAIN	K771	K671	K651	TOTAL GAIN[2]
160 V[3]	-36dB	0	0	0	0dB	0	0	0	-36dB
80 V	-36dB	0	0	0	+6dB	1	0	0	-30dB
40 V	-24dB	0	0	1	0dB	0	0	0	-24dB
20 V	-24dB	0	0	1	+6dB	1	0	0	-18dB
10 V	-12dB	0	1	0	0dB	0	0	0	-12dB
5 V	-12dB	0	1	0	+6dB	1	0	0	-6dB
2.5 V	0dB	1	0	0	0dB	0	0	0	0dB
1.2 V	0dB	1	0	0	+6dB	1	0	0	+6dB
600 mV	0dB	1	0	0	+12dB	0	1	0	+12dB
300 mV	0dB	1	0	0	+18dB	1	1	0	+18dB
160 mV	0dB	1	0	0	+24dB	0	1	1	+24dB
80 mV	0dB	1	0	0	+30dB	1	1	1	+30dB

1 Maximum rms sinewave amplitude for linear operation.
2 INPUT to ASIG
3 140 Vrms is the maximum rated input voltage

U752 is a unity gain differential input to single ended output amplifier. Common mode rejection is trimmed by R9601 which balances the + and - input signal path gains. U651 and its related components comprise a dc servo that maintains a near zero dc offset condition at the output of U752 under all gain conditions. The output of the integrator is fed back through R8507 into the + signal path. C5502 and R5505 provide low frequency compensation that corrects for the input ac coupling rolloff below about 30 Hz.

The output signal from relay K651 is labeled ASIG and is routed several places. It is connected to the channel A input ranging comparators shown on schematic <3>, J461-6 (to the dual input/phasemeter board), and to the ASIG monitor buffers U571A and U571B. The output from U571A is connected through R8502 and a shielded cable to the front panel CHANNEL A MONITOR connector. Note that there is a 6 dB loss introduced by R8504 and R8503. U751B provides the ASIG source in SYS-2xx and SYS-3xx configurations. Under normal conditions of autoranging the peak value of ASIG will vary over a 6-7 dB window between approximately 1.60-3.75 Vpeak.

In the SYS-11 configuration only a jumper is inserted between pins 6 and 8 of J461 to connect ASIG to MAINSIG because the PHA-2 board is not present.

Range Amp & Lowpass Filters <6>

MAINSIG is routed to J951-7 connecting to the DIS-2 module. FUNCSIG is the selected signal to be passed to the main voltmeter and CNTRSIG is the signal presented to the frequency counter. In the amplitude measurement mode FUNCSIG is connected directly to MAINSIG via a relay on the DIS-2 module.

FUNCSIG is connected to the Range Amp stage consisting of a programmable 0 dB to -48 dB attenuator and a fixed +20.6 dB gain (x11) amplifier U741. CMOS switch U742 selects one of five 12 dB attenuator steps. U742 is controlled by three bits originating from Q2-Q4 of data latch U171. U741 is operated non-inverting to prevent loading on U742. C9405 adjusts high frequency flatness above approximately 50 kHz.

TABLE LVF2.3
RANGE AMPLIFIER SWITCHING

AMPLITUDE RANGE	ATTEN	U742 A	U742 B	U742 C	ADDED GAIN
≥80 mV	-48 dB	0	1	1	0 dB
20 mV	-36 dB	1	0	0	+12 dB
5 mV	-24 dB	1	0	1	+24 dB
1.2 mV	-12 dB	1	1	0	+36 dB
300 uV	0 dB	1	1	1	+48 dB

The output of the range amp U741 becomes the input to the lowpass bandwidth limiting filter stage. This stage provides four selections of high frequency rolloff including flat (">500 kHz"), 80 kHz, 30 kHz, and 22 kHz. In the flat state the upper -3 dB point is typically 600-700 kHz.

The 80 kHz and 30 kHz filters have 3-pole Butterworth response and are composed of U543A and U543B respectively. Typical -3 dB frequency accuracy is 3% (5% specified). The 22 kHz filter U541A is cascaded from the output of the 30 kHz filter to provide a 6-pole response with a sharper rolloff beyond the audio spectrum. Its -3 dB point is approximately 22.4 kHz and the response shape has been optimized to conform to CCIR Recommendation 468 for unweighted measurements. The CMOS MUX U542 selects the desired lowpass filter and is buffered through U541B. U541B also provides approximately +7 dB of gain. Filter selection is controlled by two bits originating from data latch U421, outputs 5Q and 6Q.

The output of the range amp U741 also drives an inverting amplifier composed of U544A, R6411, and R6412. This provides the signal (RANGESIG) that is routed to the comparators on schematic <3> for autoranging control of U742. When properly operating the peak output of the range amp U741 will vary over a 12-13 dB window between approximately 35-160 mV; and the output of the lowpass buffer U541B will vary between approximately 70-340 mV peak.

U841 and U842 provide regulated ±6 Volts to operate the CMOS MUXs on schematics <6> and <7>. The accuracy of these supplies is not critical to instrument calibration. The regulator ICs contain over-dissipation and current limiting protection.

Option & Highpass Filters <7>

LPSIG is the output from the lowpass bandwidth limiting filter stage and is connected to pin 8 of option filter sockets J801, J811, J812, J813, and J814. Option filters derive their input from this signal. The outputs are connected to pin 2 of their respective socket, and selected by the CMOS MUX U521. The three control bits labeled WA, WB, and WC originate from the 3Q, 4Q, and 7Q outputs of data latch U421 located on schematic <6>. When all bits are low (0V) a bypass path is selected for no option filtering.

LPSIG also drives buffer amplifier U622B which provides the front panel EXT FILTER OUTPUT signal through a cable connected to P621. The front panel EXT FILTER INPUT is connected through P622 and overload protection resistor R6201 to the selection MUX U521.

The option filter buffer U512A provides unity gain and a low impedance source to the following highpass filter stage. R5102 and diodes D5101-D5102 limit the maximum signal amplitude during ranging transients to minimize settling time. Under normal conditions of autoranging the peak signal will not exceed approximately 340 mV, unless the external or option filters exhibit greater than unity gain.

The highpass bandwidth limiting filter stage comprises U512B, CMOS MUX U511, and related circuitry. Four selections are provided including flat (<10 Hz), 22 Hz, 100 Hz, and 400 Hz. The 100 Hz and 400 Hz filter responses are 3-pole Butterworth with a typical -3 dB frequency accuracy of 3% (5% guaranteed). The 22 Hz response is also 3-pole but has been optimized to conform to the requirements of CCIR Rec 468. R9001 adjusts the flatness above 50 Hz of the 22 Hz filter. R6100, R7100, and R5101 provide gain compensation to correct for stray capacitive loading effects in the filters.

The output of the highpass bandwidth limiting filter is coupled through C5001 to the last gain stage composed of U701 and related components. This gain stage has about +20.6 dB of gain (x11) and drives the ac-dc detectors. The signal amplitude at this point typically varies between 0-3.7 Vpeak, however significantly higher peak amplitudes may be present depending upon the exact signal and filter selection. R9101 adjusts the READSIG offset and R9102 adjusts low frequency flatness below 20 Hz.

U821A provides a buffered replica of READSIG for external monitoring. The output of U821A is coupled through R8201 and a shielded cable to the front panel READING MONITOR OUTPUT connector. U821B provides a buffered signal to the DSP module, if installed. R7201 and R7202 provide a 6 dB loss and a convenient node to couple the output signal OPTSIG from the Wow & Flutter option.

RMS, AVG, & PEAK Detectors <8>

The final processed signal, READSIG from <7>, is applied to the rms detector, U822 (Analog Devices AD637), and a precision full-wave rectifier for the average and peak detection modes. The rms detector integration time constant is determined by C8302, C4301, C4302 and controlled by one half of CMOS switch U431. R8301 adjusts the offset error term of the rms detector. The rms detector output at U431-13 is normally 0 to +2.6 V. D8301, R8302, and R8303 provide clamping to minimize settling time from ranging transients. R3302, R3304, C3301, and C3302 form a 2-pole lowpass filter to reduce the ac ripple content in the detector output dc voltage. The output of this network is applied to one of the inputs of the detector selection MUX U331.

U731A and U731B comprise a precision full-wave rectifier used for the AVG, Q-PEAK, S-PEAK, and PEAK modes of detection. R9301 adjusts the rectifier balance and is adjusted for equal amplitude peaks at TP9203 with a low level sinewave signal. R9201 adjusts for the offset error term while R9103 trims the rectifier gain. D7201 and D7202 clamp the rectifier output to minimize overload recovery from ranging transients.

Average detection is accomplished by filtering the full-wave rectified signal. Filter networks R5302-R5303-C5301-C5302, R5304-R5305-C5303-C5304, and R5306-R5307-C5305-C5306 provide three different integration time constants selected by half of CMOS MUX U431. The integration time constants are selected by two control bits originating from 5Q and 6Q of data latch U321, and are ganged to the reading rate selection.

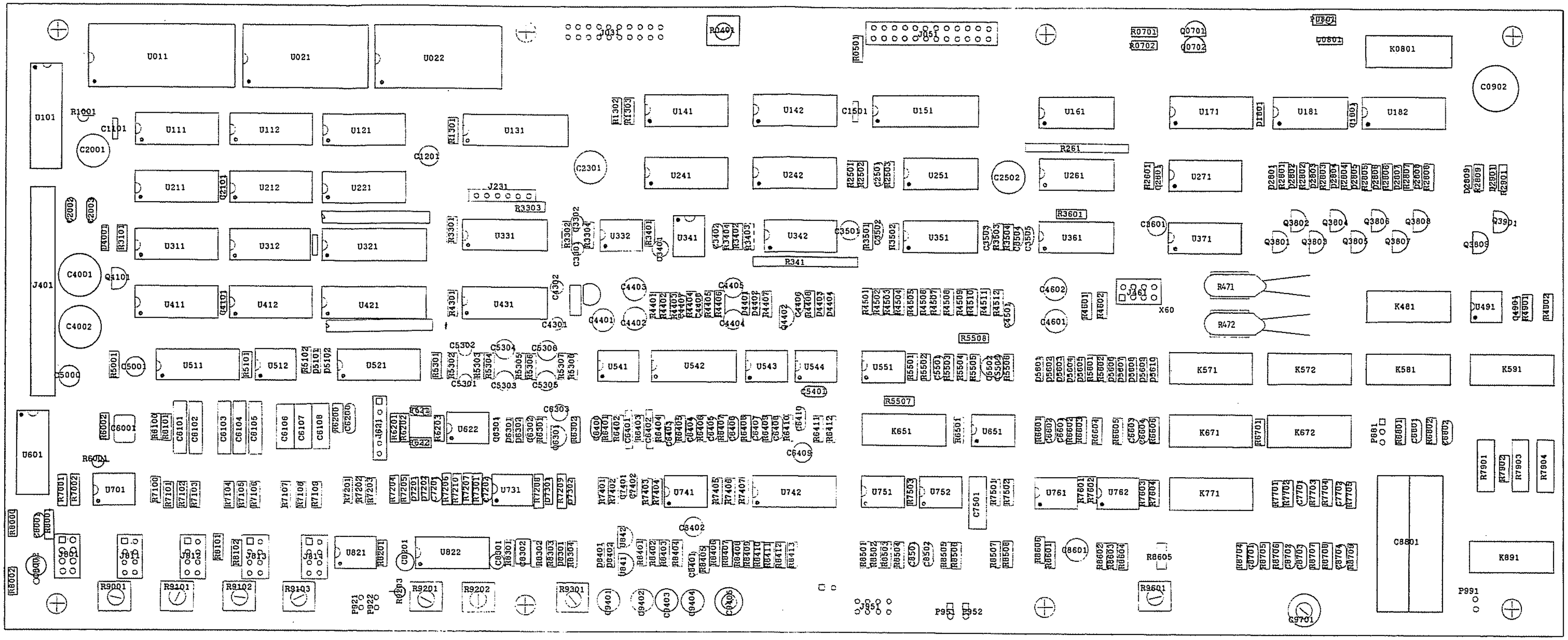
The Q-PEAK and PEAK detector is composed of U622A and buffer U322B. The S-PEAK detection mode is identical to PEAK except that readings are scaled by 0.7071 (in software) to read the rms equivalent of a sinewave with the same peak value. U622A and D6301-D6302, R6301-6302, and C6303 form a fast attack-slow decay peak detector that captures the peak value of the full-wave rectifier output. When Q6301 is off, R6302 is effectively in series with C6303 and increases the attack time to achieve the proper quasi-peak detector response. The output of buffer U322B is attenuated slightly and filtered by R4301, R3301, and C4403 to scale the output dc voltage and provide the correct ballistic response required by CCIR Recommendation 468. When Q6301 is on, the series resistance becomes very small resulting in a very fast attack time with almost ideal peak detection for repetitive signals. R6301 determines the decay time constant which is approximately 300 msec with any of the peak detector selections.

MUX U331 selects the output of the rms detector, the selected average detector integration network, the quasi-peak/peak detector output, or the output from J231-1 and J231-5 used with the Wow & Flutter option. The MUX is buffered with U332A and provides feedback for the various rms and average detector filter networks. The buffer output is additionally filtered through R3401 and C3401 before being presented to the voltage-to-frequency converter, U341.

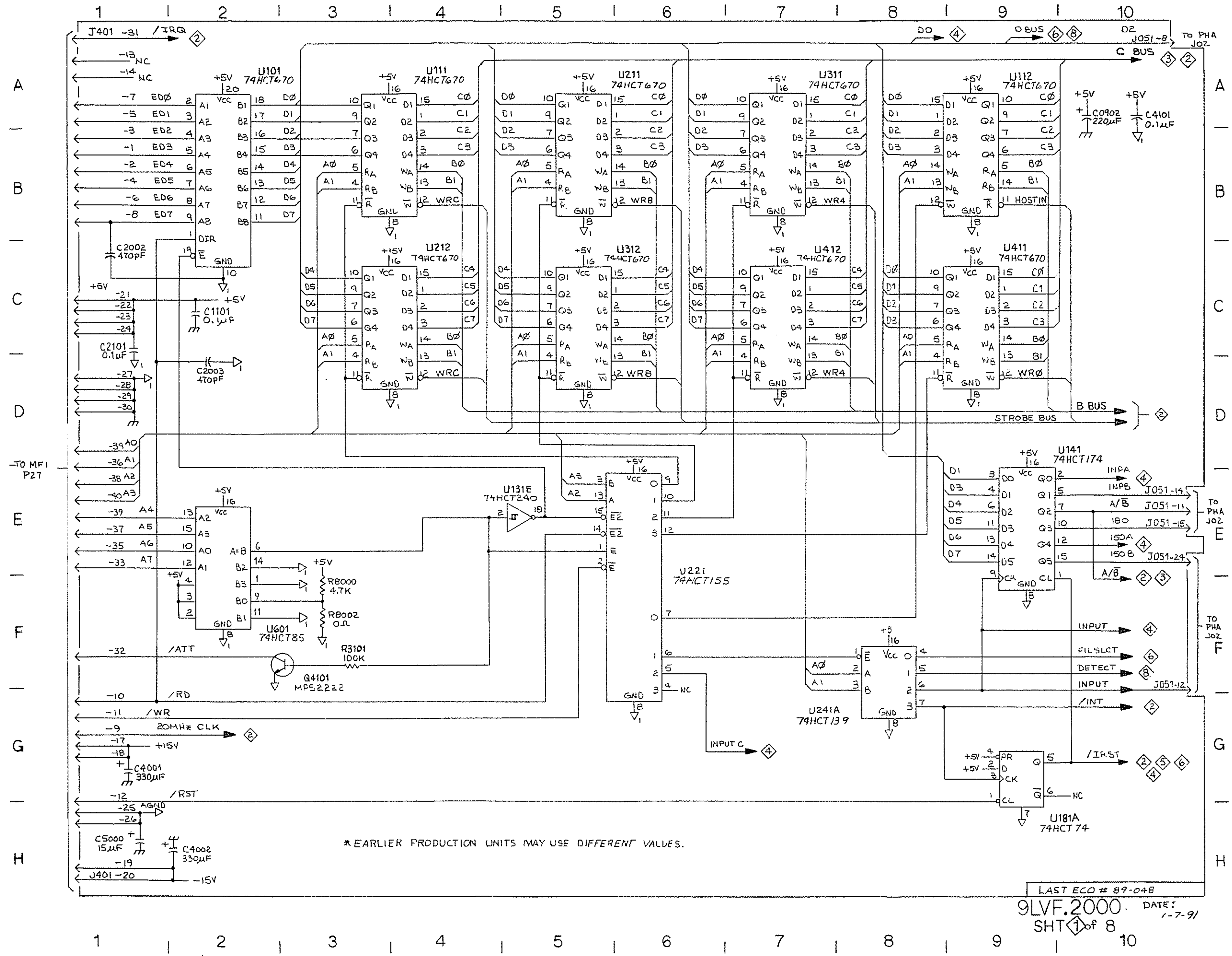
Voltage measurements are accomplished by measuring the output frequency of a voltage-to-frequency (V-F) converter. This technique offers superior noise integration and permits reading rate selection by switching the frequency counter gate interval. The V-F converter is a monolithic IC (AD654) that outputs a TTL compatible squarewave whose frequency is a linear function of the input dc voltage. A nominal 2.5-2.6 Vdc input produces a 100 kHz "full scale" output frequency. R0401 adjusts for gain tolerances in the V-F converter and its timing capacitor C3402. R3403 is selected to center the adjustment range of R0401. R3404 improves the noise immunity of the converter at very low levels. TABLE LVF2.4 gives the approximate full scale resolution as a function of reading rate.

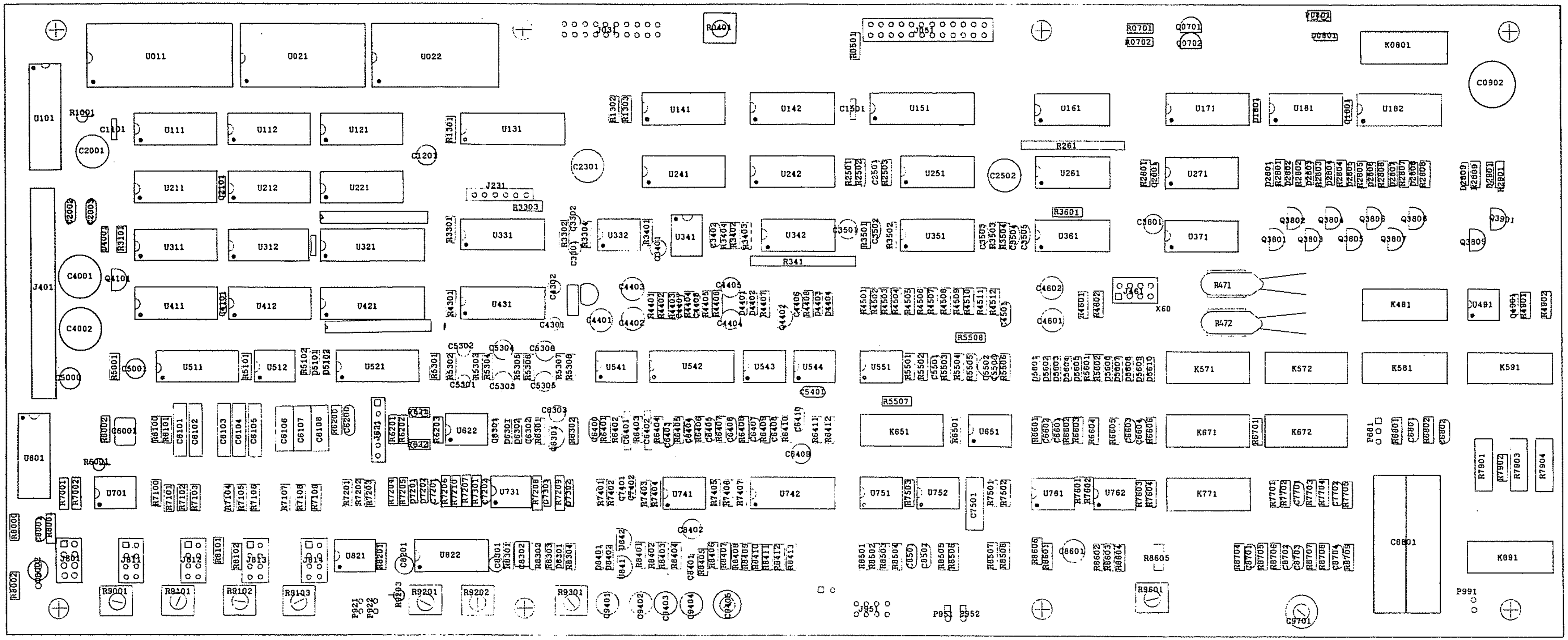
TABLE LVF2.4
DETECTOR RESOLUTION VERSUS READING RATE

READING RATE	COUNTER INTERVAL	FULL SCALE RESOLUTION
32/sec	32.77 msec	1/3150
16/sec	65.5 msec	1/6300
8/sec	131.1 msec	1/12600
4/sec	262.1 msec	1/25200

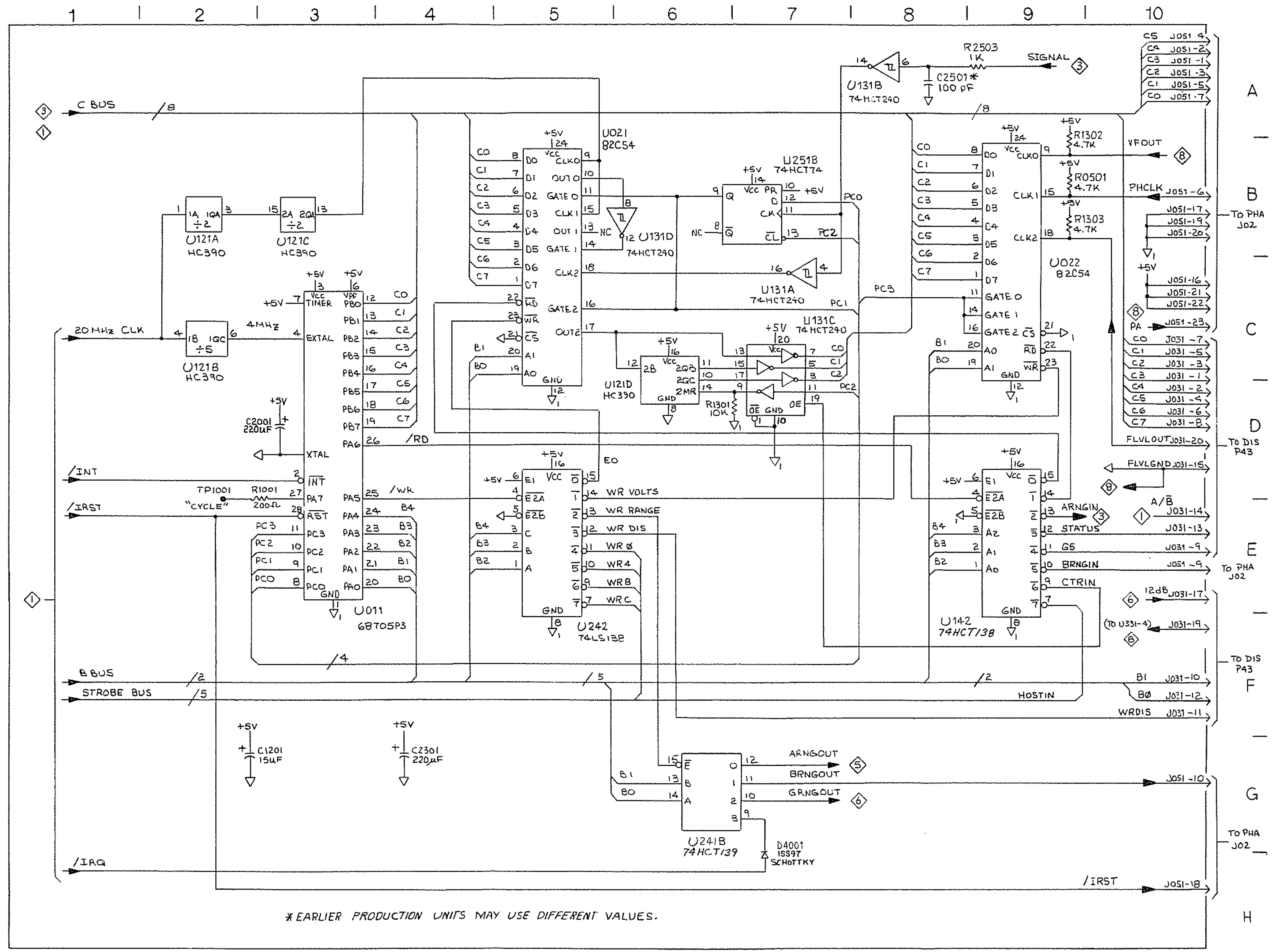


ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)


J401
/IRQ
U101 74HCT670
U111 74HCT670
U211 74HCT670
U311 74HCT670
U112 74HCT670
U212 74HCT670
U312 74HCT670
U412 74HCT670
U411 74HCT670
C BUS
D0
D BUS
J051-8
TO PHA J02
C0902 220µF
C4101 0.1µF
C2002 470pF
C1101 0.1µF
C2101 0.1µF
C2003 470pF
B BUS
STROBE BUS
TO MF1 P27
U141 74HCT174
INPA
INPB
J051-14
J051-11
J051-15
J051-24
U131E 74HCT240
U221 74HCT155
U601 74HCT85
R8000 4.7K
R8002 0Ω
R3101 100K
Q4101 MPS2222
/ATT
/RD
/WR
20MHz CLK
INPUT C
U241A 74HCT139
INPUT
FILSLCT
DETECT
J051-12
/INT
/IRST
U181A 74HCT74
/RST
AGND
C4001 330µF
C5000 15µF
C4002 330µF
J401-20
-15V
*EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.
LAST ECO # 89-048
9LVF.2000
SHT 1 of 8
DATE: 1-7-91

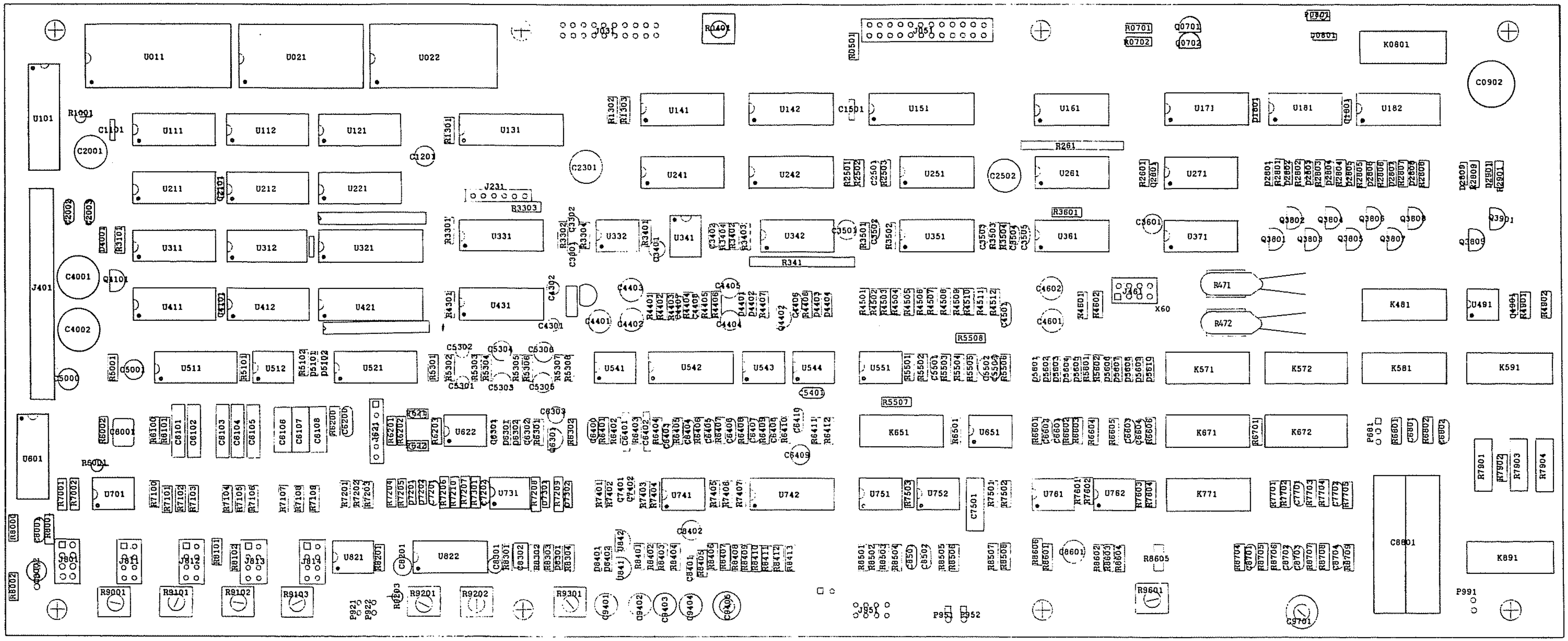


ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)

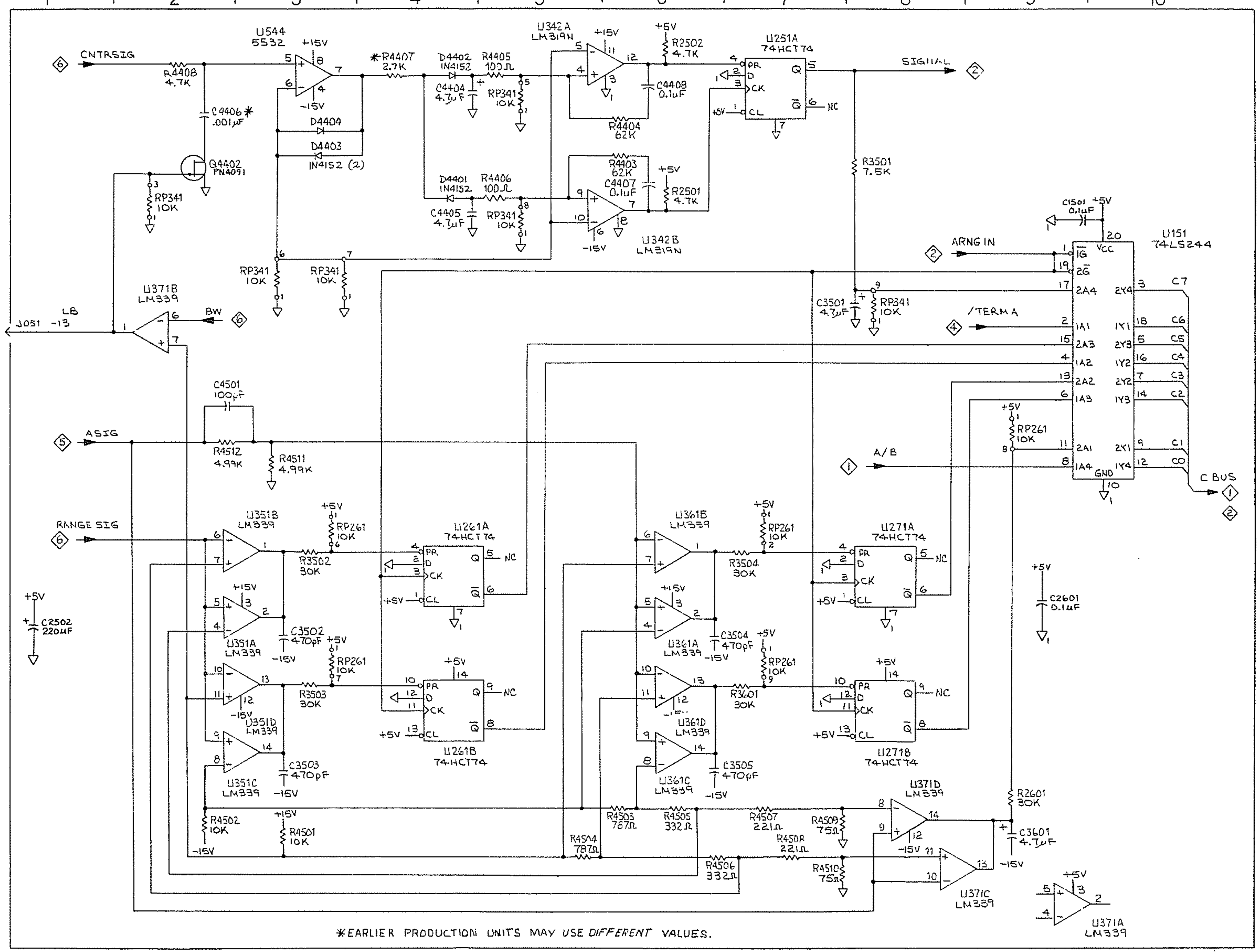


*EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.

9LVF.2000
SHT 2 of 8
DATE: 1-7-91

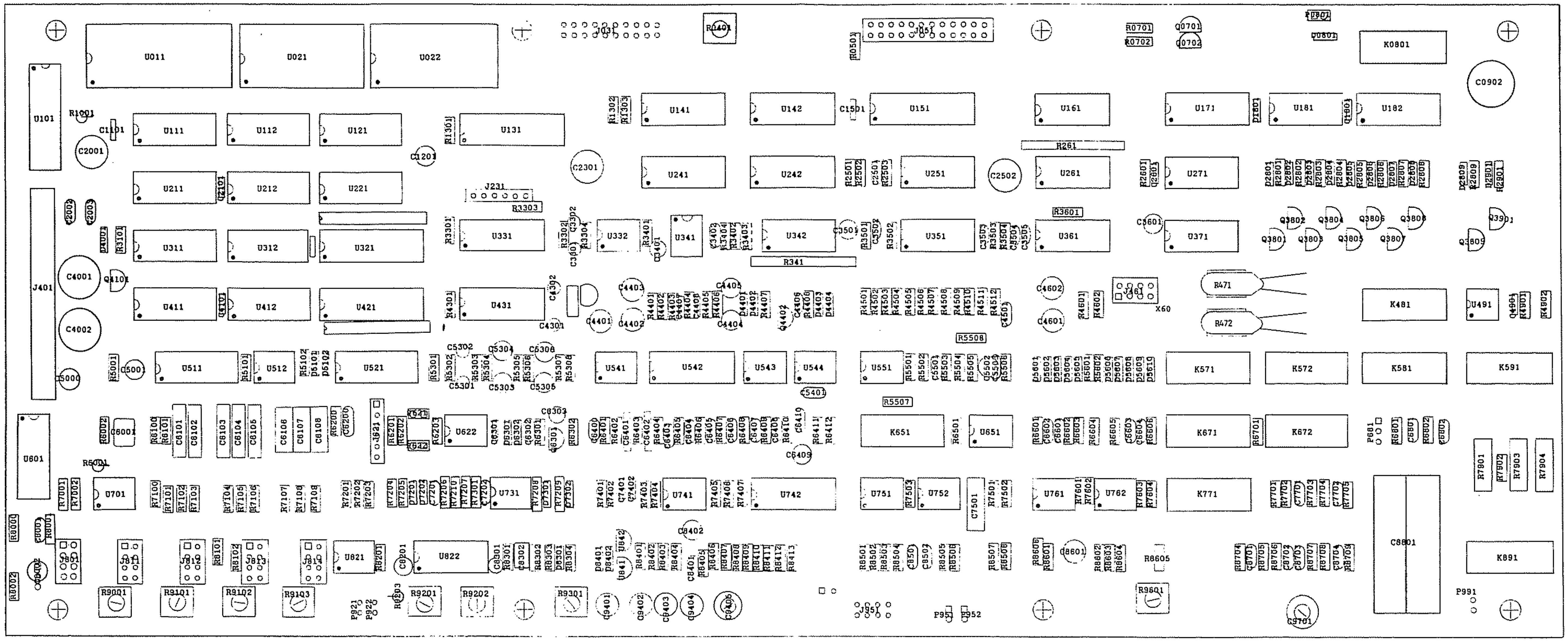


ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)

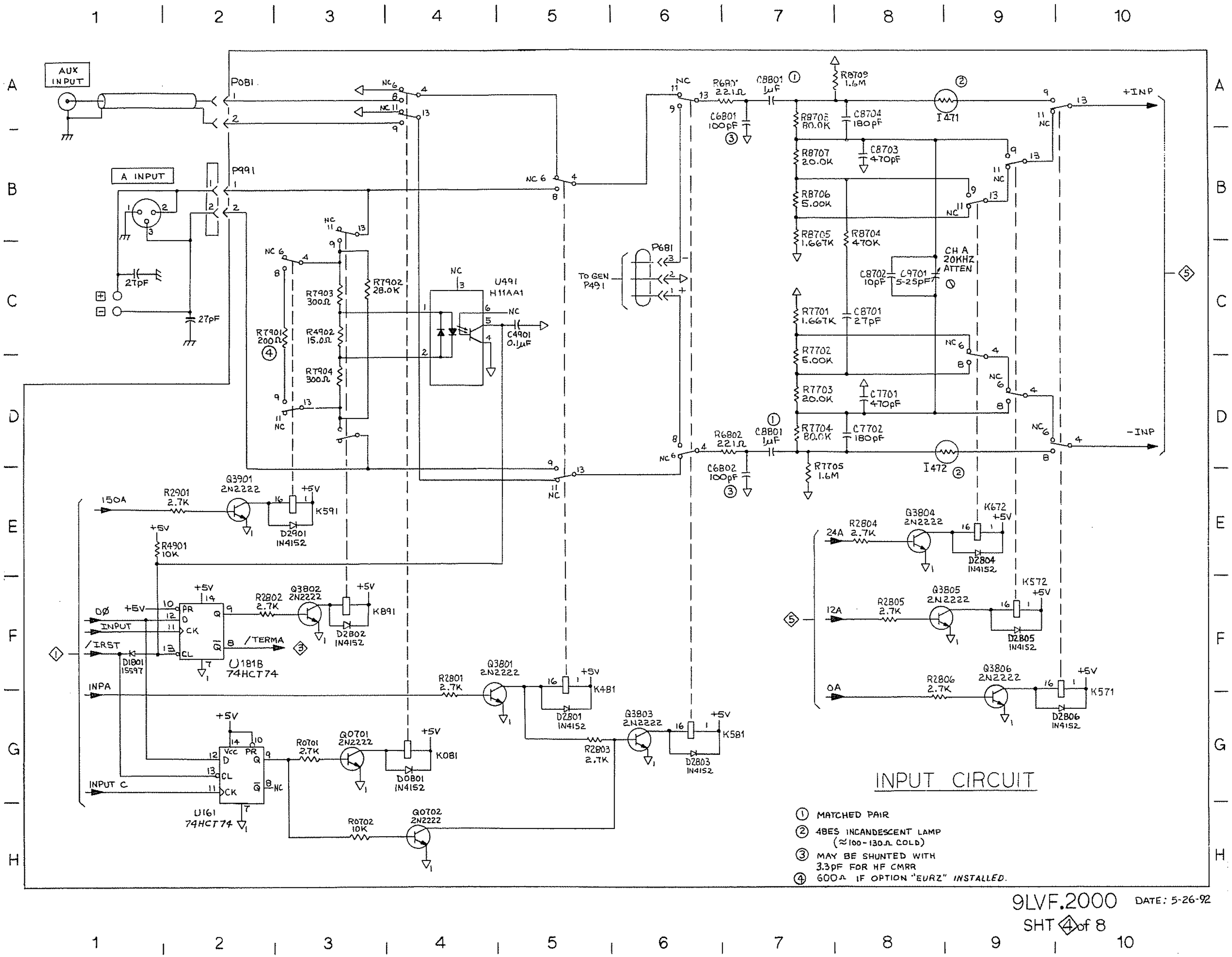


9LVF.2000 DATE: 1-7-91

SHT 3 of 8



ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)

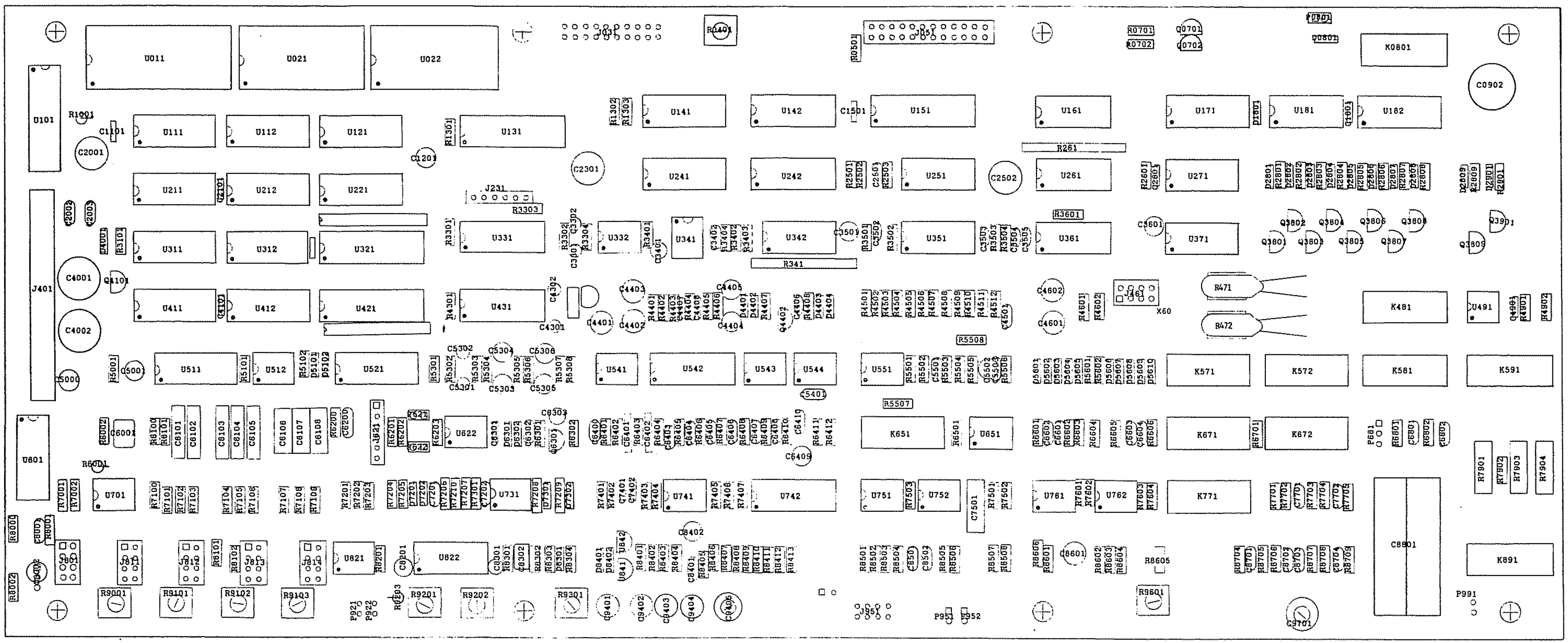


INPUT CIRCUIT

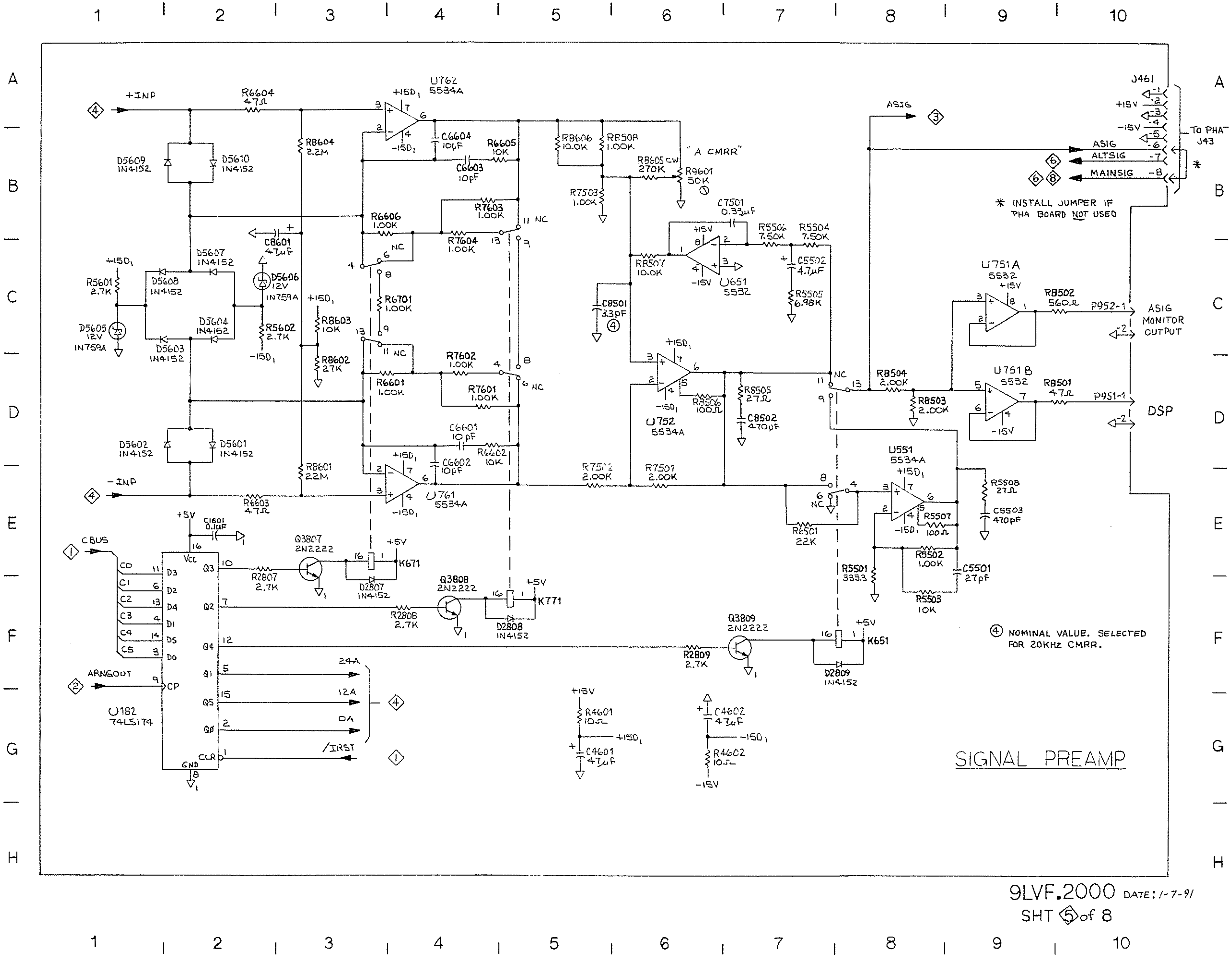
1. MATCHED PAIR
2. 48ES INCANDESCENT LAMP (≈100-130Ω COLD)
3. MAY BE SHUNTED WITH 3.3pF FOR HF CMRR
4. 600Ω IF OPTION "EURZ" INSTALLED.

9LVF.2000 DATE: 5-26-92

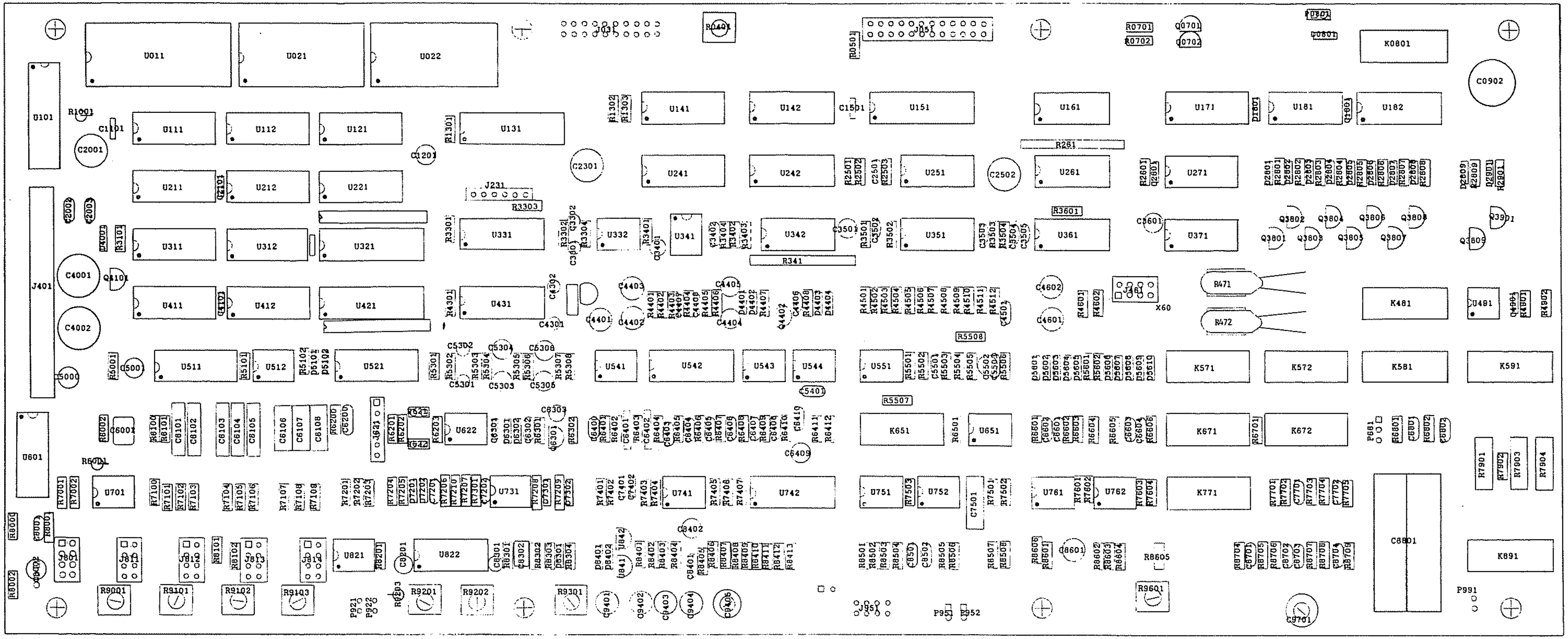
SHT 4 of 8



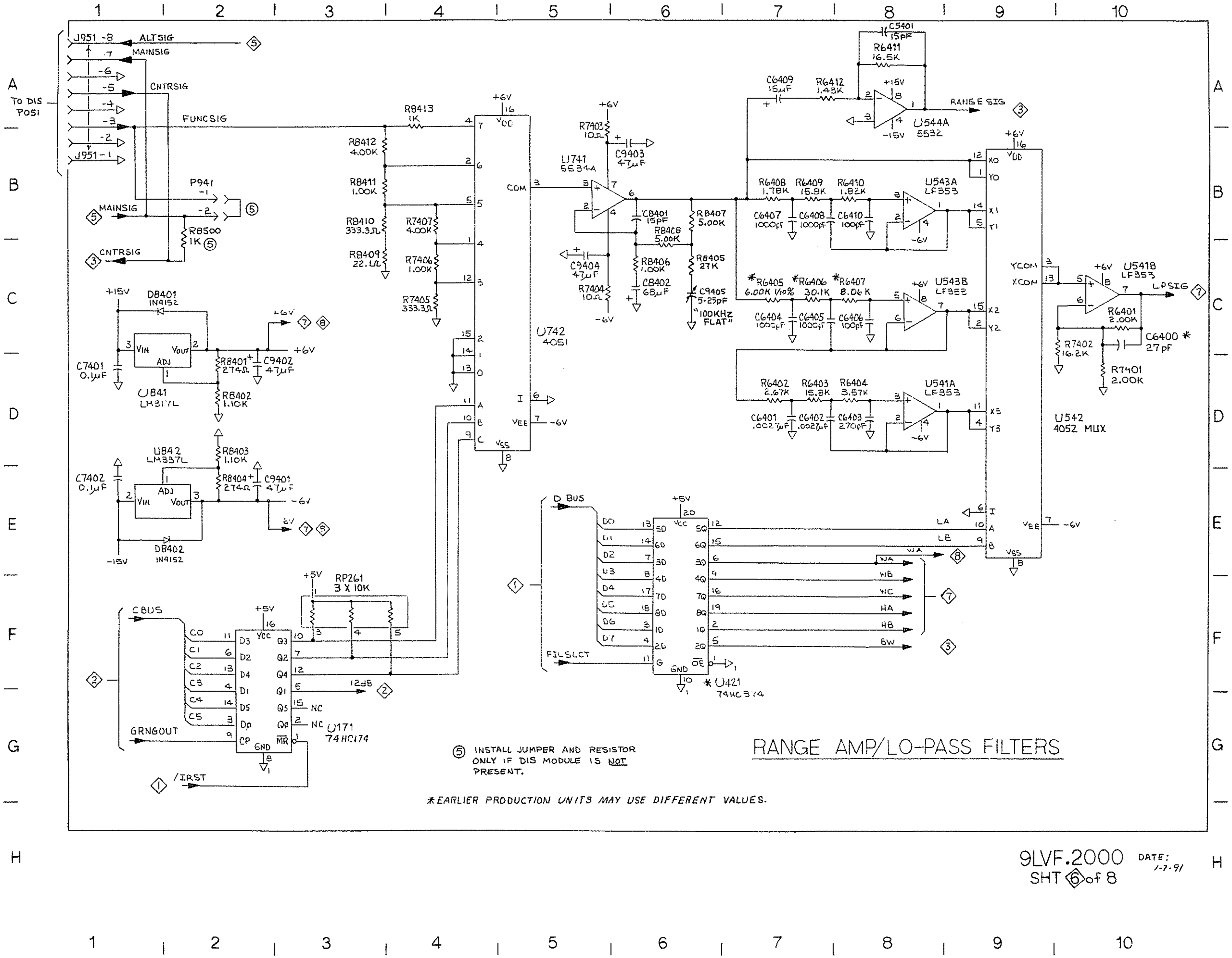
ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)

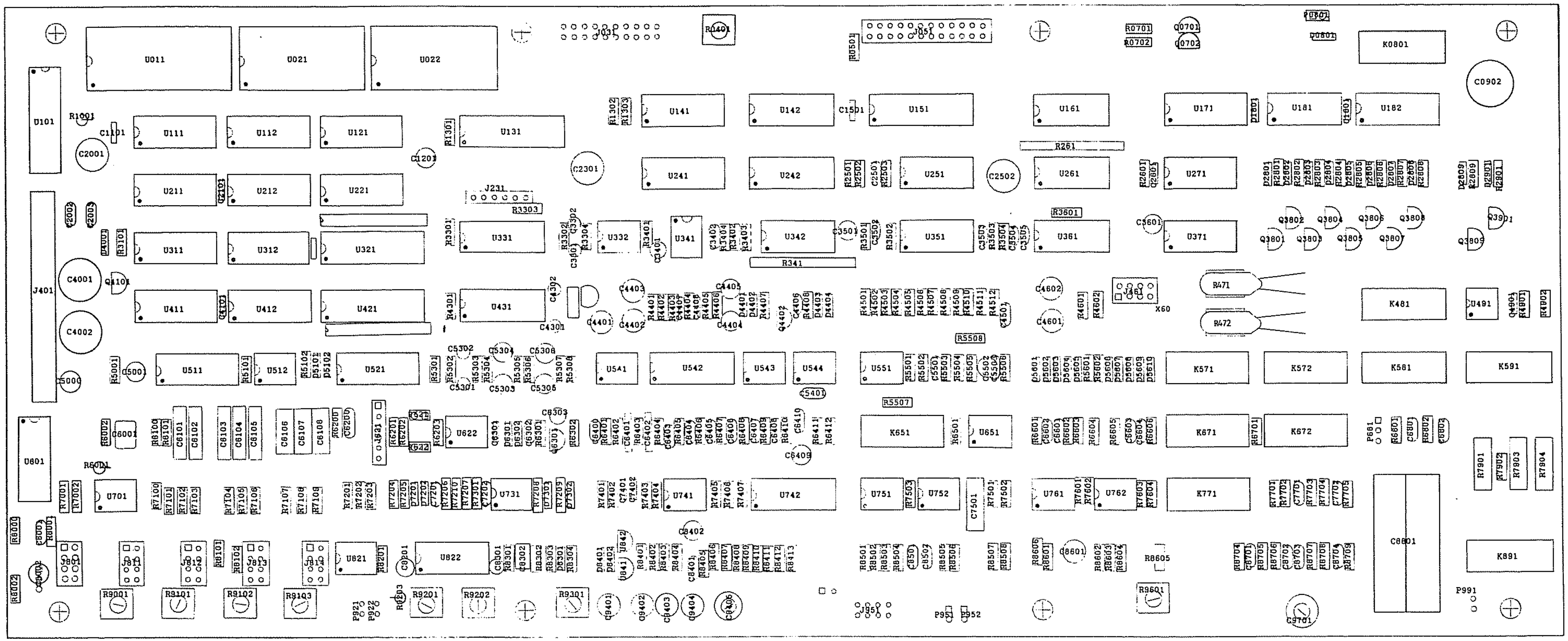


9LVF.2000 DATE: 1-7-91
SHT 5 of 8

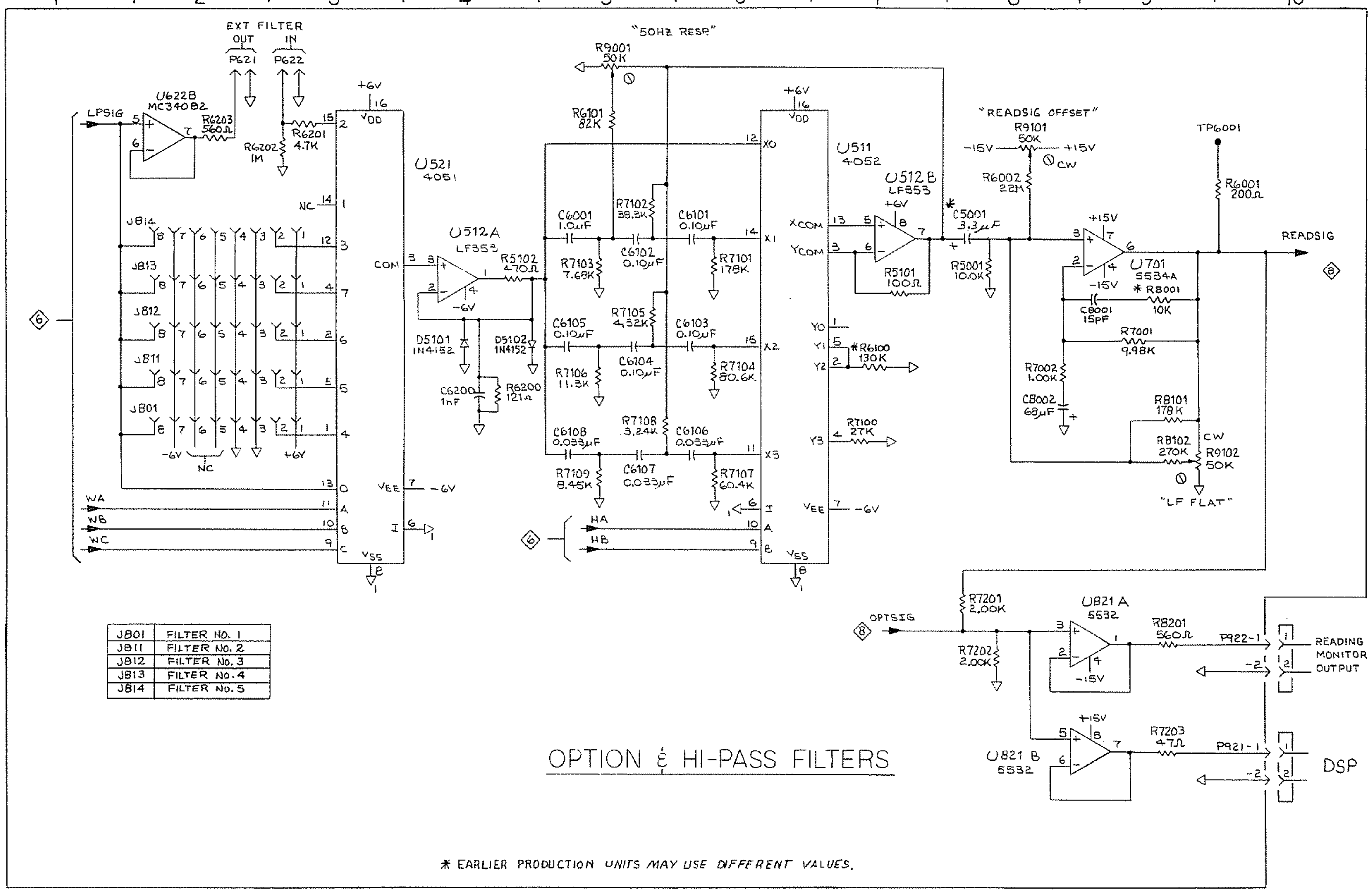


ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)


RANGE AMP/LO-PASS FILTERS
⑤ INSTALL JUMPER AND RESISTOR ONLY IF DIS MODULE IS NOT PRESENT.
*EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.
9LVF.2000
SHT ⑥ of 8
DATE: 1-7-91
To DIS POS1
J951-8 ALTSIG
MAINSIG
CNTRSIG
FUNCSIG
P941
R8500 1K ⑤
U741 5534A
U742 4051
U841 LM317L
U842 LM337L
D8401 1N4152
D8402 1N4152
RP261 3 X 10K
CBUS
GRNGOUT
/IRST
U171 74HC174
12dB
D BUS
FILSLCT
U421 74HC374
U544A 5532
RANGE SIG
U543A LF353
U543B LF353
U541A LF353
U541B LF353
LPSIG
U542 4052 MUX
"100KHZ FLAT"

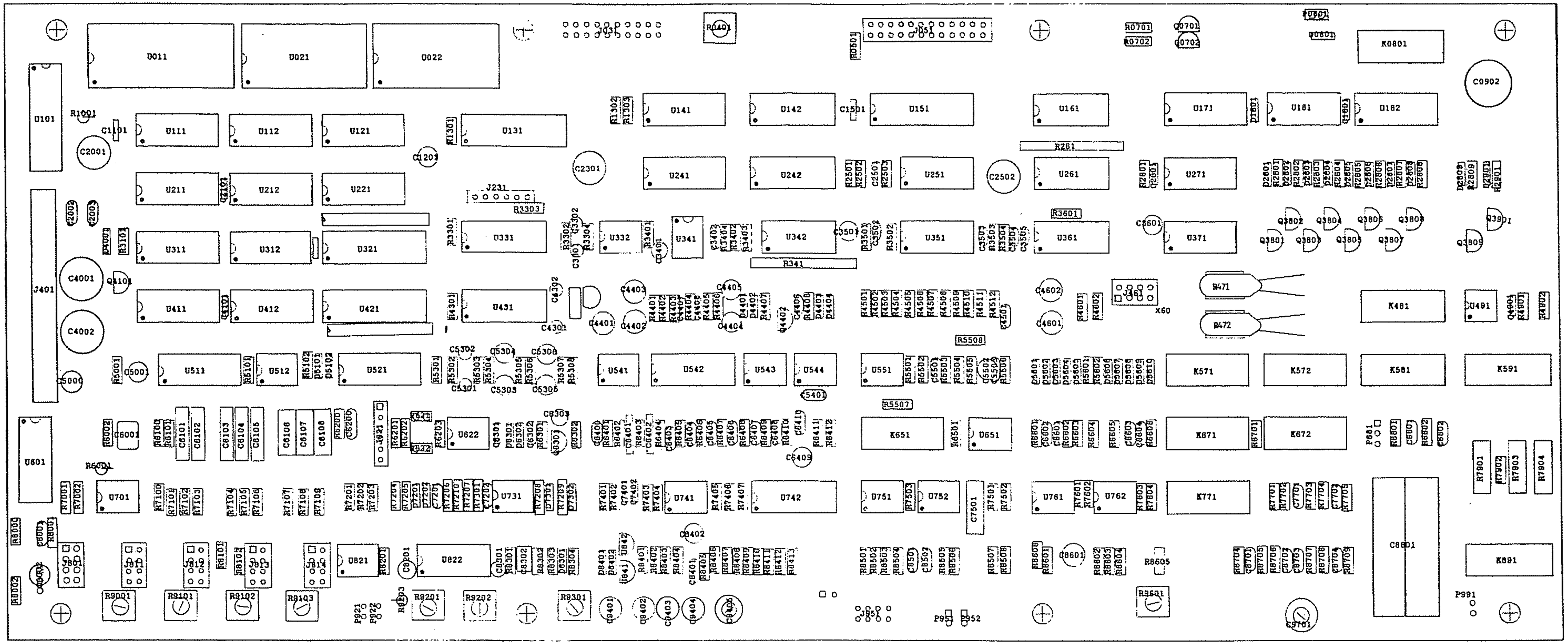


ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)

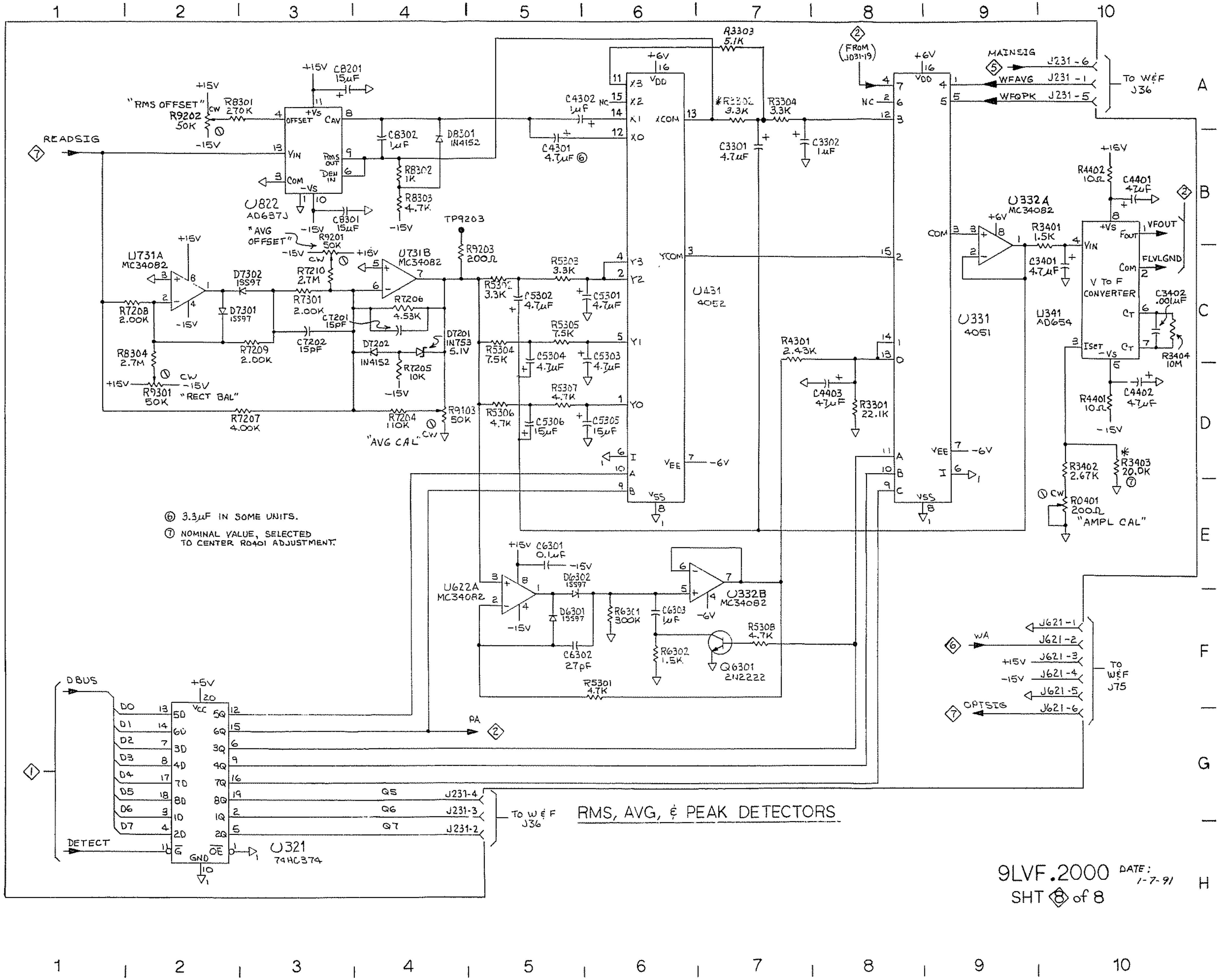


3-31-88 DWM ECO 88-003

9LVF.2000 DATE: 1-7-90
SHT 7 of 8



ANALYZER MAIN MODULE 9LVF.2000 (6200.LVF1.6)



RMS, AVG, & PEAK DETECTORS

9LVF.2000 DATE: 1-7-91

SHT 8 of 8

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C0902	1A10	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1101	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	2G2	2832.0156	CAP TA-EL 25V 20%	15uF
C1501	3C10	2172.0104	CAP CERAM 100V 20%	.1uF
C1801	5E2	2172.0104	CAP CERAM 100V 20%	.1uF
C2001	2G2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2002	1C1	2172.0471	CAP CERAM 100V 20%	470pF
C2003	1D2	2172.0471	CAP CERAM 100V 20%	470pF
C2101	1C1	2172.0104	CAP CERAM 100V 20%	.1uF
C2301	2G4	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2501	2A8	2296.0101	CAP MICA 500V 1%	100pF
C2502	3F1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2601	3E9	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	8B7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3302	8B7	2952.0105	CAP AL-EL 50V 20%	1uF
C3401	8C10	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3402	8C10	2276.0102	CAP MICA 100V 1%	.001uF
C3501	3C8	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3502	3F3	2172.0471	CAP CERAM 100V 20%	470pF
C3503	3G3	2172.0471	CAP CERAM 100V 20%	470pF
C3504	3F6	2172.0471	CAP CERAM 100V 20%	470pF
C3505	3G6	2172.0471	CAP CERAM 100V 20%	470pF
C3601	3G9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4001	1G1	2932.0337	CAP AL-EL 25V 20%	330uF
C4002	1H1	2932.0337	CAP AL-EL 25V 20%	330uF
C4101	1A10	2172.0104	CAP CERAM 100V 20%	.1uF
C4301	8B5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4302	8A5	2952.0105	CAP AL-EL 50V 20%	1uF
C4401	8B10	2932.0476	CAP AL-EL 25V 20%	47uF
C4402	8D10	2932.0476	CAP AL-EL 25V 20%	47uF
C4403	8D8	2932.0476	CAP AL-EL 25V 20%	47uF
C4404	3A4	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4405	3B4	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4406	3A2	2276.0102	CAP MICA 100V 1%	.001uF
C4407	3B6	2172.0104	CAP CERAM 100V 20%	.1uF
C4408	3A6	2172.0104	CAP CERAM 100V 20%	.1uF
C4501	3D2	2296.0101	CAP MICA 500V 1%	100pF
C4601	5G5	2932.0476	CAP AL-EL 25V 20%	47uF
C4602	5G6	2932.0476	CAP AL-EL 25V 20%	47uF
C4901	4C5	2172.0104	CAP CERAM 100V 20%	.1uF
C5000	1H1	2832.0156	CAP TA-EL 25V 20%	15uF
C5001	7B8	2832.0335	CAP TA-EL 25V 20%	3.3uF
C5301	8C6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5302	8C5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5303	8D6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5304	8D5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5305	8D6	2832.0156	CAP TA-EL 25V 20%	15uF
C5306	8D5	2832.0156	CAP TA-EL 25V 20%	15uF
C5401	6A9	2294.0150	CAP MICA 500V 5%	15pF
C5501	5E9	2294.0270	CAP MICA 500V 5%	27pF
C5502	5C7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5503	5E9	2172.0471	CAP CERAM 100V 20%	470pF

REPLACEABLE ELECTRICAL PARTS LIST: 9LVF.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C6001	7B5	2454.0105	CAP POLYE 50V 5%	1uF
C6101	7B5	2675.0104	CAP POLYC 100V 2%	.1uF
C6102	7B5	2675.0104	CAP POLYC 100V 2%	.1uF
C6103	7C6	2675.0104	CAP POLYC 100V 2%	.1uF
C6104	7C5	2675.0104	CAP POLYC 100V 2%	.1uF
C6105	7C5	2675.0104	CAP POLYC 100V 2%	.1uF
C6106	7D6	2555.0333	CAP POLYP 50V 2%	.033uF
C6107	7D5	2454.0333	CAP POLYE 50V 5%	.033uF
C6108	7D5	2555.0333	CAP POLYP 50V 2%	.033uF
C6200	7D4	2276.0102	CAP MICA 100V 1%	.001uF
C6301	8E5	2172.0104	CAP CERAM 100V 20%	.1uF
C6302	8F5	2294.0270	CAP MICA 500V 5%	27pF
C6303	8F6	2952.0105	CAP AL-EL 50V 20%	1uF
C6400	6C10	2294.0270	CAP MICA 500V 5%	27pF
C6401	6D7	2555.0272	CAP POLYP 50V 2%	.0027uF
C6402	6D7	2555.0272	CAP POLYP 50V 2%	.0027uF
C6403	6D8	2296.0271	CAP MICA 500V 1%	270pF
C6404	6C7	2276.0102	CAP MICA 100V 1%	.001uF
C6405	6C7	2276.0102	CAP MICA 100V 1%	.001uF
C6406	6C8	2296.0101	CAP MICA 500V 1%	100pF
C6407	6B7	2276.0102	CAP MICA 100V 1%	.001uF
C6408	6B7	2276.0102	CAP MICA 100V 1%	.001uF
C6409	6A7	2832.0156	CAP TA-EL 25V 20%	15uF
C6410	6B8	2296.0101	CAP MICA 500V 1%	100pF
C6601	5D4	2294.0100	CAP MICA 500V 5%	10pF
C6602	5E4	2294.0100	CAP MICA 500V 5%	10pF
C6603	5B4	2294.0100	CAP MICA 500V 5%	10pF
C6604	5B4	2294.0100	CAP MICA 500V 5%	10pF
C6801	4A7	2296.0101	CAP MICA 500V 1%	100pF
C6802	4E7	2296.0101	CAP MICA 500V 1%	100pF
C7201	8C4	2294.0150	CAP MICA 500V 5%	15pF
C7202	8C3	2294.0150	CAP MICA 500V 5%	15pF
C7401	6D1	2172.0104	CAP CERAM 100V 20%	.1uF
C7402	6E1	2172.0104	CAP CERAM 100V 20%	.1uF
C7501	5B7	2454.0334	CAP POLYE 50V 5%	.33uF
C7701	4D8	2296.0471	CAP MICA 500V 1%	470pF
C7702	4D8	2296.0181	CAP MICA 500V 1%	180pF
C8001	7C9	2294.0150	CAP MICA 500V 5%	15pF
C8002	7C8	2822.0686	CAP TA-EL 16V 20%	68uF
C8201	8A3	2832.0156	CAP TA-EL 25V 20%	15uF
C8301	8B3	2832.0156	CAP TA-EL 25V 20%	15uF
C8302	8B4	2454.0105	CAP POLYE 50V 5%	1uF
C8401	6C6	2294.0150	CAP MICA 500V 5%	15pF
C8402	5C5	2822.0686	CAP TA-EL 16V 20%	68uF
C8501	5V5	2172.0339	CAP CERAM 100V 20%	3.3pF
C8502	5D7	2172.0471	CAP CERAM 100V 20%	470pF
C8601	5B2	2932.0476	CAP AL-EL 25V 20%	47uF
C8701	4C8	2294.0270	CAP MICA 500V 5%	27pF
C8702	4C8	2294.0100	CAP MICA 500V 5%	10pF
C8703	4B8	2296.0471	CAP MICA 500V 1%	470pF
C8704	4A8	2296.0181	CAP MICA 500V 1%	180pF
C8801	4D7,4A7	2694.0105	CAP POLYC 250V 5%	1uF

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C8802	7D8	2694.0105	CAP POLYC 250V 5%	1uF
C9401	6E2	2932.0476	CAP AL-EL 25V 20%	47uF
C9402	6D2	2932.0476	CAP AL-EL 25V 20%	47uF
C9403	6B6	2932.0476	CAP AL-EL 25V 20%	47uF
C9404	6C5	2932.0476	CAP AL-EL 25V 20%	47uF
C9405	6C6	4450.0250	VAR CAP PC	5-25pF
C9701	4C8	4450.0250	VAR CAP PC	5-25pF
D0801	4G4	3110.4152	DIODE SIGNAL	4152
D1801	4F1	3120.0000	DIODE SCHOTTKY	1SS97
D2801	4G5	3110.4152	DIODE SIGNAL	4152
D2802	4F3	3110.4152	DIODE SIGNAL	4152
D2803	4G6	3110.4152	DIODE SIGNAL	4152
D2804	4E9	3110.4152	DIODE SIGNAL	4152
D2805	4F9	3110.4152	DIODE SIGNAL	4152
D2806	4G9	3110.4152	DIODE SIGNAL	4152
D2807	5F3	3110.4152	DIODE SIGNAL	4152
D2808	5F5	3110.4152	DIODE SIGNAL	4152
D2809	5F7	3110.4152	DIODE SIGNAL	4152
D2901	4E3	3110.4152	DIODE SIGNAL	4152
D4001	2H6	3120.0000	DIODE SCHOTTKY	1SS97
D4401	3B4	3110.4152	DIODE SIGNAL	4152
D4402	3A4	3110.4152	DIODE SIGNAL	4152
D4403	3B3	3110.4152	DIODE SIGNAL	4152
D4404	3B3	3110.4152	DIODE SIGNAL	4152
D5101	7C4	3110.4152	DIODE SIGNAL	4152
D5102	7C4	3110.4152	DIODE SIGNAL	4152
D5601	5D2	3110.4152	DIODE SIGNAL	4152
D5602	5D2	3110.4152	DIODE SIGNAL	4152
D5603	5C1	3110.4152	DIODE SIGNAL	4152
D5604	5C2	3110.4152	DIODE SIGNAL	4152
D5605	5C1	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D5606	5C2	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D5607	5C2	3110.4152	DIODE SIGNAL	4152
D5608	5C1	3110.4152	DIODE SIGNAL	4152
D5609	5B2	3110.4152	DIODE SIGNAL	4152
D5610	5B2	3110.4152	DIODE SIGNAL	4152
D6301	8F5	3120.0000	DIODE SCHOTTKY	1SS97
D6302	8F5	3120.0000	DIODE SCHOTTKY	1SS97
D7201	8C4	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
D7202	8C4	3110.4152	DIODE SIGNAL	4152
D7301	8C2	3120.0000	DIODE SCHOTTKY	1SS97
D7302	8C3	3120.0000	DIODE SCHOTTKY	1SS97
D8301	8B4	3110.4152	DIODE SIGNAL	4152
D8401	6C1	3110.4152	DIODE SIGNAL	4152
D8402	6E1	3110.4152	DIODE SIGNAL	4152
I471	4A8	4700.4840	LAMP INCANDESCENT	48V 40mA
I472	4D8	4700.4840	LAMP INCANDESCENT	48V 40mA
J031	2C10,2D10	4221.1020	JACK PC 2 X .1	20 PIN
J051	2A10,2B10,2C10,1A10,1E10	4221.1024	JACK PC 2 X .1	24 PIN

REPLACEABLE ELECTRICAL PARTS LIST: 9LVF.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION		
J231	8G5,8A10	4221.1006	JACK PC .1		6 PIN
J401	1A-H1	4151.1740	CABLE ASSY .05		RBN 17 40 COND
J461	5A10	4221.1008	JACK PC 2 X .1		8 PIN
J621	8F10	4221.1006	JACK PC .1		6 PIN
J801	7D2	4221.1008	JACK PC 2 X .1		8 PIN
J811	7C2	4221.1008	JACK PC 2 X .1		8 PIN
J812	7C2	4221.1008	JACK PC 2 X .1		8 PIN
J813	7C2	4221.1008	JACK PC 2 X .1		8 PIN
J814	7B2	4221.1008	JACK PC 2 X .1		8 PIN
J951	6A1	4221.1008	JACK PC 2 X .1		8 PIN
K081	4G4,4A4	4530.0002	RELAY		DPDT
K481	4B5,4E5,4F5	4530.0002	RELAY		DPDT
K571	4A10,4D10,4F10	4530.0002.1	RELAY PC LOW POWER STABLE		DPDT
K572	4B9,4D9,4F9	4530.0002.1	RELAY PC LOW POWER STABLE		DPDT
K581	4A6,4D6,4G6	4530.0002	RELAY PC LOW POWER		DPDT
K591	4C3,4D3,4E3	4530.0002	RELAY PC LOW POWER		DPDT
K651	5D7,5E7,5F7	4530.0002	RELAY PC LOW POWER		DPDT
K671	5C3,5E3	4530.0002	RELAY PC LOW POWER		DPDT
K672	4B9,4D9,4E9	4530.0002.1	RELAY		DPDT
K771	5B5,5D5,5F5	4530.0002	RELAY PC LOW POWER		DPDT
K891	4B3,4D3,4F3	4530.0002	RELAY PC LOW POWER		DPDT
P081	4A2	4221.0036	PLUG PC	.1 X.43	36 PIN
P621	7A2	4221.0036	PLUG PC	.1 X.43	36 PIN
P622	7A3	4221.0036	PLUG PC	.1 X.43	36 PIN
P681	4C6	4221.0036	PLUG PC	.1 X.43	36 PIN
P921	7F10	4221.0036	PLUG PC	.1 X.43	36 PIN
P922	7E10	4221.0036	PLUG PC	.1 X.43	36 PIN
P951	5D10	4221.0036	PLUG PC	.1 X.43	36 PIN
P952	5C10	4221.0036	PLUG PC	.1 X.43	36 PIN
P991	4B2	4221.0036	PLUG PC	.1 X.43	36 PIN
Q0701	4G3	3211.2222	XSTR NPN TO92		PN2222A
Q0702	4H4	3211.2222	XSTR NPN TO92		PN2222A
Q3801	4G4	3211.2222	XSTR NPN TO92		PN2222A
Q3802	4F3	3211.2222	XSTR NPN TO92		PN2222A
Q3803	4G6	3211.2222	XSTR NPN TO92		PN2222A
Q3804	4E8	3211.2222	XSTR NPN TO92		PN2222A
Q3805	4F8	3211.2222	XSTR NPN TO92		PN2222A
Q3806	4G9	3211.2222	XSTR NPN TO92		PN2222A
Q3807	5E3	3211.2222	XSTR NPN TO92		PN2222A
Q3808	5F4	3211.2222	XSTR NPN TO92		PN2222A
Q3809	5F7	3211.2222	XSTR NPN TO92		PN2222A
Q3901	4E2	3211.2222	XSTR NPN TO92		PN2222A
Q4101	1F2	3211.2222	XSTR NPN TO92		PN2222A
Q4402	3B2	3214.4091	XSTR FET TO92		PN4091
Q6301	8F7	3211.2222	XSTR NPN TO92		PN2222A
R0401	8E10	4412.0201	POT TRIM PC ENC		200
R0501	2B9	1214.0202	RES 1/4W C FLM 5%		2.0K
R0701	4G3	1214.0272	RES 1/4W C FLM 5%		2.7K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R0702	4H3	1214.0103	RES 1/4W C FLM 5%	10K
R1001	2E3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R1301	2D6	1214.0103	RES 1/4W C FLM 5%	10K
R1302	2B9	1214.0202	RES 1/4W C FLM 5%	2.0K
R1303	2B9	1214.0202	RES 1/4W C FLM 5%	2.0K
R2501	3B6	1214.0472	RES 1/4W C FLM 5%	4.7K
R2502	3A6	1214.0472	RES 1/4W C FLM 5%	4.7K
R2503	2A9	1214.0102	RES 1/4W C FLM 5%	1K
R2601	3G9	1214.0303	RES 1/4W C FLM 5%	30K
R261	3F7,3E7,3F3,3E3,3D9	1984.9103	RES NET SIP 5% B	9 X 10K
R2801	4G4	1214.0272	RES 1/4W C FLM 5%	2.7K
R2802	4F2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2803	4G5	1214.0272	RES 1/4W C FLM 5%	2.7K
R2804	4E8	1214.0272	RES 1/4W C FLM 5%	2.7K
R2805	4F8	1214.0272	RES 1/4W C FLM 5%	2.7K
R2806	4G8	1214.0272	RES 1/4W C FLM 5%	2.7K
R2807	5E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2808	5F4	1214.0272	RES 1/4W C FLM 5%	2.7K
R2809	5F6	1214.0272	RES 1/4W C FLM 5%	2.7K
R2901	4E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R3101	1F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R3301	8D8	1136.2212	RES 1/8W M FLM 1%	22.1K
R3302	8A7	1214.0223	RES 1/4W C FLM 5%	22K
R3303	8A7	1214.0512	RES 1/4W C FLM 5%	5.1K
R3304	8A7	1214.0332	RES 1/4W C FLM 5%	3.3K
R3401	8C10	1214.0152	RES 1/4W C FLM 5%	1.5K
R3402	8D10	1136.2671	RES 1/8W M FLM 1%	2.67K
R3403	8D10	1136.2002	RES 1/8W M FLM 1%	20.0K
R3404	8C10	1214.0106	RES 1/4W C FLM 5%	10M
R341	3C8,3B2,3C3,3B5,3A5	1984.9103	RES NET SIP 5% B	9 X 10K
R3501	3B8	1214.0752	RES 1/4W C FLM 5%	7.5K
R3502	3E3	1214.0303	RES 1/4W C FLM 5%	30K
R3503	3F3	1214.0303	RES 1/4W C FLM 5%	30K
R3504	3E7	1214.0303	RES 1/4W C FLM 5%	30K
R3601	3F7	1214.0303	RES 1/4W C FLM 5%	30K
R4301	8C7	1136.2431	RES 1/8W M FLM 1%	2.43K
R4401	8D10	1214.0100	RES 1/4W C FLM 5%	10
R4402	8B10	1214.0100	RES 1/4W C FLM 5%	10
R4403	3B6	1214.0623	RES 1/4W C FLM 5%	62K
R4404	3A6	1214.0623	RES 1/4W C FLM 5%	62K
R4405	3A5	1214.0101	RES 1/4W C FLM 5%	100
R4406	3B5	1214.0101	RES 1/4W C FLM 5%	100
R4407	3A4	1214.0272	RES 1/4W C FLM 5%	2.7K
R4408	3A2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4501	3G3	1136.1002	RES 1/8W M FLM 1%	10.0K
R4502	3G2	1136.1002	RES 1/8W M FLM 1%	10.0K
R4503	3G5	1136.7870	RES 1/8W M FLM 1%	787
R4504	3G5	1136.7870	RES 1/8W M FLM 1%	787
R4505	3G6	1136.3320	RES 1/8W M FLM 1%	332
R4506	3G6	1136.3320	RES 1/8W M FLM 1%	332
R4507	3G7	1136.2210	RES 1/8W M FLM 1%	221
R4508	3G7	1136.2210	RES 1/8W M FLM 1%	221

REPLACEABLE ELECTRICAL PARTS LIST: 9LVF.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4509	3G7	1214.0750	RES 1/4W C FLM 5%	75
R4510	3H7	1214.0750	RES 1/4W C FLM 5%	75
R4511	3D3	1136.4991	RES 1/8W M FLM 1%	4.99K
R4512	3D2	1136.4991	RES 1/8W M FLM 1%	4.99K
R4601	5G5	1214.0100	RES 1/4W C FLM 5%	10
R4602	5G6	1214.0100	RES 1/4W C FLM 5%	10
R4901	4E1	1214.0103	RES 1/4W C FLM 5%	10K
R4902	4C3	1136.1509	RES 1/8W M FLM 1%	15.0
R5001	7B8	1136.1002	RES 1/8W M FLM 1%	10.0K
R5101	7C7	1214.0101	RES 1/4W C FLM 5%	100
R5102	7C4	1214.0471	RES 1/4W C FLM 5%	470
R5301	8F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R5302	8C5	1214.0332	RES 1/4W C FLM 5%	3.3K
R5303	8C5	1214.0332	RES 1/4W C FLM 5%	3.3K
R5304	8C5	1214.0752	RES 1/4W C FLM 5%	7.5K
R5305	8C5	1214.0752	RES 1/4W C FLM 5%	7.5K
R5306	8D5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5307	8D5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5308	8F7	1214.0472	RES 1/4W C FLM 5%	4.7K
R5501	5F8	1139.3330	RES 1/8W M FLM .1%	333.3
R5502	5E8	1139.1001	RES 1/8W M FLM .1%	1.00K
R5503	5F8	1214.0103	RES 1/4W C FLM 5%	10K
R5504	5C7	1136.7501	RES 1/8W M FLM 1%	7.50K
R5505	5C7	1136.6981	RES 1/8W M FLM 1%	6.98K
R5506	5C7	1136.7501	RES 1/8W M FLM 1%	7.50K
R5507	5E8	1214.0101	RES 1/4W C FLM 5%	100
R5508	5E8	1214.0270	RES 1/4W C FLM 5%	27
R5601	5C1	1214.0272	RES 1/4W C FLM 5%	2.7K
R5602	5C2	1214.0272	RES 1/4W C FLM 5%	2.7K
R6001	7B10	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R6002	7B8	1214.0226	RES 1/4W C FLM 5%	22M
R6100	7C7	1214.0134	RES 1/4W C FLM 5%	130K
R6101	7A5	1214.0823	RES 1/4W C FLM 5%	82K
R6200	7D4	1136.1210	RES 1/8W M FLM 1%	121
R6201	7A3	1214.0472	RES 1/4W C FLM 5%	4.7K
R6202	7B3	1214.0105	RES 1/4W C FLM 5%	1M
R6203	7A2	1214.0561	RES 1/4W C FLM 5%	560
R6301	8F6	1214.0304	RES 1/4W C FLM 5%	300K
R6302	8F6	1214.0152	RES 1/4W C FLM 5%	1.5K
R6401	6C10	1139.2001	RES 1/8W M FLM .1%	2.00K
R6402	6D7	1136.2671	RES 1/8W M FLM 1%	2.67K
R6403	6D7	1136.1582	RES 1/8W M FLM 1%	15.8K
R6404	6D8	1136.3571	RES 1/8W M FLM 1%	3.57K
R6405	6C7	1139.6001	RES 1/8W M FLM .1%	6.00K
R6406	6C7	1136.3012	RES 1/8W M FLM 1%	30.1K
R6407	6C8	1136.8061	RES 1/8W M FLM 1%	8.06K
R6408	6B7	1136.1781	RES 1/8W M FLM 1%	1.78K
R6409	6B7	1136.1582	RES 1/8W M FLM 1%	15.8K
R6410	6B8	1136.1821	RES 1/8W M FLM 1%	1.82K
R6411	6A8	1136.1652	RES 1/8W M FLM 1%	16.5K
R6412	6A7	1136.1431	RES 1/8W M FLM 1%	1.43K
R6501	5E7	1214.0223	RES 1/4W C FLM 5%	22K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R6601	5D3	1139.1001	RES 1/8W M FLM .1%	1.00K
R6602	5D4	1214.0103	RES 1/4W C FLM 5%	10K
R6603	5E2	1214.0470	RES 1/4W C FLM 5%	47
R6604	5A2	1214.0470	RES 1/4W C FLM 5%	47
R6605	5B4	1214.0103	RES 1/4W C FLM 5%	10K
R6606	5B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R6701	5C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R6801	4A7	1136.2210	RES 1/8W M FLM 1%	221
R6802	4E7	1136.2210	RES 1/8W M FLM 1%	221
R7001	7C9	1139.9981	RES 1/8W M FLM .1%	9.98K
R7002	7C8	1139.1001	RES 1/8W M FLM .1%	1.00K
R7100	7D7	1214.0273	RES 1/4W C FLM 5%	27K
R7101	7B6	1136.1783	RES 1/8W M FLM 1%	178K
R7102	7B5	1136.3832	RES 1/8W M FLM 1%	38.3K
R7103	7B5	1136.7681	RES 1/8W M FLM 1%	7.68K
R7104	7C6	1136.8062	RES 1/8W M FLM 1%	80.6K
R7105	7C5	1136.4321	RES 1/8W M FLM 1%	4.32K
R7106	7C5	1136.1132	RES 1/8W M FLM 1%	11.3K
R7107	7D6	1136.6042	RES 1/8W M FLM 1%	60.4K
R7108	7D5	1136.3241	RES 1/8W M FLM 1%	3.24K
R7109	7D5	1136.8451	RES 1/8W M FLM 1%	8.45K
R7201	7E8	1139.2001	RES 1/8W M FLM .1%	2.00K
R7202	7E8	1139.2001	RES 1/8W M FLM .1%	2.00K
R7203	7F9	1214.0470	RES 1/4W C FLM 5%	47
R7204	8D4	1214.0114	RES 1/4W C FLM 5%	110K
R7205	8C4	1214.0103	RES 1/4W C FLM 5%	10K
R7206	8C4	1136.4531	RES 1/8W M FLM 1%	4.53K
R7207	8D3	1139.4001	RES 1/8W M FLM .1%	4.00K
R7208	8C2	1139.2001	RES 1/8W M FLM .1%	2.00K
R7209	8C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R7210	8C3	1214.0275	RES 1/4W C FLM 5%	2.7M
R7301	8C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R7401	6C10	1139.2001	RES 1/8W M FLM .1%	2.00K
R7402	6C9	1136.1622	RES 1/8W M FLM 1%	16.2K
R7403	6B5	1214.0100	RES 1/4W C FLM 5%	10
R7404	6C5	1214.0100	RES 1/4W C FLM 5%	10
R7405	6C4	1139.3330	RES 1/8W M FLM .1%	333.3
R7406	6C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7407	6B4	1139.4001	RES 1/8W M FLM .1%	4.00K
R7501	5E6	1139.2001	RES 1/8W M FLM .1%	2.00K
R7502	5E5	1139.2001	RES 1/8W M FLM .1%	2.00K
R7503	5B5	1139.1001	RES 1/8W M FLM .1%	1.00K
R7601	5D4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7602	5D4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7603	5B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7604	5B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7701	4C7	1139.1671	RES 1/8W M FLM .1%	1.667K
R7702	4C7	1139.5001	RES 1/8W M FLM .1%	5.00K
R7703	4D7	1139.2002	RES 1/8W M FLM .1%	20.0K
R7704	4D7	1139.8002	RES 1/8W M FLM .1%	80.0K
R7705	4E7	1214.0165	RES 1/4W C FLM 5%	1.6M
R7901	4C3	1656.2000	RES 3W W WND 1%	200

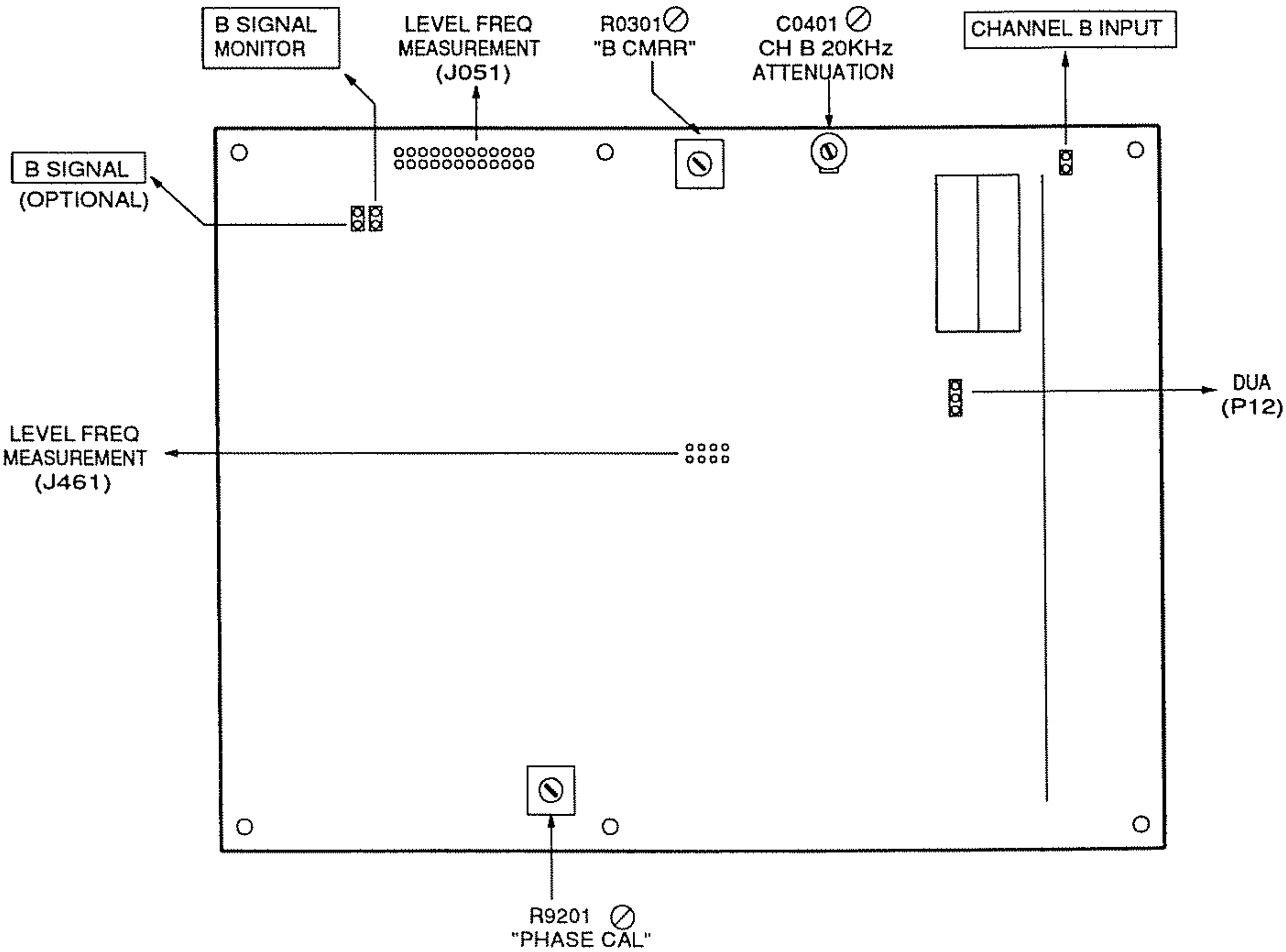
REPLACEABLE ELECTRICAL PARTS LIST: 9LVF.2000

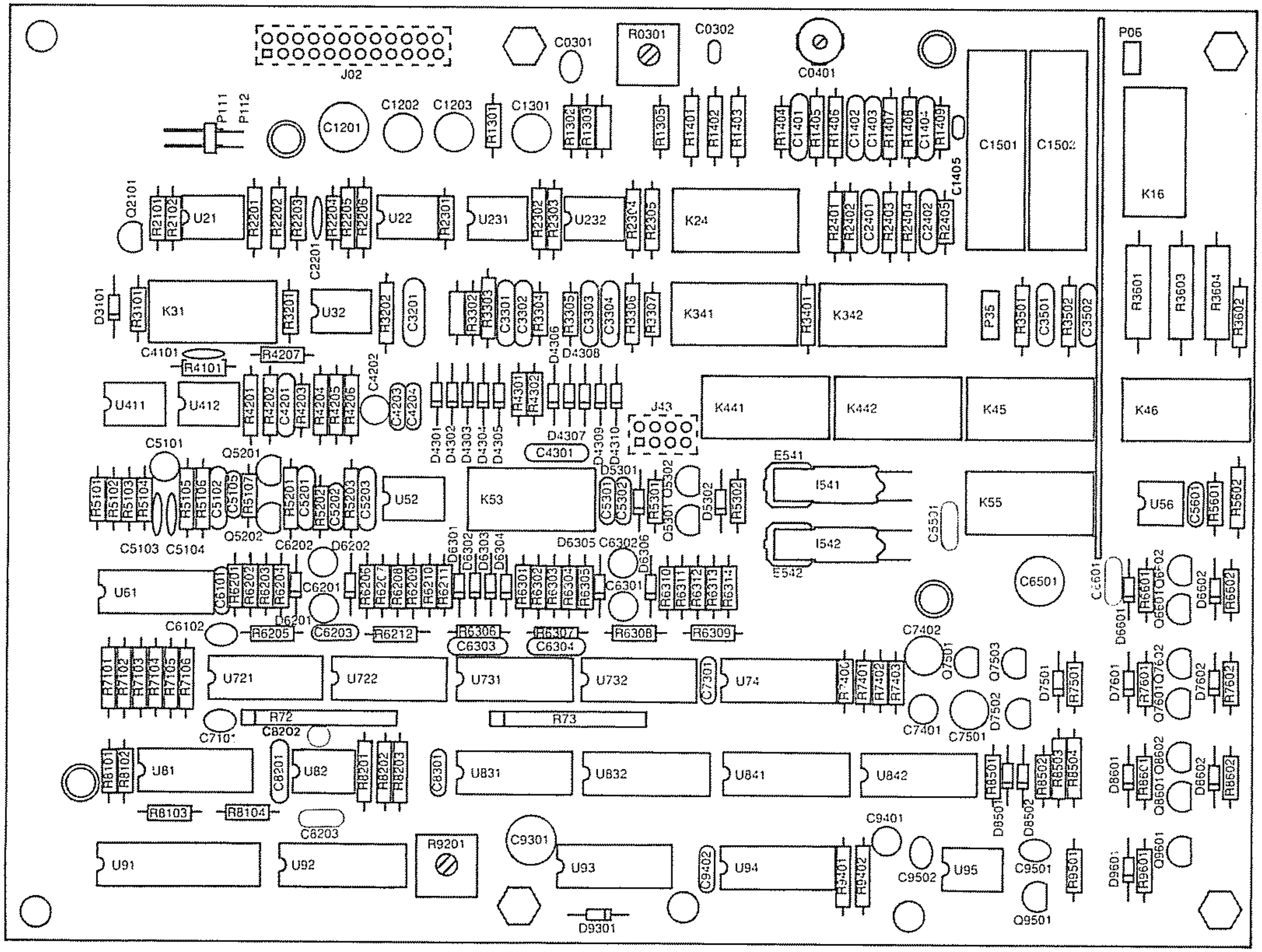
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R7902	4C3	1136.2802	RES 1/8W M FLM 1%	28.0K
R7903	4C3	1656.3000	RES 3W W WND 1%	300
R7904	4D3	1656.3000	RES 3W W WND 1%	300
R79E1	4C3	1656.6000	RES 3W W WND 1%	600
R8000	1F3	1214.0472	RES 1/4W C FLM 5%	4.7K
R8001	7C9	1214.0103	RES 1/4W C FLM 5%	10K
R8002	1F3	1214.0000	JUMPER .4 X.25	00
R8101	7D9	1136.1783	RES 1/8W M FLM 1%	178K
R8102	7D9	1214.0274	RES 1/4W C FLM 5%	270K
R8201	7E9	1214.0561	RES 1/4W C FLM 5%	560
R8301	8A2	1214.0274	RES 1/4W C FLM 5%	270K
R8302	8B4	1214.0102	RES 1/4W C FLM 5%	1K
R8303	8B4	1214.0472	RES 1/4W C FLM 5%	4.7K
R8304	8C2	1214.0275	RES 1/4W C FLM 5%	2.7M
R8401	6D2	1136.2740	RES 1/8W M FLM 1%	274
R8402	6D2	1136.1101	RES 1/8W M FLM 1%	1.10K
R8403	6D2	1136.1101	RES 1/8W M FLM 1%	1.10K
R8404	6E2	1136.2740	RES 1/8W M FLM 1%	274
R8405	6C6	1214.0273	RES 1/4W C FLM 5%	27K
R8406	6C6	1139.1001	RES 1/8W M FLM .1%	1.00K
R8407	6B6	1139.5001	RES 1/8W M FLM .1%	5.00K
R8408	6C6	1139.5001	RES 1/8W M FLM .1%	5.00K
R8409	6C3	1136.2219	RES 1/8W M FLM 1%	22.1
R8410	6B3	1139.3330	RES 1/8W M FLM .1%	333.3
R8411	6B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R8412	6B3	1139.4001	RES 1/8W M FLM .1%	4.00K
R8413	6B4	1214.0102	RES 1/4W C FLM 5%	1K
R8501	5D9	1214.0470	RES 1/4W C FLM 5%	47
R8502	5C9	1214.0561	RES 1/4W C FLM 5%	560
R8503	5D8	1139.2001	RES 1/8W M FLM .1%	2.00K
R8504	5D8	1139.2001	RES 1/8W M FLM .1%	2.00K
R8505	5D7	1214.0270	RES 1/4W C FLM 5%	
27				
R8506	5D7	1214.0101	RES 1/4W C FLM 5%	100
R8507	5C6	1136.1002	RES 1/8W M FLM 1%	10.0K
R8508	5B5	1139.1001	RES 1/8W M FLM .1%	1.00K
R8601	5E3	1214.0226	RES 1/4W C FLM 5%	22M
R8602	5D3	1214.0273	RES 1/4W C FLM 5%	27K
R8603	5C3	1214.0103	RES 1/4W C FLM 5%	10K
R8604	5B3	1214.0226	RES 1/4W C FLM 5%	22M
R8605	5B6	1214.0274	RES 1/4W C FLM 5%	270K
R8606	5B5	1136.1002	RES 1/8W M FLM 1%	10.0K
R8704	4B7	1214.0474	RES 1/4W C FLM 5%	470K
R8705	4B7	1139.1671	RES 1/8W M FLM .1%	1.667K
R8706	4B7	1139.5001	RES 1/8W M FLM .1%	5.00K
R8707	4B7	1139.2002	RES 1/8W M FLM .1%	20.0K
R8708	4A7	1139.8002	RES 1/8W M FLM .1%	80.0K
R8709	4A7	1214.0165	RES 1/4W C FLM 5%	1.6M
R9001	7A5	4412.0503	POT TRIM PC ENC	50K
R9101	7B8	4412.0503	POT TRIM PC ENC	50K
R9102	7D9	4412.0503	POT TRIM PC ENC	50K
R9103	8D4	4412.0503	POT TRIM PC ENC	50K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R9201	8C3	4412.0503	POT TRIM PC ENC	50K
R9202	8A2	4412.0503	POT TRIM PC ENC	50K
R9203	8C4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R9301	8D2	4412.0503	POT TRIM PC ENC	50K
R9601	5B6	4412.0503	POT TRIM PC ENC	50K
U011	2D3	3331.6805	uPROCESSOR EPROM	68705P3
U021	2B5	3332.8254	TIMER INTERVAL PROG	82C54
U022	2B9	3332.8254	TIMER INTERVAL PROG	82C54
U101	1B2	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U111	1B3	3313.0670	REGISTER FILE 4X4	74LS670
U112	1B9	3313.0670	REGISTER FILE 4X4	74LS670
U121	2C6,2C2,2B3,2B2	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U131	2D7,2C7,2B6,1E4,2A8	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U141	1E9	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U142	2F9	3313.0138	DECODER 3-LINE/8-LINE	74LS138
U151	3C10	3313.0244	BUFFER 8X TRI-STATE	74LS244
U161	4G2	3313.0074	FLIP-FLOP 2X D	74LS74
U171	6F2	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U181	3F2,1G9	3313.0074	FLIP-FLOP 2X D	74LS74
U182	5F2	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U211	1B5	3313.0670	REGISTER FILE 4X4	74LS670
U212	1C3	3313.0670	REGISTER FILE 4X4	74LS670
U221	1E6	3313.0155	DECODER 2 X 2-LN/4-LN	74LS155
U241	2G6,1G8	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
U242	2E5	3313.0138	DECODER 3-LINE/8-LINE	74LS138
U251	3A7,2B7	3324.0074	FLIP-FLOP 2X D	74HCT74
U261	6F3,3E4,3F4	3324.0074	FLIP-FLOP 2X D	74HCT74
U271	3F8,3E8	3324.0074	FLIP-FLOP 2X D	74HCT74
U311	1B7	3313.0670	REGISTER FILE 4X4	74LS670
U312	1C5	3313.0670	REGISTER FILE 4X4	74LS670
U321	8G2	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U331	8C9	3321.4051	MULTIPLEX 8X	4051
U332	8E7	3412.0082	OP AMP DUAL	MC34082
U341	8C10	3441.0654	CONVERTER VOLT TO FREQ	AD654J
U342	3B5,3A5	3422.0319	COMPARATOR DUAL HI-SPEED	LM319
U351	3G3,3F3,3E3	3424.0339	COMPARATOR QUAD	LM339
U361	3E6,3F6,3G6	3424.0339	COMPARATOR QUAD	LM339
U371	3H8,3G8,3C2	3424.0339	COMPARATOR QUAD	LM339
U411	1C9	3313.0670	REGISTER FILE 4X4	74LS670
U412	1C7	3313.0670	REGISTER FILE 4X4	74LS670
U421	6F6	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U431	8B6	3321.4052	MULTIPLEX 4X DIFF	4052
U491	4C4	3630.0001	OPTO-ISOLATOR	H11AA1
U511	7B6	3321.4052	MULTIPLEX 4X DIFF	4052
U512	7B7,7C4	3412.0353	OP AMP DUAL	TL072/LF353
U521	7B4	3321.4051	MULTIPLEX 8X	4051
U541	6D8,6C10	3412.0353	OP AMP DUAL	TL072/LF353
U542	6C9	3321.4052	MULTIPLEX 4X DIFF	4052
U543	6C8	3412.0353	OP AMP DUAL	TL072/LF353
U544	6A8	3412.5532	OP AMP DUAL	5532
U551	5E8	3411.5534	OP AMP SINGLE	5534A

REPLACEABLE ELECTRICAL PARTS LIST: 9LVF.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U601	1E2	3313.0085	COMPARATOR 4-BIT MAG	74LS85
U622	8F5,7A2	3412.0082	OP AMP DUAL	MC34082
U651	5C6	3412.5532	OP AMP DUAL	5532
U701	7B9	3411.5534	OP AMP SINGLE	5534A
U731	8C4,8C2	3412.0082	OP AMP DUAL	MC34082
U741	6B5	3411.5534	OP AMP SINGLE	5534A
U742	6B4	3321.4051	MULTIPLEX 8X	4051
U751	5C9,5D9	3412.5532	OP AMP DUAL	5532
U752	5D6	3411.5534	OP AMP SINGLE	5534A
U761	5E4	3411.5534	OP AMP SINGLE	5534A
U762	5A4	3411.5534	OP AMP SINGLE	5534A
U821	7F8,7E9	3412.5532	OP AMP DUAL	5532
U822	8A3	3441.0637	CONVERTER RMS TO DC	AD637J
U841	6D1	3430.1317	VOLT REG POS VAR TO92	LM317L
U842	6E1	3431.1337	VOLT REG NEG VAR TO92	LM337L


B SIGNAL MONITOR
LEVEL FREQ MEASUREMENT (J051)
R0301 "B CMRR"
C0401 CH B 20KHz ATTENUATION
CHANNEL B INPUT
B SIGNAL (OPTIONAL)
DUA (P12)
LEVEL FREQ MEASUREMENT (J461)
R9201 "PHASE CAL"



DUAL INPUT ANALYZER & PHASE OPTION 9PHA.2000 (6200.PHA1.7)

PHA-2, DUAL INPUT / PHASEMETER

The PHA-2 circuit board mounts to the LVF-2 module and adds a second autoranging input channel and phasemeter to the System One analyzer. The functional circuits on the board include the input attenuators, input preamplifier, range comparators, and phasemeter.

Input Circuit <1>

The input signal is derived from the front panel connectors or the internal generator monitor interconnection via relays K45 and K55. Relays K45 and K55 are ganged together to provide optimum input isolation when monitoring the generator output. P35 connects to a shielded cable originating on the B output of the generator.

Relay K16 selects the 600 Ohm and 150 Ohm terminations. Its control bit originates from the Q output of flip-flop U93A. When a termination is selected the flip-flop Q output clocks high and causes relay K16 to be energized through Q6601. Relay K46 provides 600/150 Ohm selection. In the 600 Ohm selection, relay K46 is open and the termination is composed of resistors R3602-R3604 and R5602. R3601 shunts the 600 Ohm termination to obtain the 150 Ohm termination (300 Ohms if option **EURZ** is installed). The terminations are protected against excessive power dissipation by sensing a small portion of the total input voltage through the divider action of R3603, R3604, and R5602 and the ac optocoupler U56. An input level greater than approximately +32 dBu (30 Vrms) will forward bias the light-emitting diodes inside U56. This causes the phototransistor inside U56 to conduct, clearing the control flip-flop U93A and de-energizing relay K16.

The selected input signal passes through RF suppression filters composed of R3501, C3501, R3502, and C3502. In some units C3501 or C3502 may be shunted with a small capacitor to balance the total input capacitance. The signal is then ac-coupled to the input attenuators through C1501 and C1502. C1501 and C1502 are ratio matched for optimum low frequency common mode rejection.

The input attenuators provide four 12 dB steps from 0 dB to -36 dB. Relay K441 is energized in the 0 dB state, K442 for -12 dB, and K342 for -24 dB. -36 dB is the default state with all three relays off. Refer to TABLE PHA2.1 more information concerning attenuator step selection versus input voltage. C0401 adjusts the attenuator high frequency flatness above approximately 10 kHz. R1409 and R2405 trim the total input resistance to be 100 kOhms, each side to ground.

Signal Preamp <2>

The selected and attenuated input signal is buffered and amplified by U232, U231, U22, and U412. Diodes D4301-4304, and D4307-4310 provide overload protection by clamping the op-amp input voltage to approximately ±13 V, determined by zener diodes D4305 and D4306. High frequency distortion due to the non-linear capacitance of the diodes is minimized by the inherent bootstrap action of this configuration.

NOTE: The residual leakage current of the input clamping diodes can exhibit significant optical modulation. Exposure to fluorescent lighting with the top cover removed may cause an increase in input hum products due to this effect!

When no attenuation has been selected the incandescent lamps R541 and R542, located on schematic <1>, limit input current during an overload condition. Normally the lamps are cold and present a low resistance (typically 100-130 Ohms) to the input circuit. During an overload the lamp resistance rises dramatically.

The pre-amplifier gain is controlled by relays K341 and K24, providing +12 dB and +6 dB steps respectively. If both are energized the preamp gain is +18 dB. K31 switches an additional +12 dB gain stage comprising U412, R4201, and R4202 for higher sensitivity. See TABLE PHA2.1 or more information concerning pre-amplifier gain states versus input voltage.

U22 is a unity gain differential input to single ended output amplifier. Common mode rejection is trimmed by R0301 which balances the + and - input signal path gains. U32A and its related components comprise a dc servo that maintains a near zero dc offset condition at the output of U22 under all gain conditions. The output of the servo integrator is feedback through R3202 into the + signal path. C4202 and R4205 provide low frequency compensation that corrects for the input ac coupling rolloff below about 30 Hz.

The output signal from relay K31 is labeled BSIG and is routed several places. It is connected to the channel B input ranging comparators shown on schematic <3>, to K53, and to the BSIG monitor buffers U21A and U21B. The output from U21A is coupled through R2102 and a shielded cable to the front panel CHANNEL B MONITOR connector. Note that there is a 6 dB loss introduced by R2201 and R2202. U21B provides the buffered BSIG for routing to the DSP module in SYS-2xx and SYS-3xx configurations. Under normal autoranging conditions BSIG will vary over a 6-7 dB window between approximately 1.60-3.75 Vpeak.

K53 controls whether ASIG (supplied through J43-6) or BSIG is routed to J43-8 to become the MAINSIG. K53 is off for channel A, on for channel B. ALTSIG is the opposite or unselected channel and is routed to J43-7 for use by the LEVEL meter located on the DIS-2 board in CROSSTALK or DUAL CHANNEL modes.

TABLE PHA2.1
CHANNEL-B INPUT RANGES & SYSTEM GAIN

RANGE[1]	ATTENUATION	K441	K442	K342	PREAMP GAIN	K24	K341	K31	TOTAL GAIN[2]
160 V[3]	-36dB	0	0	0	0dB	0	0	0	-36dB
80 V	-36dB	0	0	0	+6dB	1	0	0	-30dB
40 V	-24dB	0	0	1	0dB	0	0	0	-24dB
20 V	-24dB	0	0	1	+6dB	1	0	0	-18dB
10 V	-12dB	0	1	0	0dB	0	0	0	-12dB
5 V	-12dB	0	1	0	+6dB	1	0	0	-6dB
2.5 V	0dB	1	0	0	0dB	0	0	0	0dB
1.2 V	0dB	1	0	0	+6dB	1	0	0	+6dB
600 mV	0dB	1	0	0	+12dB	0	1	0	+12dB
300 mV	0dB	1	0	0	+18dB	1	1	0	+18dB
160 mV	0dB	1	0	0	+24dB	0	1	1	+24dB
80 mV	0dB	1	0	0	+30dB	1	1	1	+30dB

1 Maximum rms sinewave amplitude for linear operation.
2 INPUT to BSIG
3 140 Vrms is the maximum rated input voltage

Autorange Comparators <3>

The signal from the B channel input amplifier is fed through the preemphasis network R5101, R5106, C5102. This compensates for the slew rate limitations of the op-amps in the preamplifier, reducing amplitude of signal at high frequencies before an up-range occurs. This signal feeds four comparators, two sense the need to up-range and two sense the need to downrange. The two comparators in each pair are used to sense the positive peak value and negative peak value of the signal.

Consider the operation of U61A. Its negative input is connected to the signal input and its positive input is connected to a +1.75V reference. The output of the comparator will go low when positive signal peak exceeds this reference. U61B performs the same comparison function for negative peaks. The outputs of the two comparators are wired together. Since these are open collector outputs, if either comparator senses too large a peak value the output line will go low. R8101 and R8104 level shift the -15 V output of the comparators to the +5 V logic of U81. When the comparator output goes low it will set the flip-flop U81A. The microprocessor on the LVF-2 board reads the output of this flip-flop through tri-state buffer U91 and knows if an overrange condition occurred. When the microprocessor reads this information the clock input of U81 is strobed, clearing the overrange indication. The flip-flop allows momentary signal overloads to be detected with infrequent monitoring by the microprocessor.

Comparators U61C and U61D perform the same comparison function on the signal at a 6 dB lower amplitude. If the signal is below this level the microprocessor knows that the input gain must be increased. When the correct input range is achieved the upper comparator output will be high and the lower comparator output will be low. Any change of state in the comparators causes an uprange or downrange as appropriate.

Comparators U411A and U411B monitor the signal level against a 100 mV reference. This is used to sense when the signal is of insufficient amplitude to guarantee accurate phasemeter operation. When this occurs the output of the comparators will rise. This signal must remain under this minimum level until C5101 charges for the processor to shut down the phasemeter reading.

Tri-state buffer U91 allows the microprocessor to read the state of various logic signals on the phasemeter board. In addition to the three range comparison signals described above, the state of the Channel B input termination resistors (/TERM B) and a ranging signal (PHASEN) from the phasemeter are monitored.

Phasemeter <4>

The phasemeter is shown in FIGURE PHA2.1. The Channel A and Channel B signals enter through R5202 and R5201. When line LB goes to 0 V, JFET switches Q5202 and Q5201 connect the capacitors C5203 and C5204 to ground. These form lowpass filter circuits which reduce the interfering effects of noise components greater than approximately 100 kHz. These signals are buffered by U52 which drives the comparators and peak detectors. The operation of the Channel A circuits will be described, the channel B circuits are identical.

Diodes D6301 and D6302 cause the output of U62A to be offset from the input by one diode drop. For positive signal voltages the output will be 0.6 V higher than the input, for negative voltages the output will be 0.6 V lower than the input. This output signal is rectified by diodes D6201 and D6202. The positive voltage from D6201 is stored on capacitor C6201 and serves as the positive threshold reference for the comparators. The negative voltage from D6202 is stored on capacitor C6202 and serves as the negative reference for the comparators. The input signal is developed across R6306 and fed to the four comparators in U721 and U722. Each comparator compares the signal to a different reference, one to each of the two references discussed above and two at zero.

Series resistor capacitor networks R6203-C6201 and R6207-C6203 provide hysteresis to prevent oscillation on the comparator transitions without disturbing the dc value of the reference voltage. Since U721A and U722B are comparing to ground the hysteresis is provided with resistors only. R6208 offsets the hysteresis voltage so that the comparison point of U722B for positive going zero crossings is 0 V. The outputs of the comparators are used to drive dual flip-flop U831. The waveforms for all of the comparator outputs and the flip-flop outputs are shown in FIGURE PHA2.1. The resulting flip-flop outputs are square waves in which the rising edge represents one zero crossing of the input signal. The use of separate comparators to compare the zero crossing and the peak provides a large amount of hysteresis and reduces the sensitivity of the phasemeter to interfering noise.

Dual flip-flop U94 and data selectors U841 and U832 form a pair of edge triggered flip-flops. The data selectors also implement the 0-360° or ±180° range selection. Consider the operation of U841 and U94B. Consider the operation when the range select line /180 is low. U841 is an electronic switch which selects the input to the flip-flop. Its position is selected by the logic level at its A input. Suppose the flip-flop U94 is cleared so that the /Q output is high. This forces the D input high and sets the switch to the 1 position. The squared version of the channel B input is fed to the clock input of the flip-flop. When the next positive transition of this signal occurs the flip-flop will be clocked and the outputs will change state. This will set the switch to its 0 input, connecting the squared version of the channel A signal to the clock input. The next positive transition of the channel A signal will cause the flip flop to change state back again.

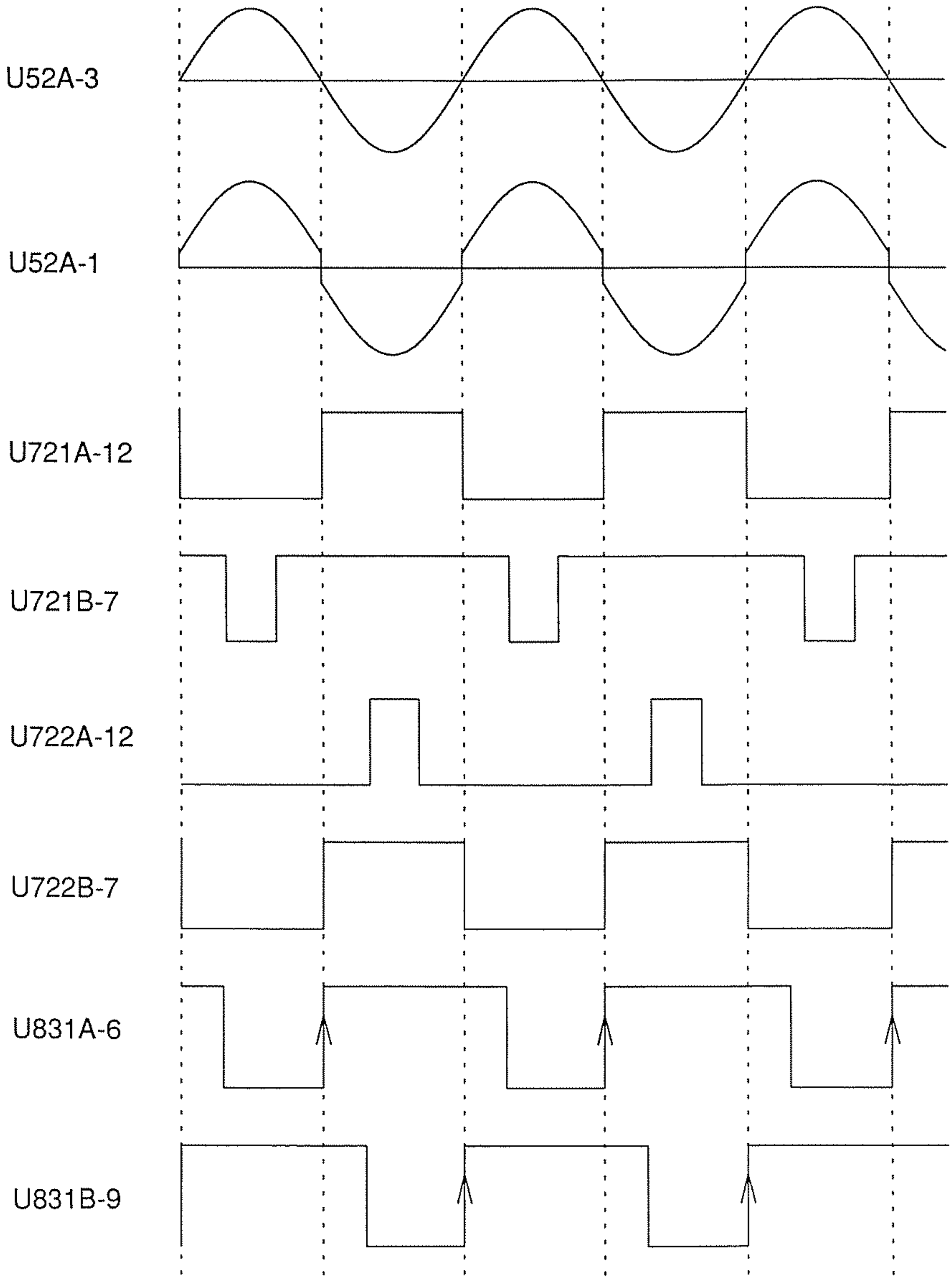
The output of the flip-flop will then represent the time difference between the two channels. The average voltage of this waveform is proportional to the phase difference between the two channels. R9401 and C9401 perform this averaging. The result is fed to the voltage to frequency converter U82. The output frequency is sent to the LVF-2 board for counting by the microprocessor circuits. An identical data switch and flip-flop circuit comprising U832 and U94A measures the phase shift between the negative going zero crossings. This is averaged through R9402 into the same capacitor (C9401) as the previous circuit. This reduces errors on the measurement due to asymmetry on the signal waveforms. At low frequencies the averaging provided by C9401 is not enough to suppress ripple. Q9501 switches in C9501 to increase the filtering.

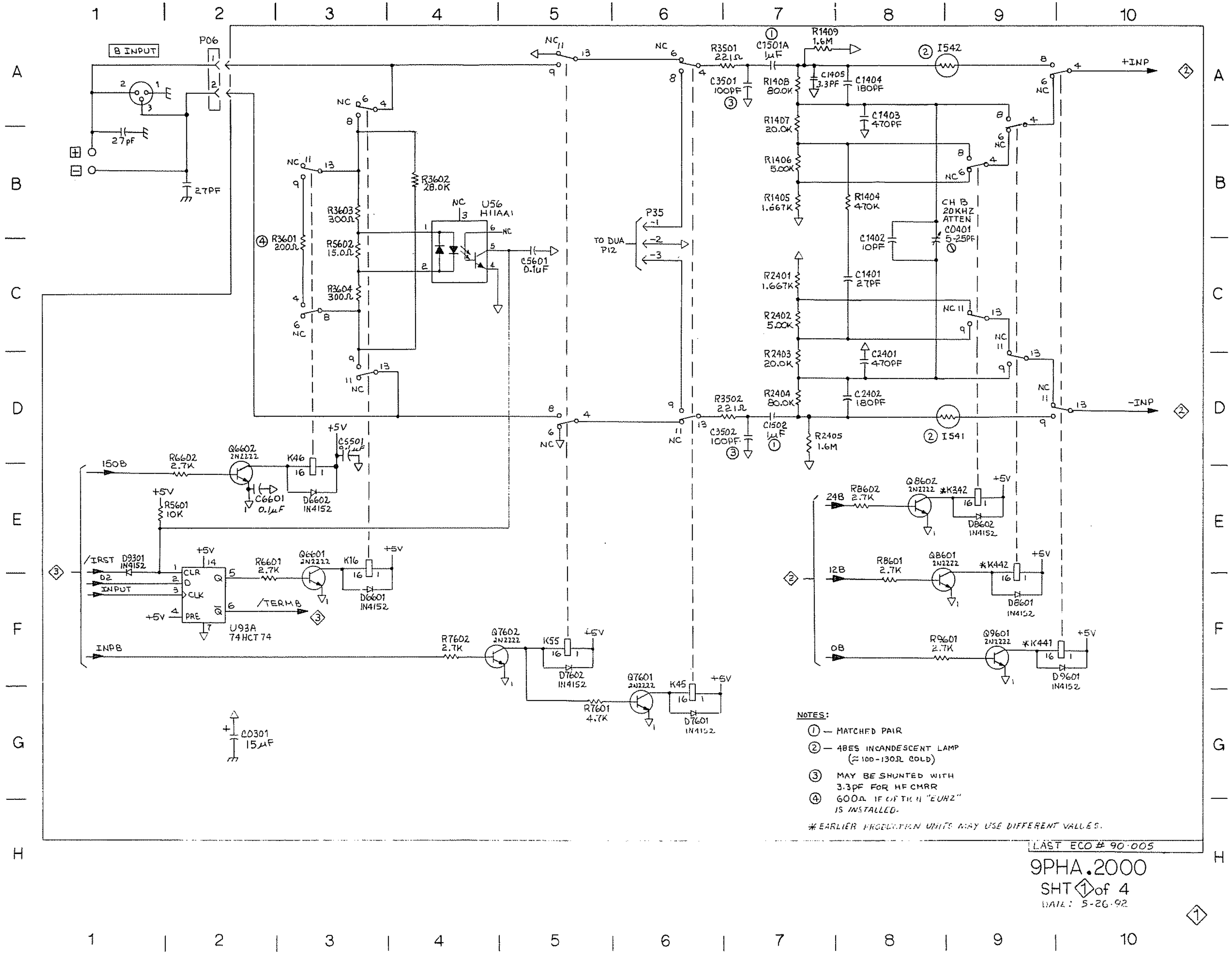
Since the phase measurement is the average value of the voltage pulse from U94 it is important that the amplitude of this pulse be well controlled and noise free. This is provided by a separate +5V power supply, regulated by U95A. This is an open collector comparator which compares its output to a reference voltage obtained from D7502.

The discussion so far has assumed the phasemeter is operating with a 0-360° range. If the signals being measured are in phase, the phasemeter may read 0° or 360°. If the circuit bounces back and forth between these values quickly the display will read the average, or something near 180°. By comparing the rising edge of one signal to the falling edge of the other signal a ±180° range is achieved. This is accomplished by using the 2 and 3 inputs of the data selectors U841 and U832. When the 180 line is high the A input of the data selectors will select between the 2 and 3 inputs instead of the 0 and 1 inputs.

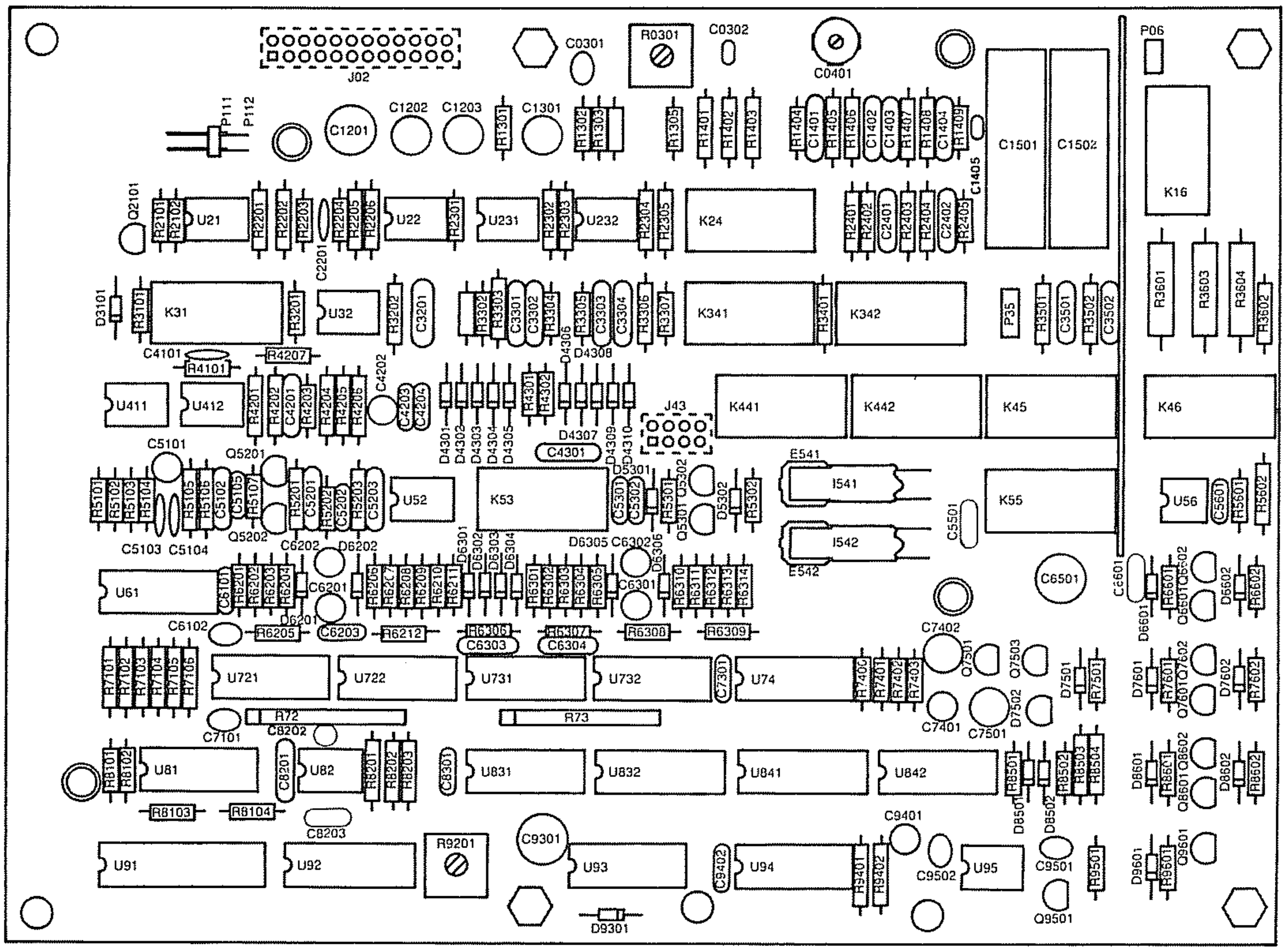
A simple phase comparison between the two input channels is performed by the exclusive-OR gate U842A. The comparison pulses at its output are averaged by R7401 and C7401. If the signals are within ±90° this voltage will be low. If the signals are within 90-270° the voltage will be high. This is fed into U842B and U842C which are used as a comparator at approximately +2.5 V. The logic output PHASEN is then fed to the tri-state buffer U61 for reading by the microprocessor. This information is passed to the host computer with the phase reading. C7402 and Q7501 increase the averaging at low frequencies to reduce the ripple on the comparison voltage. R7403 provides hysteresis to prevent oscillation at comparison voltages near the 2.5 V threshold.

Figure PHA2.1 PHASEMETER OPERATION

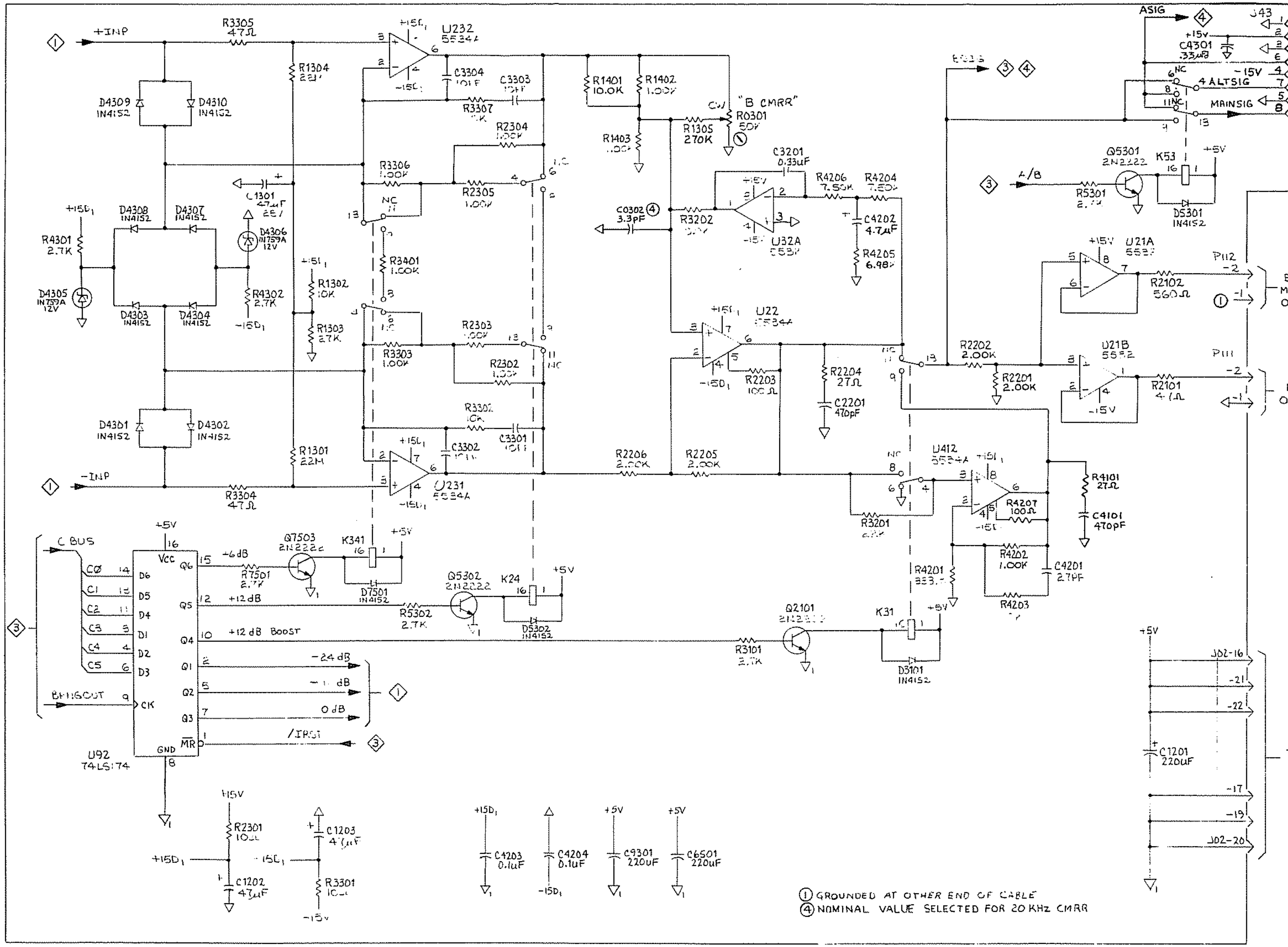




B INPUT
P06
27pF
27PF
R3601 200Ω
R3603 300Ω
R5602 15.0Ω
R3604 300Ω
R3602 28.0K
U56 H11AA1
C5601 0.1uF
TO DUA P12
P35
R3501 221Ω
C3501 100PF
C1501A 1uF
R1409 1.6M
C1405 3.3PF
C1404 180PF
R1408 80.0K
R1407 20.0K
C1403 470PF
R1406 5.00K
R1405 1.667K
R1404 470K
C1402 10PF
CH B 20KHZ ATTEN
C0401 5-25PF
C1401 27PF
R2401 1.667K
R2402 5.00K
R2403 20.0K
C2401 470PF
R2404 80.0K
C2402 180PF
R3502 221Ω
C3502 100PF
C1502 1uF
R2405 1.6M
I542
I541
+INP
-INP
150B
R6602 2.7K
Q6602 2N2222
K46
C5501 0.1uF
C6601 0.1uF
D6602 1N4152
R5601 10K
/IRST
D9301 1N4152
D2
INPUT
CLR
CLK
PRE
/TERMB
U93A 74HCT74
R6601 2.7K
Q6601 2N2222
K16
D6601 1N4152
INPB
R7602 2.7K
Q7602 2N2222
K55
D7602 1N4152
R7601 4.7K
Q7601 2N2222
K45
D7601 1N4152
C0301 15uF
24B
R8602 2.7K
Q8602 2N2222
*K342
D8602 1N4152
12B
R8601 2.7K
Q8601 2N2222
*K442
D8601 1N4152
0B
R9601 2.7K
Q9601 2N2222
*K441
D9601 1N4152
NOTES:
① — MATCHED PAIR
② — 48ES INCANDESCENT LAMP (≈100-130Ω COLD)
③ MAY BE SHUNTED WITH 3.3pF FOR HF CMRR
④ 600Ω IF OPTION "EUR2" IS INSTALLED.
*EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.
LAST ECO # 90-005
9PHA.2000
SHT 1 of 4
DATE: 5-26-92



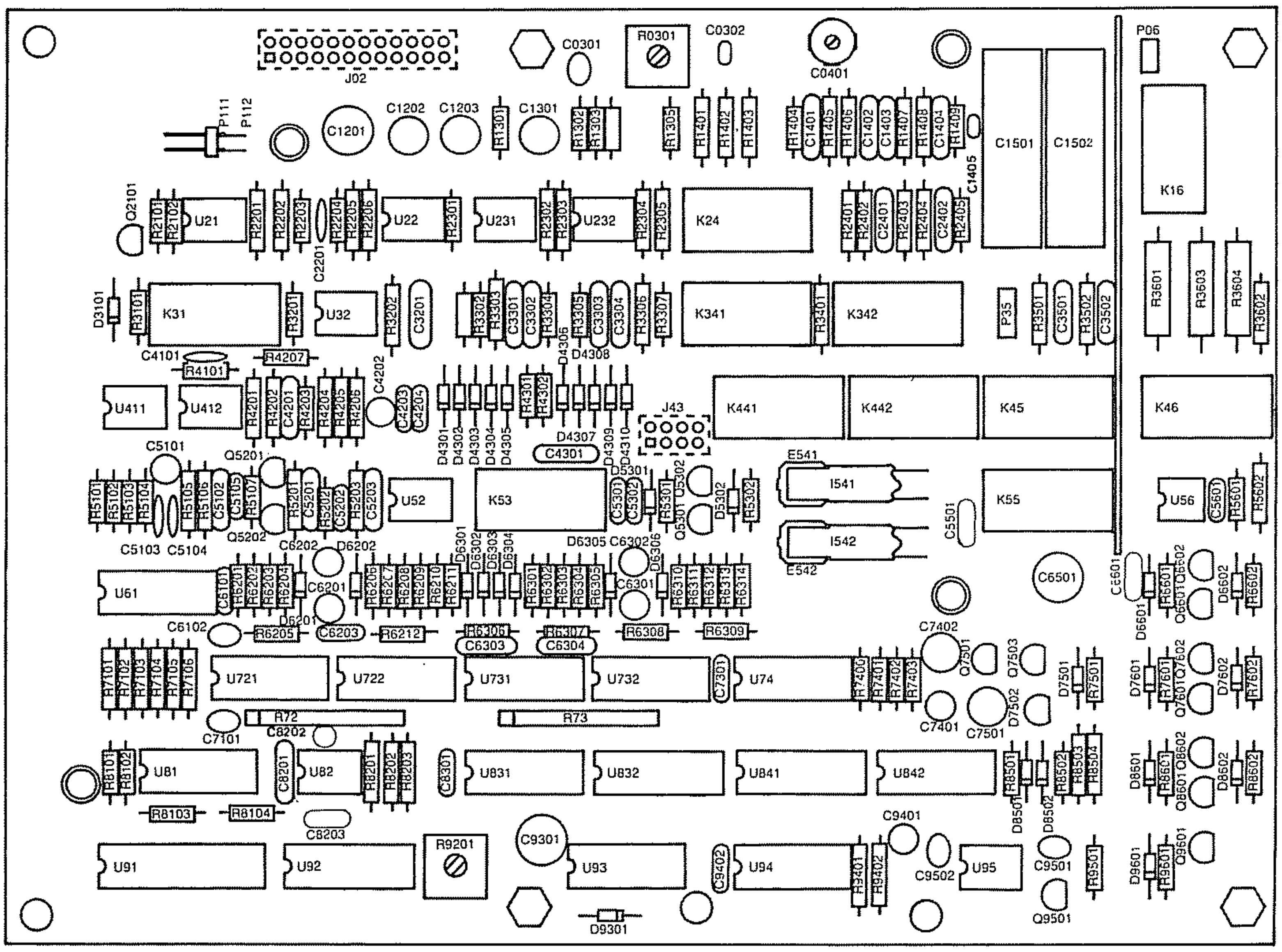
DUAL INPUT ANALYZER & PHASE OPTION 9PHA.2000 (6200.PHA1.7)



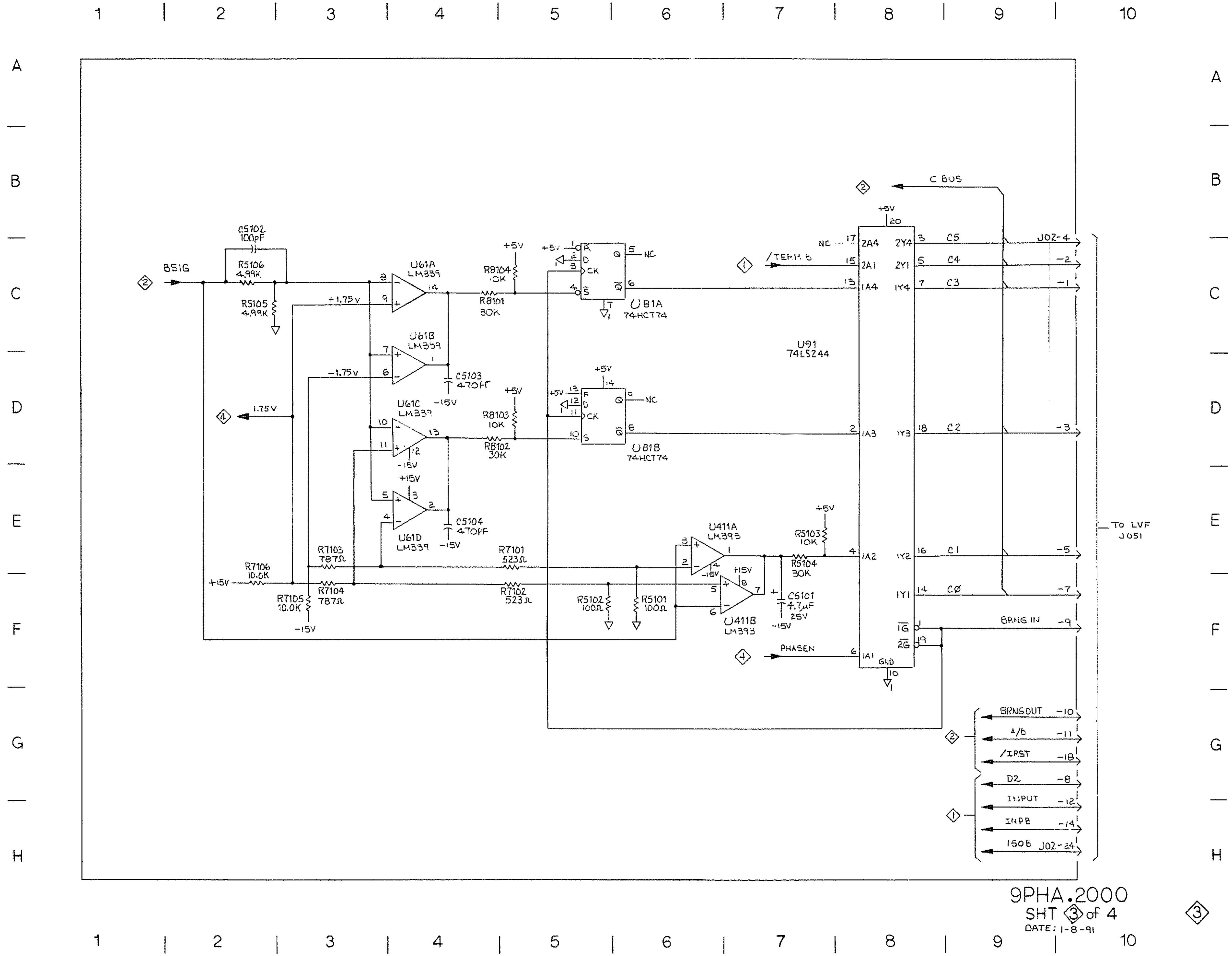
9PHA.2000

SHT 2 of 4

DATE:



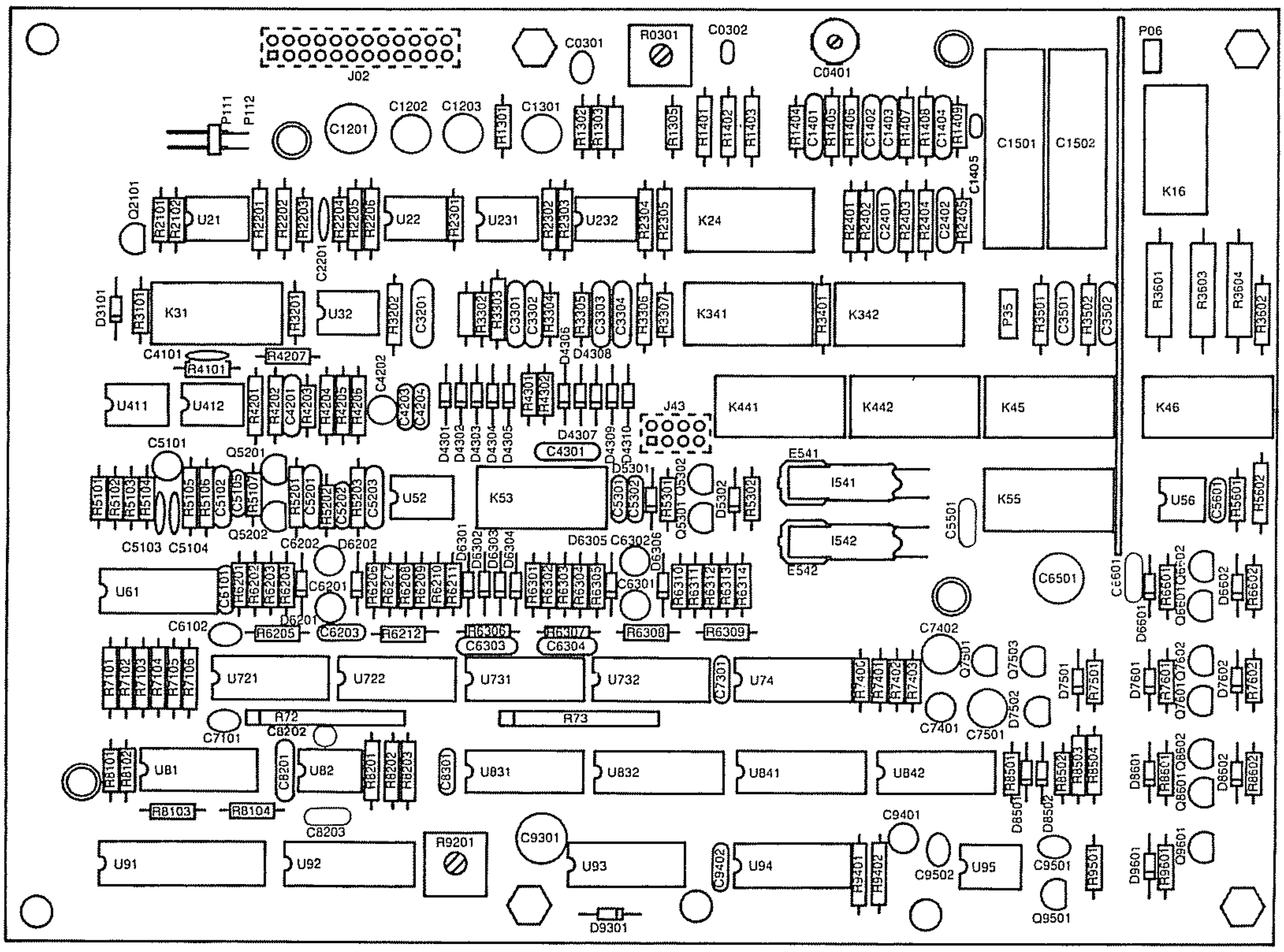
DUAL INPUT ANALYZER & PHASE OPTION 9PHA.2000 (6200.PHA1.7)



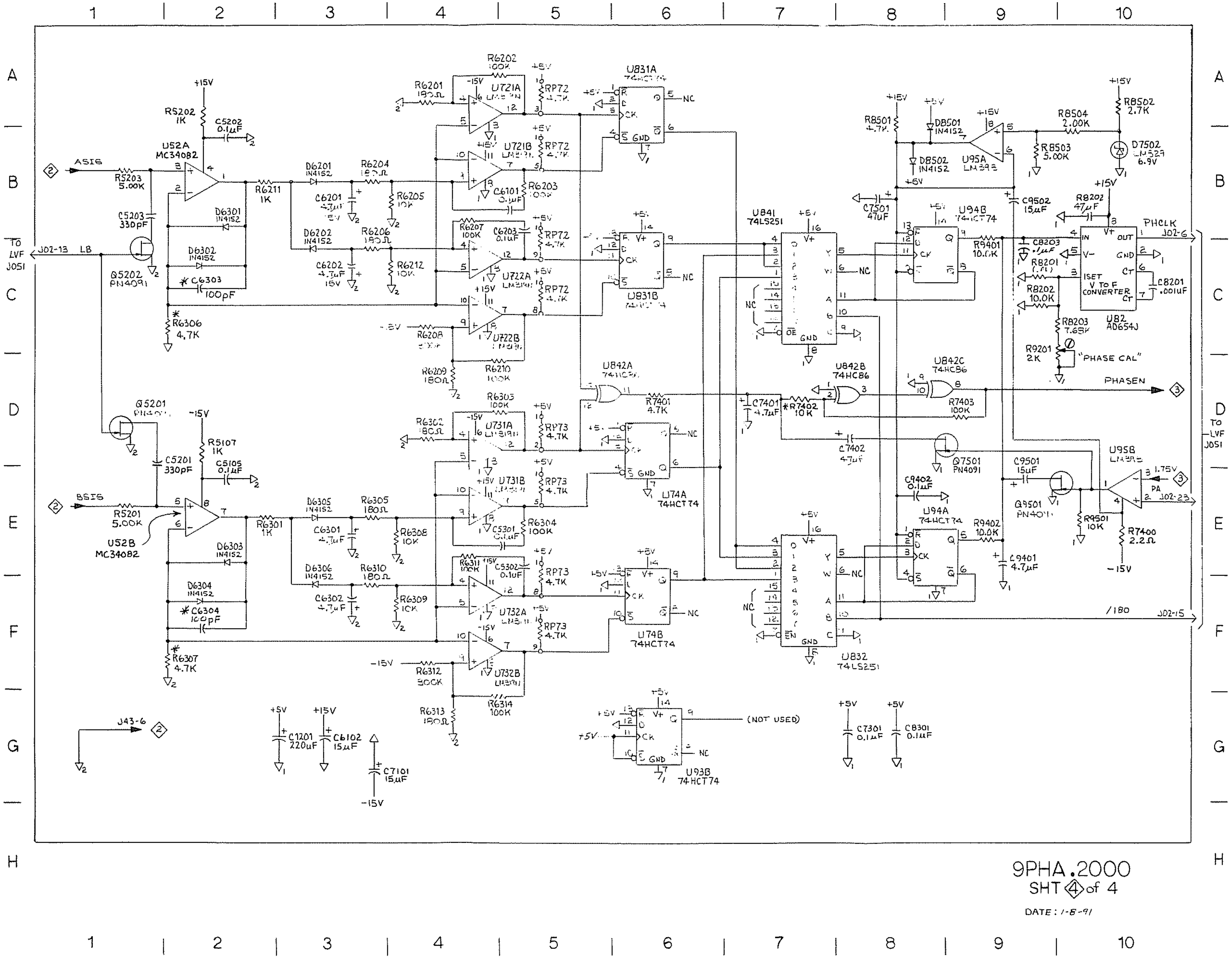
9PHA.2000

SHT 3 of 4

DATE: 1-8-91



DUAL INPUT ANALYZER & PHASE OPTION 9PHA.2000 (6200.PHA1.7)



9PHA.2000
SHT 4 of 4
DATE: 1-8-91

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION
C0301	1G2	2832.0156	CAP TA-EL 25V 20% 15uF
C0302	2B5	2172.0339	CAP CERAM 100V 20% 3.3pF
C0401	1C8	4450.0250	VAR CAP PC 5-25pF
C1201	4G2	2911.0227	CAP AL-EL 10V +80/-20% 220uF
C1202	2G2	2932.0476	CAP AL-EL 25V 20% 47uF
C1203	2G3	2932.0476	CAP AL-EL 25V 20% 47uF
C1301	2B3	2932.0476	CAP AL-EL 25V 20% 47uF
C1401	1C8	2294.0270	CAP MICA 500V 5% 27pF
C1402	1C8	2294.0100	CAP MICA 500V 5% 10pF
C1403	1B8	2296.0471	CAP MICA 500V 1% 470pF
C1404	1A8	2296.0181	CAP MICA 500V 1% 180pF
C1405	1A7	2172.0339	CAP CERAM 100V 20% 3.3pF
C1501	1A7	2694.0105	CAP POLYC 250V 5% 1uF
C1502	1D7	2694.0105	CAP POLYC 250V 5% 1uF
C2201	2D7	2172.0471	CAP CERAM 100V 20% 470pF
C2401	1D8	2296.0471	CAP MICA 500V 1% 470pF
C2402	1D7	2296.0181	CAP MICA 500V 1% 180pF
C3201	2B7	2454.0334	CAP POLYE 50V 5% .33uF
C3301	2D4	2294.0100	CAP MICA 500V 5% 10pF
C3302	2D4	2294.0100	CAP MICA 500V 5% 10pF
C3303	2A4	2294.0100	CAP MICA 500V 5% 10pF
C3304	2A4	2294.0100	CAP MICA 500V 5% 10pF
C3501	1A7	2296.0101	CAP MICA 500V 1% 100pF
C3502	1E7	2296.0101	CAP MICA 500V 1% 100pF
C4101	2E9	2172.0471	CAP CERAM 100V 20% 470pF
C4201	2E8	2294.0270	CAP MICA 500V 5% 27pF
C4202	2B7	2942.0475	CAP AL-EL 35V 20% 4.7uF
C4203	2G4	2172.0104	CAP CERAM 100V 20% .1uF
C4204	2G5	2172.0104	CAP CERAM 100V 20% .1uF
C4301	2A10	2454.0334	CAP POLYE 50V 5% .33uF
C5101	3F7	2942.0475	CAP AL-EL 35V 20% 4.7uF
C5102	3B2	2296.0101	CAP MICA 500V 1% 100pF
C5103	3D4	2172.0471	CAP CERAM 100V 20% 470pF
C5104	3E4	2172.0471	CAP CERAM 100V 20% 470pF
C5105	4D2	2172.0104	CAP CERAM 100V 20% .1uF
C5201	4D1	2296.0331	CAP MICA 500V 1% 330pF
C5202	4A2	2172.0104	CAP CERAM 100V 20% .1uF
C5203	4B1	2296.0331	CAP MICA 500V 1% 330pF
C5301	4E4	2172.0104	CAP CERAM 100V 20% .1uF
C5302	4E5	2172.0104	CAP CERAM 100V 20% .1uF
C5501	1D3	2172.0104	CAP CERAM 100V 20% .1uF
C5601	1B5	2172.0104	CAP CERAM 100V 20% .1uF
C6101	4B5	2172.0104	CAP CERAM 100V 20% .1uF
C6102	4G3	2832.0156	CAP TA-EL 25V 20% 15uF
C6201	4B3	2942.0475	CAP AL-EL 35V 20% 4.7uF
C6202	4C3	2942.0475	CAP AL-EL 35V 20% 4.7uF
C6203	4B5	2172.0104	CAP CERAM 100V 20% .1uF
C6301	4E3	2942.0475	CAP AL-EL 35V 20% 4.7uF
C6302	4F3	2942.0475	CAP AL-EL 35V 20% 4.7uF
C6303	4C2	2296.0101	CAP MICA 500V 1% 100pF
C6304	4F2	2296.0101	CAP MICA 500V 1% 100pF
C6501	2G6	2911.0227	CAP AL-EL 10V +80/-20% 220uF

REPLACEABLE ELECTRICAL PARTS LIST: 9PHA.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C6601	1E3	2172.0104	CAP CERAM 100V 20%	.1uF
C7101	4G3	2832.0156	CAP TA-EL 25V 20%	15uF
C7301	4G8	2172.0104	CAP CERAM 100V 20%	.1uF
C7401	4D7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C7402	4D8	2932.0476	CAP AL-EL 25V 20%	47uF
C7501	4B4	2932.0476	CAP AL-EL 25V 20%	47uF
C8201	4C10	2276.0102	CAP MICA 100V 1%	.001uF
C8202	4B10	2932.0476	CAP AL-EL 25V 20%	47uF
C8203	4C10	2172.0104	CAP CERAM 100V 20%	.1uF
C8301	4G8	2172.0104	CAP CERAM 100V 20%	.1uF
C9301	2G5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C9401	4E9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C9402	4E8	2172.0104	CAP CERAM 100V 20%	.1uF
C9501	4E9	2832.0156	CAP TA-EL 25V 20%	15uF
C9502	4B9	2832.0156	CAP TA-EL 25V 20%	15uF
D3101	2F8	3110.4152	DIODE SIGNAL	4152
D4301	2D2	3110.4152	DIODE SIGNAL	4152
D4302	2D2	3110.4152	DIODE SIGNAL	4152
D4303	2C1	3110.4152	DIODE SIGNAL	4152
D4304	2C2	3110.4152	DIODE SIGNAL	4152
D4305	2C1	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D4306	2B2	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D4307	2B2	3110.4152	DIODE SIGNAL	4152
D4308	2B1	3110.4152	DIODE SIGNAL	4152
D4309	2A2	3110.4152	DIODE SIGNAL	4152
D4310	2A2	3110.4152	DIODE SIGNAL	4152
D5301	2B10	3110.4152	DIODE SIGNAL	4152
D5302	2E5	3110.4152	DIODE SIGNAL	4152
D6201	4B3	3110.4152	DIODE SIGNAL	4152
D6202	4B3	3110.4152	DIODE SIGNAL	4152
D6301	4B2	3110.4152	DIODE SIGNAL	4152
D6302	4C2	3110.4152	DIODE SIGNAL	4152
D6303	4E2	3110.4152	DIODE SIGNAL	4152
D6304	4F2	3110.4152	DIODE SIGNAL	4152
D6305	4E3	3110.4152	DIODE SIGNAL	4152
D6306	4E3	3110.4152	DIODE SIGNAL	4152
D6601	1E3	3110.4152	DIODE SIGNAL	4152
D6602	1E3	3110.4152	DIODE SIGNAL	4152
D7501	2E4	3110.4152	DIODE SIGNAL	4152
D7502	4B10	3131.0069	DIODE PREC REF ZEN 6.9V	LM329
D7601	1F6	3110.4152	DIODE SIGNAL	4152
D7602	1F5	3110.4152	DIODE SIGNAL	4152
D8501	4A8	3110.4152	DIODE SIGNAL	4152
D8502	4B8	3110.4152	DIODE SIGNAL	4152
D8601	1F9	3110.4152	DIODE SIGNAL	4152
D8602	1E9	3110.4152	DIODE SIGNAL	4152
D9301	1E1	3110.4152	DIODE SIGNAL	4152
D9601	1F10	3110.4152	DIODE SIGNAL	4152
E35		4132.0155	CABLE 2 COND SHLD 15.5	3 PIN
E541		4261.0001	FUSE CLIP PC	

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION
E542		4261.0001	FUSE CLIP PC
I541	1D9	4700.4840	LAMP INCANDESCENT 48V 40mA
I542	1A9	4700.4840	LAMP INCANDESCENT 48V 40mA
J02	2F10,2G10,3C-H10,4C-F10	4221.1024	JACK PC 2 X .1 24 PIN
J43	2A10	4221.1008	JACK PC 2 X .1 8 PIN
K16	1A3,1D3,1E3	4530.0002	RELAY PC LOW POWER DPDT
K24	2B5,2C5,2E5	4530.0002	RELAY PC LOW POWER DPDT
K31	2C7,2D7,2E7	4530.0002	RELAY PC LOW POWER DPDT
K341	2B3,2C3,2E3	4530.0002	RELAY PC LOW POWER DPDT
K342	1B9,1C9,1E9	4530.0002.1	RELAY PC LOW POWER STABLE DPDT
K441	1A10,1D10,1F10	4530.0002.1	RELAY PC LOW POWER STABLE DPDT
K442	1B9,1D9,1F9	4530.0002.1	RELAY PC LOW POWER STABLE DPDT
K45	1A6,1D6,1F6	4530.0002	RELAY PC LOW POWER DPDT
K46	1B3,1C3,1D3	4530.0002	RELAY PC LOW POWER DPDT
K53	2A10,2B10	4530.0002	RELAY PC LOW POWER DPDT
K55	1A5,1D5,1F5	4530.0002	RELAY PC LOW POWER DPDT
P02		4221.0072.2	PLUG PC 2X.1 X1.03 72 PIN
P06	1A2	4221.0036	PLUG PC .1 X.43 36 PIN
P111	2C10	4221.0172	PLUG PC 90′ 2X.1 X.39 72 PIN
P35	1B6	4221.0036	PLUG PC .1 X.43 36 PIN
P43		4221.0072.2	PLUG PC 2X.1 X1.03 72 PIN
Q2101	2E6	3211.2222	XSTR NPN TO92 PN2222A
Q5201	4D1	3214.4091	XSTR FET TO92 PN4091
Q5202	4C1	3214.4091	XSTR FET TO92 PN4091
Q5301	2B9	3211.2222	XSTR NPN TO92 PN2222A
Q5302	2E4	3211.2222	XSTR NPN TO92 PN2222A
Q6601	1E3	3211.2222	XSTR NPN TO92 PN2222A
Q6602	1E2	3211.2222	XSTR NPN TO92 PN2222A
Q7501	4D9	3214.4091	XSTR FET TO92 PN4091
Q7503	2E3	3211.2222	XSTR NPN TO92 PN2222A
Q7601	1F6	3211.2222	XSTR NPN TO92 PN2222A
Q7602	1F4	3211.2222	XSTR NPN TO92 PN2222A
Q8601	1F9	3211.2222	XSTR NPN TO92 PN2222A
Q8602	1E8	3211.2222	XSTR NPN TO92 PN2222A
Q9501	4E9	3214.4091	XSTR FET TO92 PN4091
Q9601	1F9	3211.2222	XSTR NPN TO92 PN2222A
R0301	2B6	4412.0503	POT TRIM PC ENC 50K
R1301	2D3	1214.0226	RES 1/4W C FLM 5% 22M
R1302	2C3	1214.0103	RES 1/4W C FLM 5% 10K
R1303	2C3	1214.0273	RES 1/4W C FLM 5% 27K
R1304	2A3	1214.0226	RES 1/4W C FLM 5% 22M
R1305	2B6	1214.0274	RES 1/4W C FLM 5% 270K
R1401	2A5	1136.1002	RES 1/8W M FLM 1% 10.0K
R1402	2A5	1139.1001	RES 1/8W M FLM .1% 1.00K
R1403	2A5	1139.1001	RES 1/8W M FLM .1% 1.00K

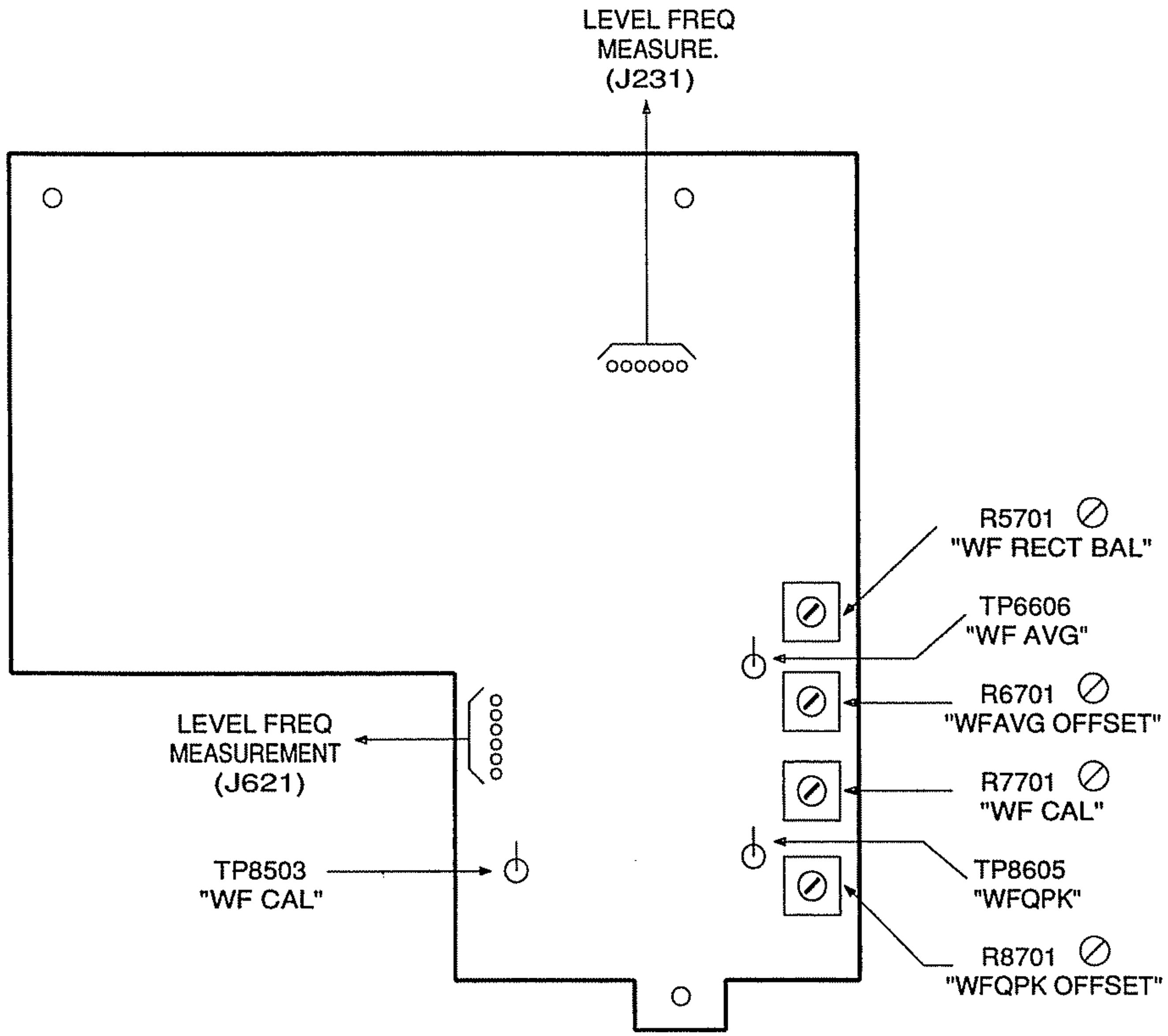
REPLACEABLE ELECTRICAL PARTS LIST: 9PHA.2000

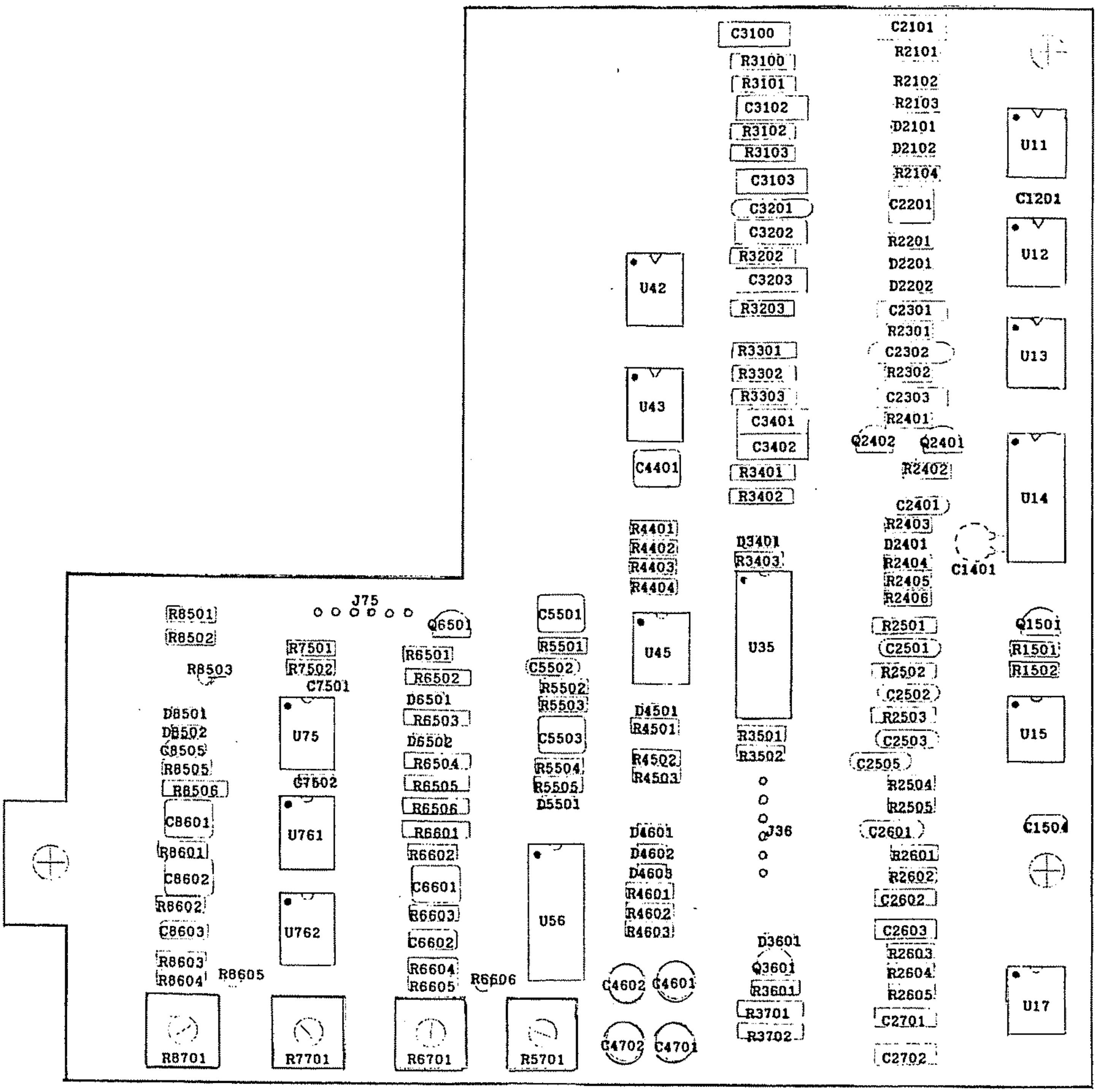
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R1404	1B8	1214.0434	RES 1/4W C FLM 5%	430K
R1405	4B7	1139.1671	RES 1/8W M FLM .1%	1.667K
R1406	1C7	1139.5001	RES 1/8W M FLM .1%	5.00K
R1407	1B7	1139.2002	RES 1/8W M FLM .1%	20.0K
R1408	1A7	1139.8002	RES 1/8W M FLM .1%	80.0K
R1409	1A7	1214.0165	RES 1/4W C FLM 5%	1.6M
R2101	2C10	1214.0470	RES 1/4W C FLM 5%	47
R2102	2C10	1214.0561	RES 1/4W C FLM 5%	560
R2201	2D8	1139.2001	RES 1/8W M FLM .1%	2.00K
R2202	2D8	1139.2001	RES 1/8W M FLM .1%	2.00K
R2203	2C6	1214.0101	RES 1/4W C FLM 5%	100
R2204	2C7	1214.0270	RES 1/4W C FLM 5%	27
R2205	2D6	1139.2001	RES 1/8W M FLM .1%	2.00K
R2206	2D5	1139.2001	RES 1/8W M FLM .1%	2.00K
R2301	2G2	1214.0100	RES 1/4W C FLM 5%	10
R2302	2C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2303	2C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2304	2B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2305	2B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2401	1C7	1139.1671	RES 1/8W M FLM .1%	1.667K
R2402	1C7	1139.5001	RES 1/8W M FLM .1%	5.00K
R2403	1D7	1139.2002	RES 1/8W M FLM .1%	20.0K
R2404	1D7	1139.8002	RES 1/8W M FLM .1%	80.0K
R2405	1E7	1214.0165	RES 1/4W C FLM 5%	1.6M
R3101	2E6	1214.0272	RES 1/4W C FLM 5%	2.7K
R3201	2E7	1214.0223	RES 1/4W C FLM 5%	22K
R3202	2B6	1136.1002	RES 1/8W M FLM 1%	10.0K
R3301	2G3	1214.0100	RES 1/4W C FLM 5%	10
R3302	2D4	1214.0103	RES 1/4W C FLM 5%	10K
R3303	2C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3304	2D2	1214.0470	RES 1/4W C FLM 5%	47
R3305	2A2	1214.0470	RES 1/4W C FLM 5%	47
R3306	2B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3307	2A4	1214.0103	RES 1/4W C FLM 5%	10K
R3401	2B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3501	1A7	1136.2210	RES 1/8W M FLM 1%	221
R3502	1D7	1136.2210	RES 1/8W M FLM 1%	221
R3601	1B3	1656.2000	RES 3W W WND 1%	200
R3602	1B4	1136.2802	RES 1/8W M FLM 1%	28.0K
R3603	1B3	1656.3000	RES 3W W WND 1%	300
R3604	1C3	1656.3000	RES 3W W WND 1%	300
R36E1	1C3	1656.6000	RES 3W W WND 1%	600
R4101	2D9	1214.0270	RES 1/4W C FLM 5%	27
R4201	2E8	1139.3330	RES 1/8W M FLM .1%	333.3
R4202	2E8	1139.1001	RES 1/8W M FLM .1%	1.00K
R4203	2E8	1214.0103	RES 1/4W C FLM 5%	10K
R4204	2B7	1136.7501	RES 1/8W M FLM 1%	7.50K
R4205	2B7	1136.6981	RES 1/8W M FLM 1%	6.98K
R4206	2B7	1136.7501	RES 1/8W M FLM 1%	7.50K
R4207	2E8	1214.0101	RES 1/4W C FLM 5%	100
R4301	2B1	1214.0272	RES 1/4W C FLM 5%	2.7K
R4302	2C2	1214.0272	RES 1/4W C FLM 5%	2.7K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION			
R5101	3F6	1214.0101	RES	1/4W C FLM 5%		100
R5102	3F5	1214.0101	RES	1/4W C FLM 5%		100
R5103	3E7	1214.0103	RES	1/4W C FLM 5%		10K
R5104	3E7	1214.0303	RES	1/4W C FLM 5%		30K
R5105	3C2	1136.4991	RES	1/8W M FLM 1%		4.99K
R5106	3C2	1136.4991	RES	1/8W M FLM 1%		4.99K
R5107	4D2	1214.0102	RES	1/4W C FLM 5%		1K
R5201	4E1	1139.5001	RES	1/8W M FLM .1%		5.00K
R5202	4A2	1214.0102	RES	1/4W C FLM 5%		1K
R5203	4B1	1139.5001	RES	1/8W M FLM .1%		5.00K
R5301	2B9	1214.0272	RES	1/4W C FLM 5%		2.7K
R5302	2E4	1214.0272	RES	1/4W C FLM 5%		2.7K
R5601	1E1	1214.0103	RES	1/4W C FLM 5%		10K
R5602	1B3	1136.1509	RES	1/8W M FLM 1%		15.0
R6201	4A4	1214.0181	RES	1/4W C FLM 5%		180
R6202	4A4	1214.0104	RES	1/4W/C/FLM 5%		100K
R6203	4B5	1214.0104	RES	1/4W/C/FLM 5%		100K
R6204	4B3	1214.0181	RES	1/4W C FLM 5%		180
R6205	4B4	1214.0103	RES	1/4W C FLM 5%		10K
R6206	4C3	1214.0181	RES	1/4W C FLM 5%		180
R6207	4B4	1214.0104	RES	1/4W/C/FLM 5%		100K
R6208	4C4	1214.0304	RES	1/4W C FLM 5%		300K
R6209	4D4	1214.0181	RES	1/4W C FLM 5%		180
R6210	4D4	1214.0104	RES	1/4W/C/FLM 5%		100K
R6211	4B2	1214.0102	RES	1/4W C FLM 5%		1K
R6212	4C4	1214.0103	RES	1/4W C FLM 5%		10K
R6301	4E2	1214.0102	RES	1/4W C FLM 5%		1K
R6302	4D4	1214.0181	RES	1/4W C FLM 5%		180
R6303	4D4	1214.0104	RES	1/4W/C/FLM 5%		100K
R6304	4E5	1214.0104	RES	1/4W/C/FLM 5%		100K
R6305	4E3	1214.0181	RES	1/4W C FLM 5%		180
R6306	4C2	1214.0472	RES	1/4W C FLM 5%		4.7K
R6307	4F2	1214.0472	RES	1/4W C FLM 5%		4.7K
R6308	4E4	1214.0103	RES	1/4W C FLM 5%		10K
R6309	4F4	1214.0103	RES	1/4W C FLM 5%		10K
R6310	4E3	1214.0181	RES	1/4W C FLM 5%		180
R6311	4E4	1214.0104	RES	1/4W/C/FLM 5%		100K
R6312	4F4	1214.0304	RES	1/4W C FLM 5%		300K
R6313	4G4	1214.0181	RES	1/4W C FLM 5%		180
R6314	4F4	1214.0104	RES	1/4W/C/FLM 5%		100K
R6601	1E2	1214.0272	RES	1/4W C FLM 5%		2.7K
R6602	1D2	1214.0272	RES	1/4W C FLM 5%		2.7K
R7101	3E5	1136.5230	RES	1/8W M FLM 1%		523
R7102	3F5	1136.5230	RES	1/8W M FLM 1%		523
R7103	3E3	1136.7870	RES	1/8W M FLM 1%		787
R7104	3F3	1136.7870	RES	1/8W M FLM 1%		787
R7105	3F3	1136.1002	RES	1/8W M FLM 1%		10.0K
R7106	3E2	1136.1002	RES	1/8W M FLM 1%		10.0K
R72	4A5,4B5,4C5	1984.9472	RES	NET SIP 5% B		9 X 4.7K
R73	4D5,4E5,4F5	1984.9472	RES	NET SIP 5% B		9 X 4.7K
R7400	4E10	1214.0229	RES	1/4W C FLM 5%		2.2
R7401	4D6	1214.0472	RES	1/4W C FLM 5%		4.7K

REPLACEABLE ELECTRICAL PARTS LIST: 9PHA.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R7402	4D7	1214.0103	RES 1/4W C FLM 5%	10K
R7403	4D9	1214.0104	RES 1/4W/C/FLM 5%	100K
R7501	2E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R7601	1F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R7602	1F4	1214.0272	RES 1/4W C FLM 5%	2.7K
R8101	3C4	1214.0303	RES 1/4W C FLM 5%	30K
R8102	3D4	1214.0303	RES 1/4W C FLM 5%	30K
R8103	3D4	1214.0103	RES 1/4W C FLM 5%	10K
R8104	3C5	1214.0103	RES 1/4W C FLM 5%	10K
R8201	4C9	1136.4122	RES 1/8W M FLM 1%	41.2K
R8202	4C9	1136.1002	RES 1/8W M FLM 1%	10.0K
R8203	4C9	1136.7681	RES 1/8W M FLM 1%	7.68K
R8501	4A8	1214.0472	RES 1/4W C FLM 5%	4.7K
R8502	4A10	1214.0272	RES 1/4W C FLM 5%	2.7K
R8503	4B9	1139.5001	RES 1/8W M FLM .1%	5.00K
R8504	4B10	1139.2001	RES 1/8W M FLM .1%	2.00K
R8601	1F8	1214.0272	RES 1/4W C FLM 5%	2.7K
R8602	1E8	1214.0272	RES 1/4W C FLM 5%	2.7K
R9201	4C9	4412.0202	POT TRIM PC ENC	2K
R9401	4B9	1136.1002	RES 1/8W M FLM 1%	10.0K
R9402	4E9	1136.1002	RES 1/8W M FLM 1%	10.0K
R9501	4E10	1214.0103	RES 1/4W C FLM 5%	10K
R9601	1F9	1214.0272	RES 1/4W C FLM 5%	2.7K
U21	2C9	3412.5532	OP AMP DUAL	5532
U22	2C6	3411.5534	OP AMP SINGLE	5534A
U231	2D4	3411.5534	OP AMP SINGLE	5534A
U232	2A4	3411.5534	OP AMP SINGLE	5534A
U32	2B6	3412.5532	OP AMP DUAL	5532
U411	3E6	3422.0393	COMPARATOR DUAL	LM393
U412	2D8	3411.5534	OP AMP SINGLE	5534A
U52	4B2,4E2	3412.0082	OP AMP DUAL	MC34082
U56	1C4	3630.0001	OPTO-ISOLATOR	H11AA1
U61	3C3,3D3,3E3	3424.0339	COMPARATOR QUAD	LM339
U721	4A4,4B4	3422.0319	COMPARATOR HI-SPEED	LM319
U722	4C4	3422.0319	COMPARATOR HI-SPEED	LM319
U731	4D4,4E4	3422.0319	COMPARATOR HI-SPEED	LM319
U732	4E4,4F4	3422.0319	COMPARATOR HI-SPEED	LM319
U74	4D6,4F6	3324.0074	FLIP-FLOP 2X D	74HCT74
U81	3C5,3D5	3324.0074	FLIP-FLOP 2X D	74HCT74
U82	4C10	3441.0654	CONVERTER VOLT TO FREQ	AD654J
U831	4A6,4C6	3324.0074	FLIP-FLOP 2X D	74HCT74
U832	4F7	3313.0251	MULTIPLEXER TRI-ST	74LS251
U841	4C7	3313.0251	MULTIPLEXER TRI-ST	74LS251
U842	4D5,4D8,4D9	3323.0086	GATE 4-IN EXCL OR	74HC86
U91	3D8	3313.0244	BUFFER 8X TRI-STATE	74LS244
U92	2E2	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U93	4G6	3324.0074	FLIP-FLOP 2X D	74HCT74
U94	4C8,4E8	3324.0074	FLIP-FLOP 2X D	74HCT74
U95	4B9,4E10	3422.0393	COMPARATOR DUAL	LM393


LEVEL FREQ
MEASURE.
(J231)
R5701
"WF RECT BAL"
TP6606
"WF AVG"
R6701
"WFAVG OFFSET"
LEVEL FREQ
MEASUREMENT
(J621)
R7701
"WF CAL"
TP8503
"WF CAL"
TP8605
"WFQPK"
R8701
"WFQPK OFFSET"



WOW & FLUTTER ANALYZER OPTION (9W&F.1000)

W&F-1, WOW & FLUTTER OPTION

Input Filter & Frequency Discriminator <1>

MAINSIG enters the wow & flutter option through J36-6. JFET Q3601 switches the signal off if wow & flutter is not selected to prevent the possibility of interference with other analyzer modes. Q3601 is driven from the output of one of the comparators inside U56 which is controlled by the presence of any bit at J36-2, J36-3, or J36-4. See TABLE WF1.1 for more information. The demodulated wow & flutter output signal is switched through JFET Q6501 and J75-6 to the LVF module for front panel monitoring.

MAINSIG is applied to noise limiting bandpass filters. U17A, U17B, and related components comprise a 2.8-3.3 kHz bandpass for use with "Low-Band" test signal frequencies of 3.0 kHz or 3.15 kHz. U15A, U15B, and related components comprise a 4.0-20 kHz bandpass for use with "High-Band" test signal frequencies between approximately 8-14 kHz. JFET Q1501 selects which filter is used.

U12, U13, and U14 comprise a frequency-to-voltage converter. When the input signal crosses zero with positive slope, U14-1 goes low, supplying current through R2402 and Q2402 to the run-up integrator U13A and C2303. When the input crosses zero again in the opposite direction, U14-1 goes high stopping the flow of current into the integrator. At this time U14-14 goes high enabling the transconductance amplifier U12 to sample the voltage the integrator achieved during the 1/2-cycle time interval. D2401, R2403, and C2401 function as a delay circuit causing U14-13 to go low after approximately 10 usec. This causes the discharge JFET, Q2401, to turn on, and resets the integrator voltage to zero so that the cycle can repeat itself on the next positive zero crossing. R2406, R2405, and R2404 impart a slight amount of hysteresis and positive feedback to minimize noise susceptibility.

The output dc voltage at U13B-7 is directly proportional to the 1/2-cycle time interval of the input signal. Because frequency is proportional to the reciprocal of period the ac component of this voltage will be proportional to wow & flutter with negligible error for values up to about 5%. The typical dc voltage at this point with a 3150 Hz test frequency is about +9.3 V.

Weighting Filter Selection <2>

The raw discriminated wow & flutter signal is coupled in amplifier U11A through C2201 and diode clamps D2101 and D2102. The diodes assist in rapid recovery during test frequency changes or run-up tests. U11A is operated with +24 dB (x16) of gain. Its output passes through a 5 kHz lowpass filter composed of U42A and related components.

U11B and related components comprise a 200 Hz low-pass filter for unweighted measurements. U43B and related components form the standard wow & flutter weighting filter, which has a bandpass response peaking at 4 Hz. U42B and related components comprise a 200 Hz highpass filter required for scrape flutter measurements.

CMOS switch U35 provides response selection and is buffered by U45B. U45A provides final amplification and low frequency response compensation before being applied to the detector stages and routed through Q6501 on <1>. R5701 adjusts the dc offset in the WFsig. TABLE WF1.1 gives the switching logic for the CMOS switch.

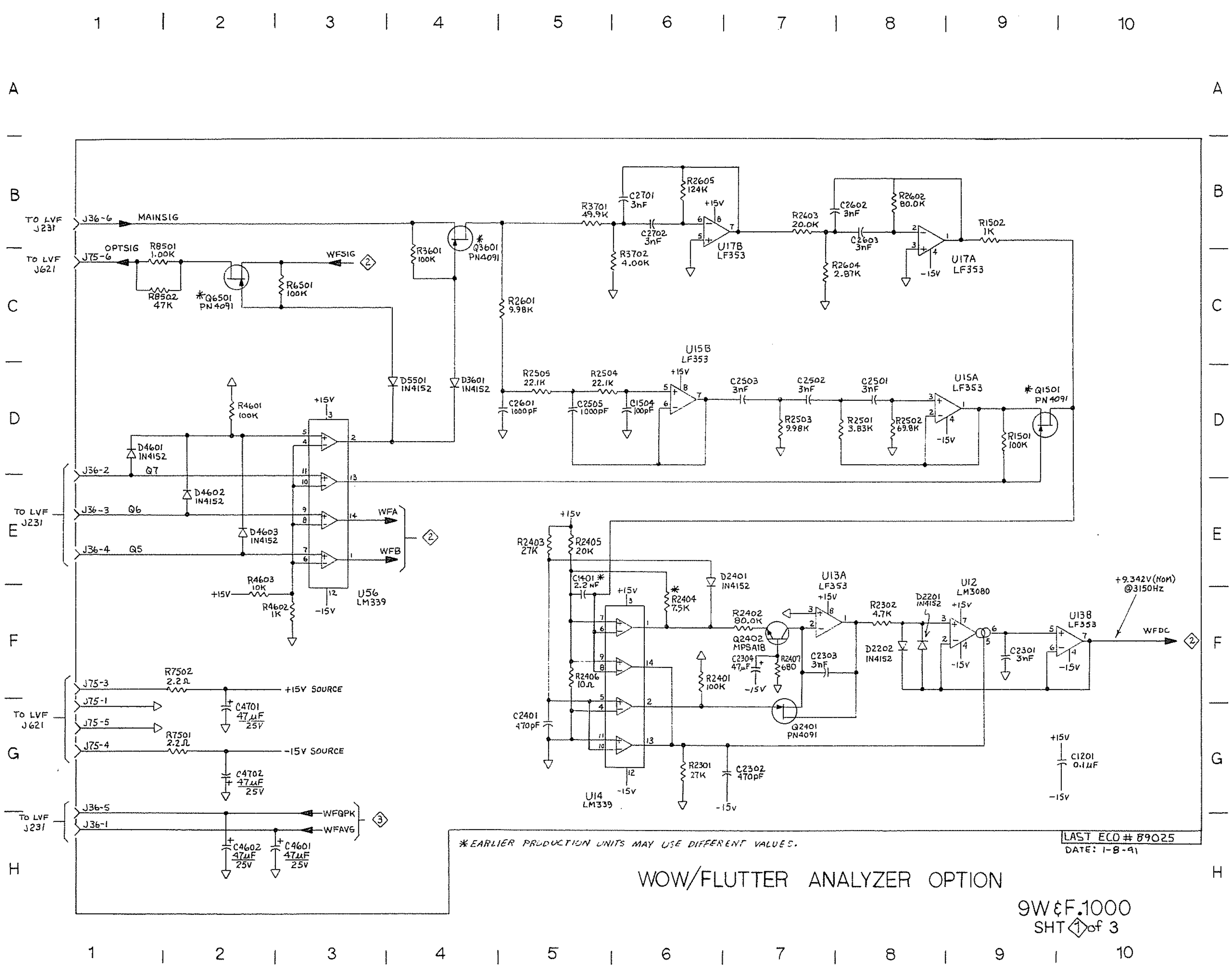
TABLE WF1.1
WOW & FLUTTER MODE SELECTION

RESPONSE	J36-2	J36-3	J36-4	U35-A	U35-B
Off	0	0	0	0	0
Weighted-LB	0	1	1	1	1
UnWtd-LB	0	1	0	1	0
Weighted-HB	1	1	1	1	1
UnWtd-HB	1	1	0	1	0
Wide-HB	1	0	1	0	1
Scrape-HB	1	0	0	0	0

Detectors <3>

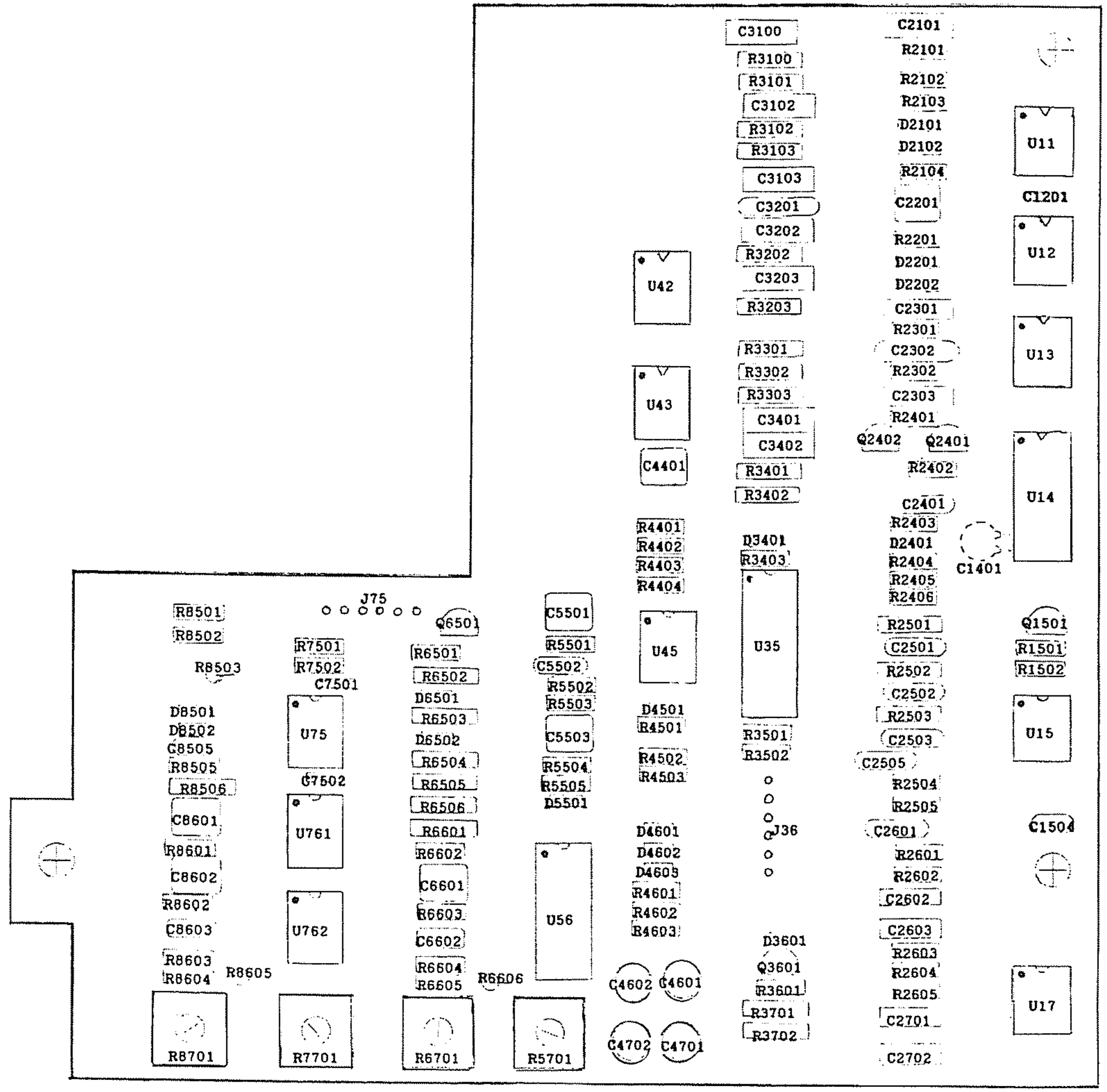
The wow & flutter analyzer detectors are shown on schematic <3>. Only one range is provided to optimize measurement speed. Autoranging with multiple ranges would impart exceptionally long time delays because wow & flutter can contain significant components as low as 0.5 Hz. U75B and U761B form a precision full-wave rectifier. R7701 adjusts detector calibration. NAB detection is really average detection so the full-wave rectified signal is passed directly through a lowpass filter, U762B, to obtain the detected dc output WFAVG. The JIS detection mode also uses the average detector but the software processes the readings to impart a long integration time constant. U75A and U761A comprise a quasi-peak detector with the ballistics required for wow & flutter measurements to IEC and DIN standards. The output of U761A is filtered through lowpass U762A and becomes the detected dc output WFQPK. R6701 and R8701 adjust for the offset error terms in their respective detector outputs. These dc outputs are routed to the LVF module through J36-1 and J36-5.

The basic detector sensitivity is approximately 3.0 Vdc for a 1% peak flutter at 3150 Hz. This sensitivity varies in inverse proportion to the test signal frequency. Thus, for example, the sensitivity becomes 0.75 Vdc for a 1% peak flutter with a test signal frequency of 12.6 kHz. The displayed wow and flutter measurement is corrected by the System One software based upon the actual measured test frequency value.

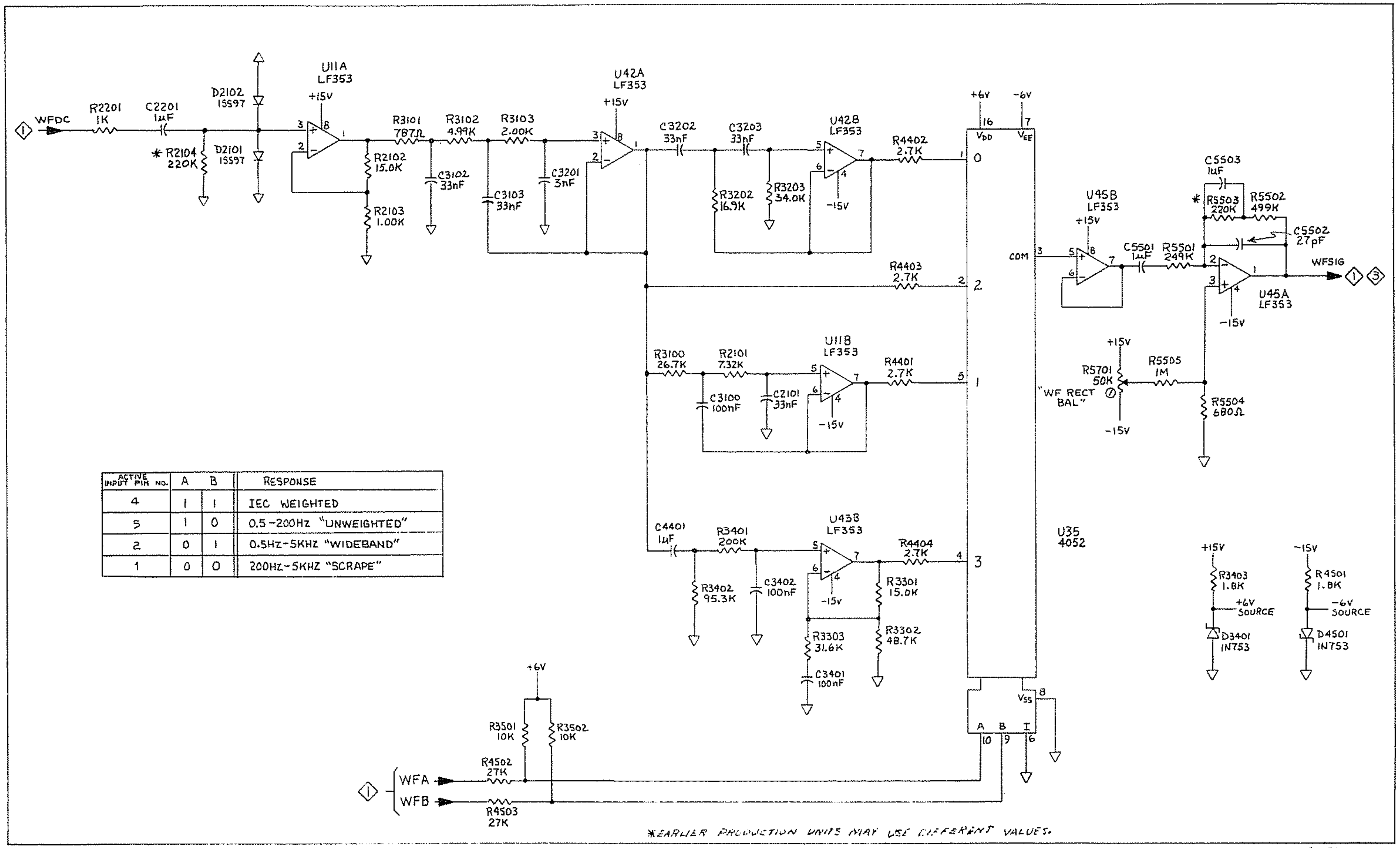


WOW/FLUTTER ANALYZER OPTION

9W&F.1000
SHT 1 of 3



WOW & FLUTTER ANALYZER OPTION (9W&F.1000)

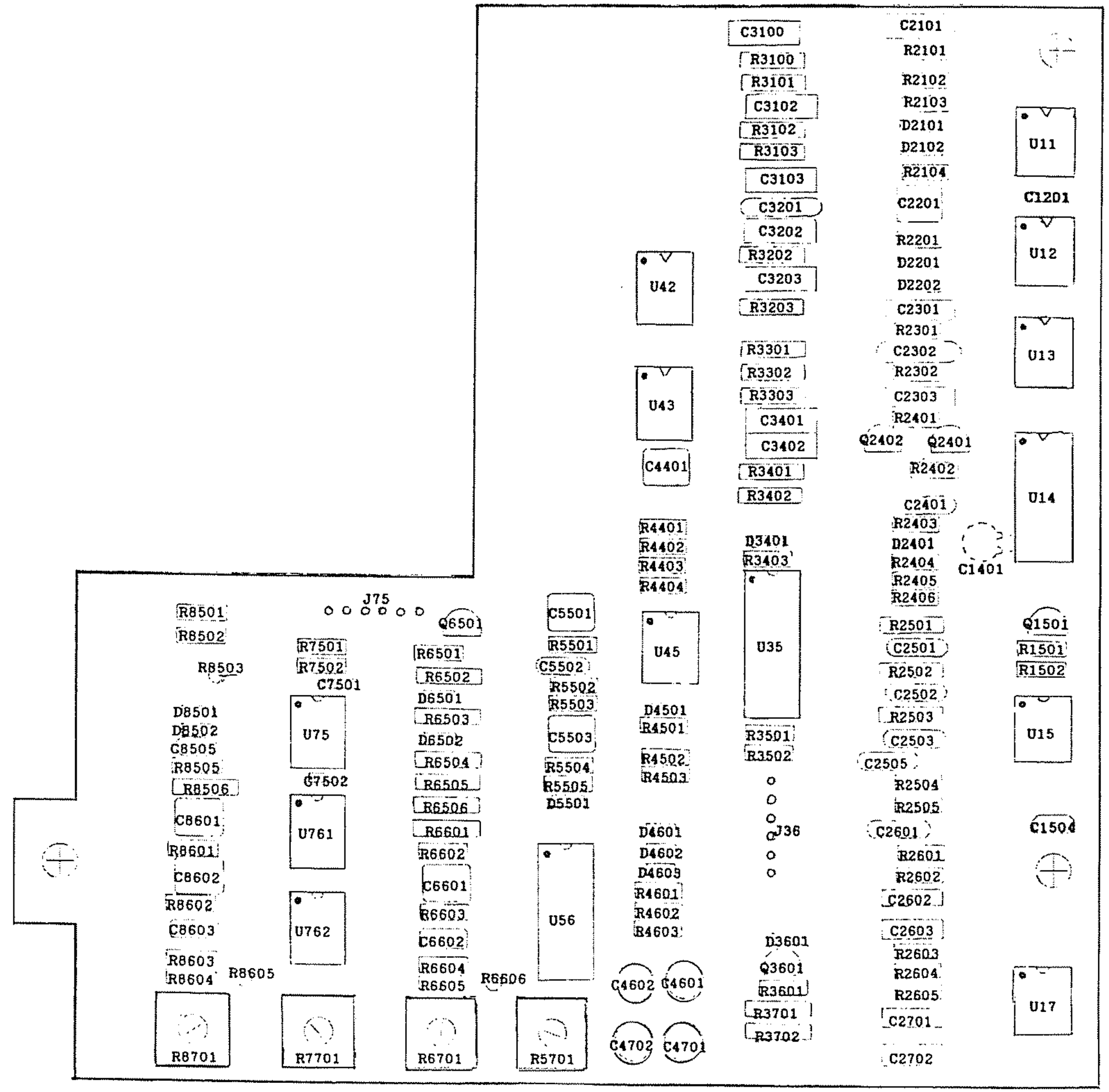


ACTIVE INPUT PIN NO.	A	B	RESPONSE
4	1	1	IEC WEIGHTED
5	1	0	0.5-200Hz "UNWEIGHTED"
2	0	1	0.5Hz-5KHz "WIDEBAND"
1	0	0	200Hz-5KHz "SCRAPE"

*EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.

DATE: 1-8-91

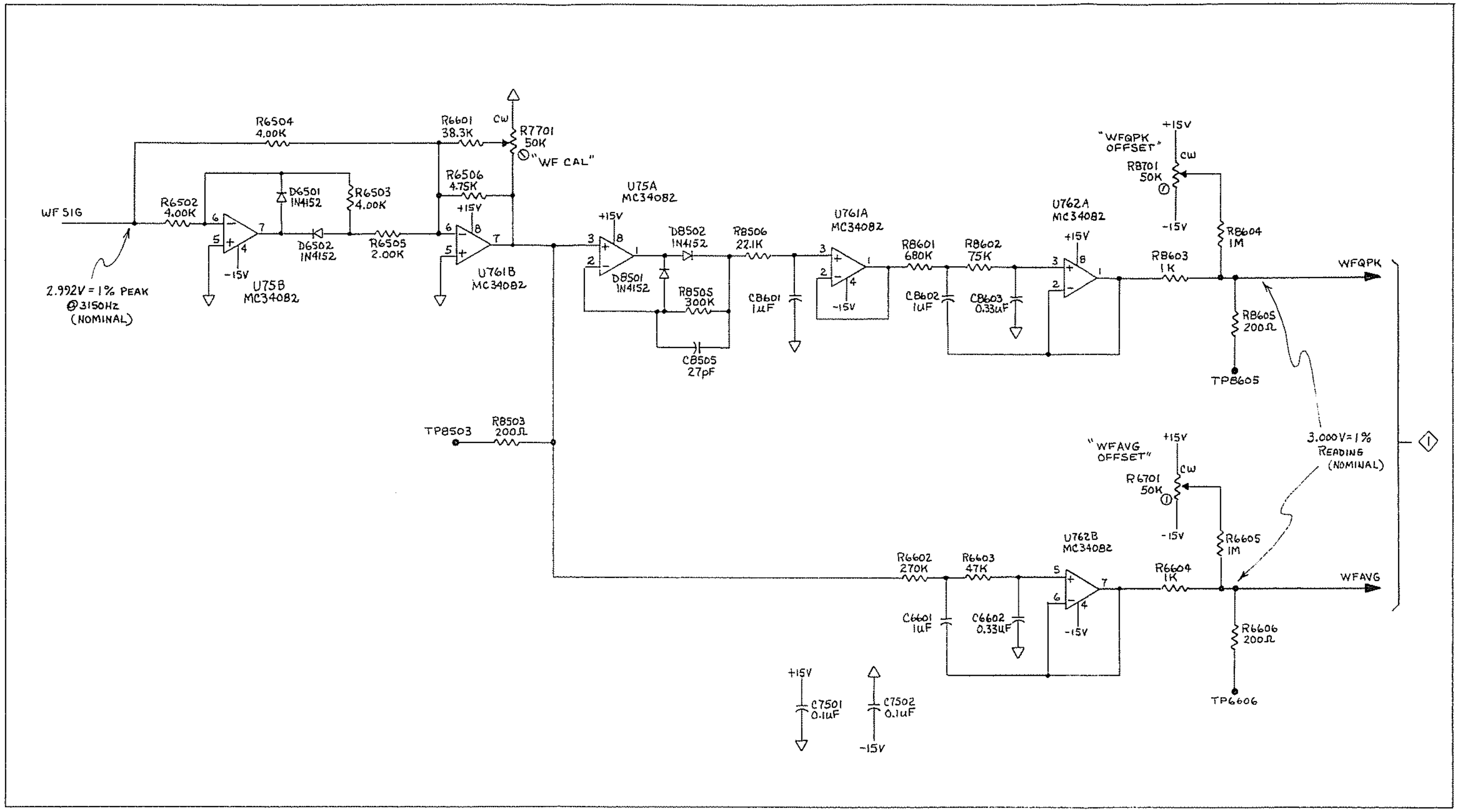
9W&F.1000
SHT 2 of 3



WOW & FLUTTER ANALYZER OPTION (9W&F.1000)

1 2 3 4 5 6 7 8 9 10

A B C D E F G H



DATE: 1-8-91

9W&F.1000
SHT 3 of 3

1 2 3 4 5 6 7 8 9 10

A B C D E F G H

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1201	1G10	2172.0104	CAP CERAM 100V 20%	.1uF
C1401	1F5	2172.0222	CAP CERAM 100V 20%	.0022uF
C1504	1D6	2296.0101	CAP MICA 500V 1%	100pF
C2101	2D6	2675.0333	CAP POLYC 100V 2%	.033uF
C2201	2B1	2454.0105	CAP POLYE 50V 5%	1uF
C2301	1F9	2296.0302	CAP MICA 500V 1%	.003uF
C2302	1G7	2296.0471	CAP MICA 500V 1%	470pF
C2303	1F7	2296.0302	CAP MICA 500V 1%	.003uF
C2304	1F7	2932.0476	CAP AL-EL 25V 20%	47uF
C2401	1G5	2296.0471	CAP MICA 500V 1%	470pF
C2501	1D8	2296.0302	CAP MICA 500V 1%	.003uF
C2502	1D7	2296.0302	CAP MICA 500V 1%	.003uF
C2503	1D7	2296.0302	CAP MICA 500V 1%	.003uF
C2505	1D5	2296.0102	CAP MICA 500V 1%	.001uF
C2601	1D5	2296.0102	CAP MICA 500V 1%	.001uF
C2602	1B7	2296.0302	CAP MICA 500V 1%	.003uF
C2603	1B8	2296.0302	CAP MICA 500V 1%	.003uF
C2701	1B6	2296.0302	CAP MICA 500V 1%	.003uF
C2702	1B6	2296.0302	CAP MICA 500V 1%	.003uF
C3100	2D5	2675.0104	CAP POLYC 100V 2%	.1uF
C3102	2C3	2675.0333	CAP POLYC 100V 2%	.033uF
C3103	2C4	2675.0333	CAP POLYC 100V 2%	.033uF
C3201	2C4	2296.0302	CAP MICA 500V 1%	.003uF
C3202	2C5	2675.0333	CAP POLYC 100V 2%	.033uF
C3203	2C6	2675.0333	CAP POLYC 100V 2%	.033uF
C3401	2F6	2675.0104	CAP POLYC 100V 2%	.1uF
C3402	2F6	2675.0104	CAP POLYC 100V 2%	.1uF
C4401	2E5	2454.0105	CAP POLYE 50V 5%	1uF
C4601	1H2	2932.0476	CAP AL-EL 25V 20%	47uF
C4602	1H2	2932.0476	CAP AL-EL 25V 20%	47uF
C4701	1G2	2932.0476	CAP AL-EL 25V 20%	47uF
C4702	1G2	2932.0476	CAP AL-EL 25V 20%	47uF
C5501	2C9	2454.0105	CAP POLYE 50V 5%	1uF
C5502	2C9	2294.0270	CAP MICA 500V 5%	27pF
C5503	2C9	2454.0105	CAP POLYE 50V 5%	1uF
C6601	3F7	2454.0105	CAP POLYE 50V 5%	1uF
C6602	3F8	2454.0334	CAP POLYE 50V 5%	.33uF
C7501	3F6	2172.0104	CAP CERAM 100V 20%	.1uF
C7502	3F7	2172.0104	CAP CERAM 100V 20%	.1uF
C8505	3D5	2294.0270	CAP MICA 500V 5%	27pF
C8601	3C6	2454.0105	CAP POLYE 50V 5%	1uF
C8602	3C7	2454.0105	CAP POLYE 50V 5%	1uF
C8603	3C7	2454.0334	CAP POLYE 50V 5%	.33uF
D2101	2C2	3110.4152	DIODE SIGNAL	4152
D2102	2B2	3110.4152	DIODE SIGNAL	4152
D2201	1F8	3110.4152	DIODE SIGNAL	4152
D2202	1F8	3110.4152	DIODE SIGNAL	4152
D2401	1E6	3110.4152	DIODE SIGNAL	4152
D3401	2F9	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
D3601	1D4	3110.4152	DIODE SIGNAL	4152
D4501	2F10	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753

REPLACEABLE ELECTRICAL PARTS LIST: 9W&F.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
D4601	1D1	3110.4152	DIODE SIGNAL	4152
D4602	1E2	3110.4152	DIODE SIGNAL	4152
D4603	1E2	3110.4152	DIODE SIGNAL	4152
D5501	1D4	3110.4152	DIODE SIGNAL	4152
D6501	3C2	3110.4152	DIODE SIGNAL	4152
D6502	3C3	3110.4152	DIODE SIGNAL	4152
D8501	3C5	3110.4152	DIODE SIGNAL	4152
D8502	3C5	3110.4152	DIODE SIGNAL	4152
J36	1B1,1E1,1H1	4221.1006	JACK PC .1	6 PIN
J75	1C1,1F1	4221.1006	JACK PC .1	6 PIN
P36	---	4221.0036.2	PLUG PC .1 X1.03	36 PIN
P75	---	4221.0036.2	PLUG PC .1 X1.03	36 PIN
Q1501	1D9	3214.4091	XSTR FET TO92	PN4091
Q2401	1G7	3214.4091	XSTR FET TO92	PN4091
Q2402	1F7	3211.0018	XSTR NPN TO92	MPSA18
Q3601	1B4	3214.4091	XSTR FET TO92	PN4091
Q6501	1C2	3214.4091	XSTR FET TO92	PN4091
R1501	1D9	1214.0104	RES 1/4W/C/FLM 5%	100K
R1502	1B9	1214.0102	RES 1/4W C FLM 5%	1K
R2101	2D6	1136.7321	RES 1/8W M FLM 1%	7.32K
R2102	2C3	1139.1502	RES 1/8W M FLM .1%	15.0K
R2103	2C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R2104	2C2	1136.4993	RES 1/8W M FLM 1%	499K
R2201	2B1	1214.0102	RES 1/4W C FLM 5%	1K
R2301	1G6	1214.0273	RES 1/4W C FLM 5%	27K
R2302	1F8	1214.0472	RES 1/4W C FLM 5%	4.7K
R2401	1F6	1214.0104	RES 1/4W/C/FLM 5%	100K
R2402	1F7	1139.8002	RES 1/8W M FLM .1%	80.0K
R2403	1E5	1214.0273	RES 1/4W C FLM 5%	27K
R2404	1F6	1214.0752	RES 1/4W C FLM 5%	7.5K
R2405	1E5	1214.0203	RES 1/4W C FLM 5%	20K
R2406	1F5	1214.0100	RES 1/4W C FLM 5%	10
R2407	1F7	1214.0681	RES 1/4W C FLM 5%	680
R2501	1D8	1136.3831	RES 1/8W M FLM 1%	3.83K
R2502	1D8	1136.6982	RES 1/8W M FLM 1%	69.8K
R2503	1D7	1139.9981	RES 1/8W M FLM .1%	9.98K
R2504	1D5	1136.2212	RES 1/8W M FLM 1%	22.1K
R2505	1D5	1136.2212	RES 1/8W M FLM 1%	22.1K
R2601	1C5	1139.9981	RES 1/8W M FLM .1%	9.98K
R2602	1B8	1139.8002	RES 1/8W M FLM .1%	80.0K
R2603	1B7	1139.2002	RES 1/8W M FLM .1%	20.0K
R2604	1C7	1136.2871	RES 1/8W M FLM 1%	2.87K
R2605	1B6	1136.1243	RES 1/8W M FLM 1%	124K
R3100	2D5	1136.2672	RES 1/8W M FLM 1%	26.7K
R3101	2C3	1136.7870	RES 1/8W M FLM 1%	787
R3102	2C4	1136.4991	RES 1/8W M FLM 1%	4.99K
R3103	2C4	1139.2001	RES 1/8W M FLM .1%	2.00K
R3202	2C6	1136.1692	RES 1/8W M FLM 1%	16.9K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R3203	2C6	1136.3402	RES 1/8W M FLM 1%	34.0K
R3301	2F7	1139.1502	RES 1/8W M FLM .1%	15.0K
R3302	2F7	1136.4872	RES 1/8W M FLM 1%	48.7K
R3303	2F6	1136.3162	RES 1/8W M FLM 1%	31.6K
R3401	2E6	1136.2003	RES 1/8W M FLM 1%	200K
R3402	2F5	1136.9532	RES 1/8W M FLM 1%	95.3K
R3403	2F9	1214.0182	RES 1/4W C FLM 5%	1.8K
R3501	2G4	1214.0103	RES 1/4W C FLM 5%	10K
R3502	2G4	1214.0103	RES 1/4W C FLM 5%	10K
R3601	1C4	1214.0104	RES 1/4W/C/FLM 5%	100K
R3701	1B5	1136.4992	RES 1/8W M FLM 1%	49.9K
R3702	1C6	1139.4001	RES 1/8W M FLM .1%	4.00K
R4401	2D7	1214.0272	RES 1/4W C FLM 5%	2.7K
R4402	2C7	1214.0272	RES 1/4W C FLM 5%	2.7K
R4403	2D7	1214.0272	RES 1/4W C FLM 5%	2.7K
R4404	2F7	1214.0272	RES 1/4W C FLM 5%	2.7K
R4501	2F10	1214.0182	RES 1/4W C FLM 5%	1.8K
R4502	2G4	1214.0273	RES 1/4W C FLM 5%	27K
R4503	2G4	1214.0273	RES 1/4W C FLM 5%	27K
R4601	1D2	1214.0104	RES 1/4W/C/FLM 5%	100K
R4602	1F3	1214.0102	RES 1/4W C FLM 5%	1K
R4603	1F2	1214.0103	RES 1/4W C FLM 5%	10K
R5501	2C9	1136.2493	RES 1/8W M FLM 1%	249K
R5502	2C10	1136.4993	RES 1/8W M FLM 1%	499K
R5503	2C9	1214.0224	RES 1/4W M FLM 5%	220K
R5504	2D9	1214.0681	RES 1/4W C FLM 5%	680
R5505	2D9	1214.0105	RES 1/4W C FLM 5%	1M
R5701	2D9	4412.0503	POT TRIM PC ENC	50K
R6501	1C3	1214.0104	RES 1/4W/C/FLM 5%	100K
R6502	3C2	1139.4001	RES 1/8W M FLM .1%	4.00K
R6503	3C3	1139.4001	RES 1/8W M FLM .1%	4.00K
R6504	3B2	1139.4001	RES 1/8W M FLM .1%	4.00K
R6505	3C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R6506	3C4	1136.4751	RES 1/8W M FLM 1%	4.75K
R6601	3B4	1136.3832	RES 1/8W M FLM 1%	38.3K
R6602	3E7	1214.0274	RES 1/4W C FLM 5%	270K
R6603	3E7	1214.0473	RES 1/4W C FLM 5%	47K
R6604	3E9	1214.0102	RES 1/4W C FLM 5%	1K
R6605	3E9	1214.0105	RES 1/4W C FLM 5%	1M
R6606	3F9	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R6701	3E9	4412.0503	POT TRIM PC ENC	50K
R7501	1G2	1214.0229	RES 1/4W C FLM 5%	2.2
R7502	1F2	1214.0229	RES 1/4W C FLM 5%	2.2
R7701	3B4	4412.0503	POT TRIM PC ENC	50K
R8501	1C1	1139.1001	RES 1/8W M FLM .1%	1.00K
R8502	1C1	1214.0473	RES 1/4W C FLM 5%	47K
R8503	3D4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R8505	3C5	1214.0304	RES 1/4W C FLM 5%	300K
R8506	3C6	1136.2212	RES 1/8W M FLM 1%	22.1K
R8601	3C7	1214.0684	RES 1/4W C FLM 5%	680K
R8602	3C7	1214.0753	RES 1/4W C FLM 5%	75K
R8603	3C9	1214.0102	RES 1/4W C FLM 5%	1K

REPLACEABLE ELECTRICAL PARTS LIST: 9W&F.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R8604	3C9	1214.0105	RES 1/4W C FLM 5%	1M
R8605	3D9	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R8701	3C9	4412.0503	POT TRIM PC ENC	50K
U11	2B3,2D6	3412.0353	OP AMP DUAL	TL072/LF353
U12	1F9	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U13	1F7,1F10	3412.0353	OP AMP DUAL	TL072/LF353
U14	1F6	3424.0339	COMPARATOR QUAD	LM339
U15	1D6,1D8	3412.0353	OP AMP DUAL	TL072/LF353
U17	1B6,1B8	3412.0353	OP AMP DUAL	TL072/LF353
U35	2C8	3321.4052	MULTIPLEX 4X DIFF	4052
U42	2C5,2C6	3412.0353	OP AMP DUAL	TL072/LF353
U43	2F6	3412.0353	OP AMP DUAL	TL072/LF353
U45	2C8,2C9	3412.0353	OP AMP DUAL	TL072/LF353
U56	1D3	3424.0339	COMPARATOR QUAD	LM339
U75	3C2,3C5	3412.0082	OP AMP DUAL	MC34082
U761	3C4,3C6	3412.0082	OP AMP DUAL	MC34082
U762	3C8,3E8	3412.0082	OP AMP DUAL	MC34082

DIS-2 DISTORTION MEASUREMENT MODULE

DIS-2, DISTORTION MEASUREMENT MODULE

Logic Interface <1>

The logic on the DIS-2 module performs three functions: tuning of the bandpass/bandreject filter, setting of mode control bits, and buffering data between the control microprocessor located on the LVF-2 module and the host computer.

Address and data information from the host computer enter the module via the 40-pin ribbon cable P28. Data is buffered by U31 to form the "D" bus. This bus drives four octal data latches and two 4-bit dual port RAMs. The operation of these devices is identical to that of the RAMs on the LVF-2 module. They contain the input level meter reading (the "LEVEL" display on the LVF panel) and the current frequency sent to the notch filter by the LVF-2 microprocessor. The module address (normally 1, and always 1 higher than the corresponding LVF-2 board) is recognized by 4-bit comparator U71. Jumper R7101 is removed only for special applications requiring DIS module address 5. Its output is used to drive the /ATT line via Q7101 and to enable address decoder U51. U51 decodes the address information to provide write and read strobes for the RAM and the data latches. U61B further decodes the write strobes into individual addresses for the data latches on the D bus.

Information from the control microprocessor located on the LVF-2 module enters the DIS-2 board via connector P94. The data is sent on the C bus while address information is provided by B0 and B1 and strobe lines STATUS and WRDIS. These are decoded by U75A to provide write strobes for the data latches on the C bus. The dual port RAMs are also on the C bus and buffer communication between the microprocessor and the host computer.

The selectable bandpass-bandreject filter can be tuned by either the host computer or the LVF-2 microprocessor. The outputs from latch pairs U83-U85 and U93-U95 are wired in parallel, with the tri-state control pins driven by inverter U92B. The state of bit 7 in U41 determines which pair of latches is used to tune the filter. When this pin is low the host computer tunes the filter and when it is high the microprocessor tunes the filter. The setting of the notch loop compensation is handled in a similar way. Control bits are sent by the host via U41 and by the LVF-2 microprocessor via U84. U72 provides the source selection based on the state of U41 bit 6.

Signal Switching & Level Voltmeter <2>

Schematic <2> contains the input and output signal switching for the DIS-2 module along with the LEVEL voltmeter. The preamplified signal from the selected A or B channel input (MAINSIG) enters the module through P16-7 and is routed through jumper R1601 connected between pins 2 and 4 of socket J15. This socket is reserved for possible future use. All units will normally be shipped with jumper R1601.

MAINSIG is then routed to the module bypass relay K25 and to buffer U242A through R2501. K25 returns MAINSIG directly back to the LVF-2 module through P16-3 as FUNCSIG whenever the LVF Reading Mode is AMPLITUDE or DUAL CHANNEL. Relay K25 is energized for all other measurement modes.

From relay K25, MAINSIG is routed to the intermodulation distortion analyzer socket J17-7 to become IMAIN. The output from the IMD analyzer option (J24-8) is routed to the tunable bandpass-bandreject filter as BPBRIN. R2402 bypasses J24 if the IMD analyzer option is not installed.

NOTE: R2402 must be removed if the IMD analyzer option is installed.

MUX U241 provides signal source selection for the LEVEL meter and the main frequency counter (on the LVF-2 module). The LEVEL meter measures the amplitude of MAINSIG in all measurement modes except CROSSTALK or DUAL CHANNEL. In these two modes the LEVEL meter measures ALTSIG which is the alternate or reference channel. This gives the analyzer the ability to simultaneously measure both the reading and reference of the opposite or alternate channel. Buffers U242A and U242B limit the maximum voltage drive to the CMOS MUX U241 during overranging transients to prevent latchup.

MUX U241 also selects the main frequency counter signal from four possible sources depending upon measurement mode. ALTSIG is routed to the counter when the measurement mode is CROSSTALK or DUAL CHANNEL. IMFREQ from J24-6 is used if the measurement mode is CCIF. The counter is connected to the output of the bandpass-bandreject filter (DISTSIG) if the measurement mode is BANDPASS, BANDREJECT, or

WOW & FLUTTER and the BPBR tuning mode is "FIXED" on the LVF panel. In all other modes the counter is connected to MAINSIG.

The selected LEVEL signal is fed through buffer U34A to highpass filter U34A which limits low frequency response below approximately 6 Hz. R3504 adjusts the dc offset of this buffer which feeds the RMS detector IC, U33. U33 has an integration time constant determined by C3301, C2204, C2205, and CMOS switch U23. R4505 trims the offset error term of the converter. D3401, R3401, and R3402 clamp the dc output voltage to provide rapid recovery from autoranging transients.

The output of the detector is filtered through the internal buffer integral of U33 to reduce the ac ripple content. The V-F converter, U32, converts the dc voltage to a frequency which is routed to the LVF-2 module for counting through P94-20. R4506 adjusts calibration of the V-F conversion and R2201 is factory selected to approximately center R4506. Replacement of U32 may also require changing R2201 to center adjustment R4506. The operation of U32 is otherwise identical to U341 on schematic <8> of the LVF-2 module.

The dc output from U33 pin 14 is also routed to J91-1 for use with the intermodulation distortion analyzer option, and to schematic <5> as VLVL for use in the notch filter control loops.

D2101 and D2102 provide low voltage supplies required by the CMOS switches on schematics <2> and <5>.

Bandpass/Bandreject Filter <3,4>

The bandpass-bandreject filter is a two stage, 4-pole, design with programmable center frequency control from 10 Hz to over 200 kHz. Schematic <3> contains the first stage and schematic <4> contains the second stage. Figure DIS2.1 shows a simplified diagram of the filter and is helpful in understanding its basic operation.

Each stage consists of a state variable topology containing four op-amps: two integrators, an inverter, and an amplifier stage. The four op-amp outputs provide all possible 2-pole minimum-phase filter responses. <3>-U46 and <4>-U49B are integrators whose outputs exhibit a bandpass response. <3>-U47 and <4>-U49A also function as integrators providing a low-pass output. <3>-U361 and <4>-U48 are inverters that complete the basic state variable loops. <3>-U362 and <4>-U38 sum the bandpass outputs (which are inverted polarity) with the respective inputs to obtain bandreject outputs. <3>-R3702 determines the Q of the first stage, while <4>-R4801 and <4>-R4802 determine the Q of the second stage. <3>-R2801 and <4>-R2802 (switched by relay K28) provide interstage feedback to optimize the filter response shape. This feedback path can be disabled when troubleshooting filter tuning problems by temporarily unsoldering one end of R2801.

NOTE: Certain aspects of this filter design are protected by US patent 4,563,652.

Relays <3>-K26 and <4>-K29 select bandpass or bandreject filter response. In the bandpass mode, both relays are energized cascading the bandpass output of the first stage with the bandpass output of the second stage. The output of <4>-K29 is coupled through a highpass filter composed of U39B, C3901, C3902, R3901, and R3902 to become DISTSIG which is returned to the LVF-2 module through relay K25 on schematic <2>. In the bandreject mode, relay K26 is off and cascades the bandreject output of the first stage with the bandreject output of the second stage. K29 also switches the polarity and magnitude of the interstage feedback and the Q of the second stage. This is done to independently optimize the response shapes of the bandpass and bandreject modes.

Filter tuning is accomplished in four decade bands by switching the integrator capacitors and varying the integrator resistors. The timing capacitors are switched by JFETs (for example Q5601 switches C6601 on schematic <3>) and both sections are ganged. Lines R1-R3 control the JFET switches with logical 0 being approximately -15 V and logical 1 being 0 V.

TABLE DIS2.1
BP/BR FILTER TUNING CAPACITOR SWITCHING

FREQUENCY BAND	R1	R2	R3	CAPACITANCE
10.00-204.775 Hz	-15	-15	0	333 nF + 330 pF
205.0-2047.75 Hz	-15	0	-15	33 nF + 330 pF
2.050-20.4775 kHz	0	-15	-15	3 nF + 330 pF
20.50-204.775 kHz	-15	-15	-15	330 pF

The JFET switching circuits are different in the two filter sections. Consider Q5602 on schematic <3> as an example of the first stage switching. Q5602 is switched through transistor Q5601 connected in the common base configuration. R5604 provides the bias current to saturate Q5601 when its emitter is pulled to -15 V by control line R1. R1602 and R1603 apply 1/2 of the ac signal across the JFET to its gate to linearize its resistance characteristic. The JFET on-resistance is typically less than <5 Ohms. R5601 provides a dc return path to keep the switched node of C6601 at 0 V.

On schematic <4>, consider the operation of JFET switch Q5801. The control voltage from R1 is directly applied to the gate through D6801. R5802 and R5803 provide the same linearization function described for the first stage. C4901, C5903, and C6904 decouple the three decade control lines to prevent high-frequency crosstalk.

Modules A86-A89 function as ganged 2.50 kOhm variable tuning resistors with programmable 13-bit resolution. Lines F3-F15 control the resistors with F15 = MSB and F3 = LSB. These control lines are TTL compatible, inverted logic, with logical 0 being high and logical 1 being low. TABLE DIS2.2 lists tuning resistor values and control bit patterns for selected frequencies in the lowest 10-200 Hz decade.

TABLE DIS2.2
BP/BR TUNING RESISTANCE VS FREQUENCY

F15-F3 (MSB-LSB)	MDAC RESISTANCE	FREQUENCY
0 000 000 000 000	2.500 kOhms	204.775 Hz
0 000 010 111 111	2.560 kOhms	200.00 Hz
0 111 111 111 111	5.000 kOhms	102.40 Hz
1 000 001 011 111	5.120 kOhms	100.00 Hz
1 011 111 111 111	10.00 kOhms	51.20 Hz
1 101 111 111 111	20.00 kOhms	25.60 Hz
1 110 011 001 011	24.98 kOhms	20.50 Hz
1 111 001 101 111	51.20 kOhms	10.00 Hz

Relay K28 provides an additional +12 dB gain step by switching the input resistance to <4>-U38. It also switches the interstage feedback (YSIG) resistance, R2802, to maintain constant filter shape in both gain states. K28 works in conjunction with the range amplifier on the LVF-2 module to provide 0 dB to +60 dB of gain, in 12 dB steps, to the bandpass-bandreject filter output signal. TABLE DIS2.3 shows the ranging logic for the BANDPASS and BANDREJECT modes only. It is slightly different than the AMPLITUDE mode logic because of the additional +12 dB gain state that permits a more sensitive 75 uV range.

The first stage of the filter also contains fine tuning and nulling circuits for use in the THD+N mode. These are driven by servo loops located on schematic <5> and cause the bandreject filter to precisely tune and null out the fundamental component. U26 is a transconductance amplifier that feeds a potion of the bandpass signal into the summing node of U362. This corrects for the effects of capacitor dissipation factor, op-amp bandwidth, and stray capacitance that prevent a perfect null of the notch output. R3602 converts the NULL control voltage into a current applied to pin 5 of U26. R2703, D2701, and D2702 pre-distort the input signal to U26 to compensate for its inherent non-linearity.

TABLE DIS2.3
K28 & LVF RANGE AMPLIFIER SWITCHING
BANDPASS/BANDREJECT MODES

BP/BR RANGE	K28	ATTEN	U742 A	U742 B	U742 C	GAIN
≥80 mV	Off	-48 dB	0	1	1	0 dB
20 mV	On	-48 dB	0	1	1	+12 dB
5 mV	On	-36 dB	1	0	0	+24 dB
1.2 mV	On	-24 dB	1	0	1	+36 dB
300 uV	On	-12 dB	1	1	0	+48 dB
75 uV	On	0 dB	1	1	1	+60 dB

C3501 provides phase compensation for the effects of op-amp finite gain at high frequencies. It is adjusted at high frequencies to maintain the null control loop within its range.

U37, Q2701, and related components form a variable gain stage that provides fine tuning of the state variable filter frequency. The output of the second integrator, LP1SIG, is coupled into U37 through the attenuator R3703 and R2707. The voltage gain of U37 is determined by R2706 and JFET Q2701, operated as a voltage-variable-resistor. Q2701 is selected for high pinch-off voltage to improve its linearity. R2705 feeds the variable signal back into the inverter stage summing node and effectively parallels R3601. R3704, R3705, and R3706 offset and scale the TUNE control voltage to the gate of JFET Q2701. As the TUNE voltage goes more positive, Q2701 becomes more conductive, increasing the gain of U37, thus increasing the frequency of the state variable filter. R2708 feeds a portion of the ac signal into the gate for the most linear JFET resistance characteristic.

Tuning/Nulling Control Loops <5>

In the THD+N mode it is necessary to continuously correct the notch frequency and nulling to maintain high degrees of fundamental rejection. Keeping in mind that the bandreject filter is actually a two stage filter, it is necessary to servo the first section only to obtain excellent fundamental rejection. The second stage can possess several percent tuning error without affecting the shape of the notch characteristic. The basic operation of the loops is to demodulate the residual fundamental content in the notch output and generate control voltages corresponding to the in-phase and 90 degree phase components. It can be shown that the in-phase component represents a null error and a 90 degree phase component represents a slight tuning error. Both must be minimized for optimum performance.

The servo loops derive their information from BP2SIG, which is the bandpass output of the second stage cascaded with the first stage bandreject output in the THD+N mode. BP2SIG contains fundamental information only with very little interference from signal harmonics that may be present. BP2SIG is fed into the inverting amplifier U43A, and a gain compensation circuit composed of U44, R4403, and R4404. The dc output VLVL from the LEVEL detector is converted into a control current through R4401 and Q4401 and modulates the transconductance amplifier U44. As the signal level increases within a given range, VLVL increases. This increases the bias current of U44 which cause more signal to be subtracted from the fixed gain path through R4405. This technique provides approximately constant servo loop gain as the signal varies over 6-7 dB within each input range. D4501 and D4502 clamp the input signal to U43A to minimize transients during tuning changes.

U43B amplifies the output of U43A and contains any fundamental tuning and nulling error information. U43B is connected to two synchronous demodulators consisting of inverted-mode switching transistors Q4201 and Q5401. Q4201 is driven by a squarewave derived from the BP1SIG which provides the 0 degree phase reference. Q5401 is driven by a square wave derived from LP1SIG which provides the 90 degree phase reference. Quad comparator U642 is used to process the input signals into the demodulator control squarewaves.

Q4201 functions with U43B, R4201, R4301, and R4302 to form the null-loop demodulator. U42B is an integrator amplifying the dc component demodulated from the output of U43B. U63 provides switching of the integration time constant to optimize loop speed as a function of fundamental frequency. COMPA and COMPB are the two control lines for this CMOS switch. When both lines are low the switch shorts out the integrator disabling the null loop for the normal bandpass and bandreject modes. Similarly, Q5401 functions with R5302, R5303, and R5304 to form the tune-loop demodulator. U641A is also an integrator with controllable time constants via U63; and is disabled if both COMPA and COMPB are low.

The outputs of the two loop integrators are fed into sample-hold circuits consisting of U53, U42A and U73, U641B respectively. The transconductance amplifiers U53 and U73 are pulsed on by the action of Q7401 and its related components every cycle of the fundamental to sample the respective loop error voltages across C5201 and C7302. This technique results in virtually no ripple in the NULL and TUNE control voltages that could cause THD products in the notch filter.

In the THD+N mode, the NULL and TUNE control voltages vary from approximately -8 to +8 Volts. In the BANDPASS and BANDREJECT modes, the control voltages are maintained near 0 V due to the shorting selection of U63. R5504 and R5505 adjust for op-amp offsets to minimize the fundamental content seen at TP4502 in the THD+N mode.

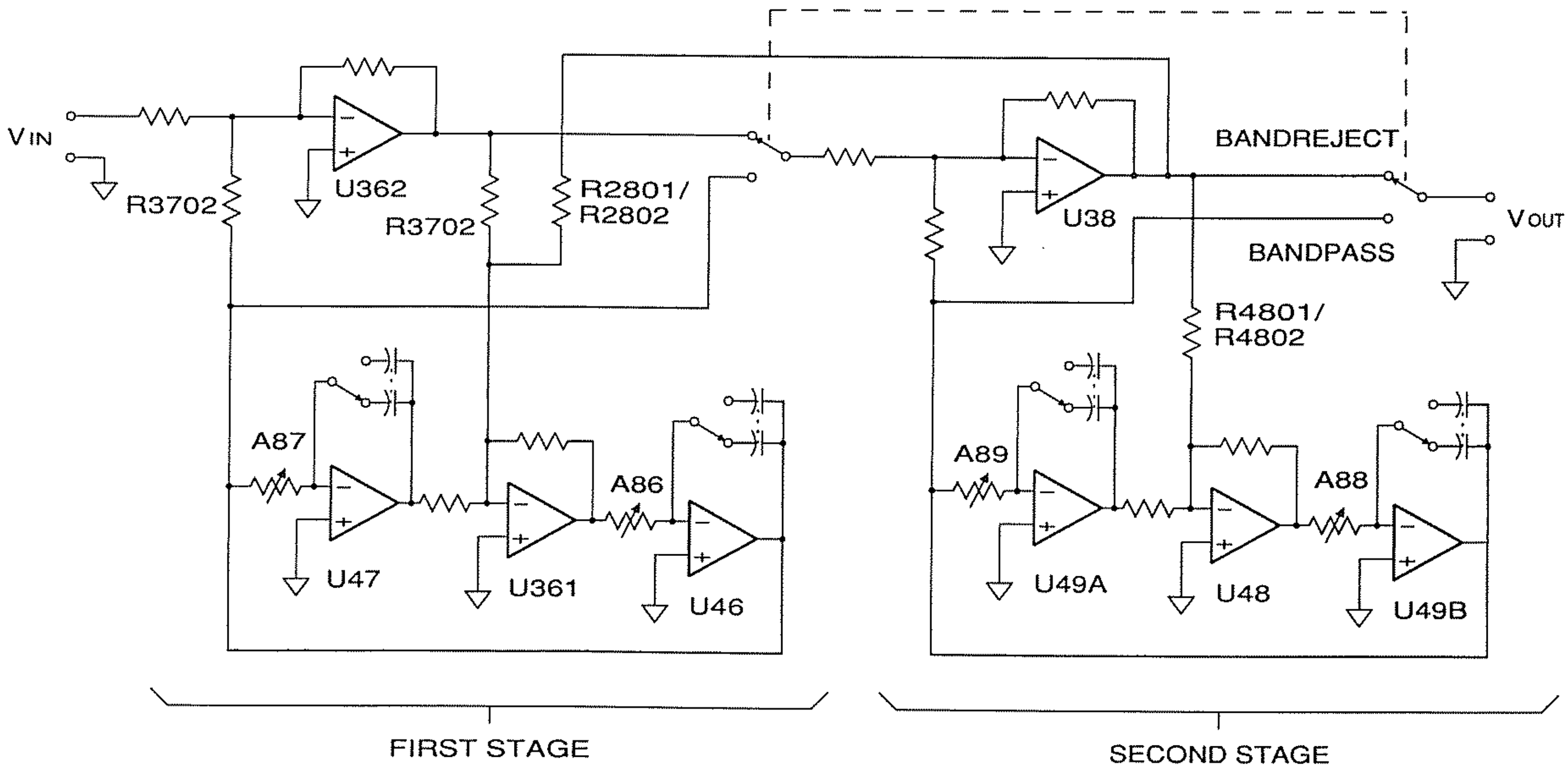
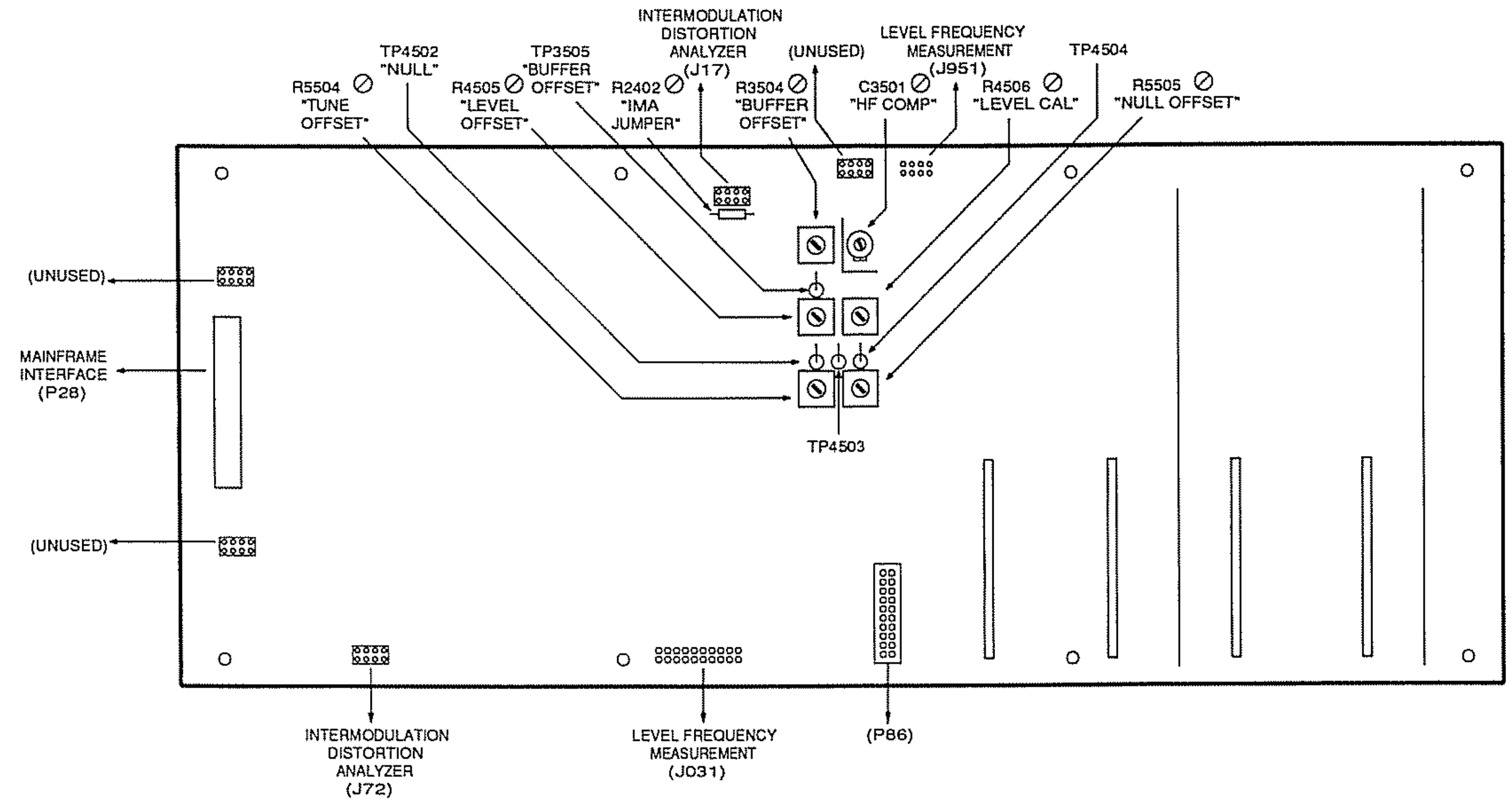
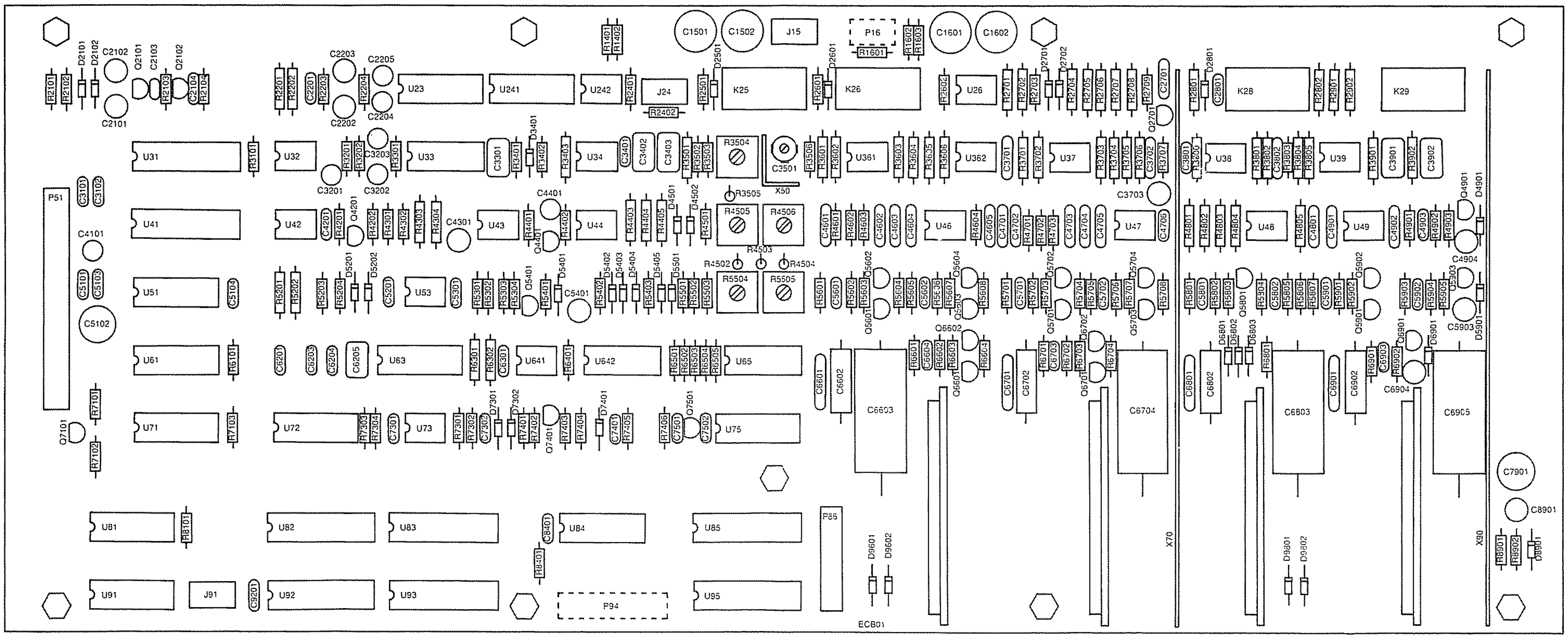


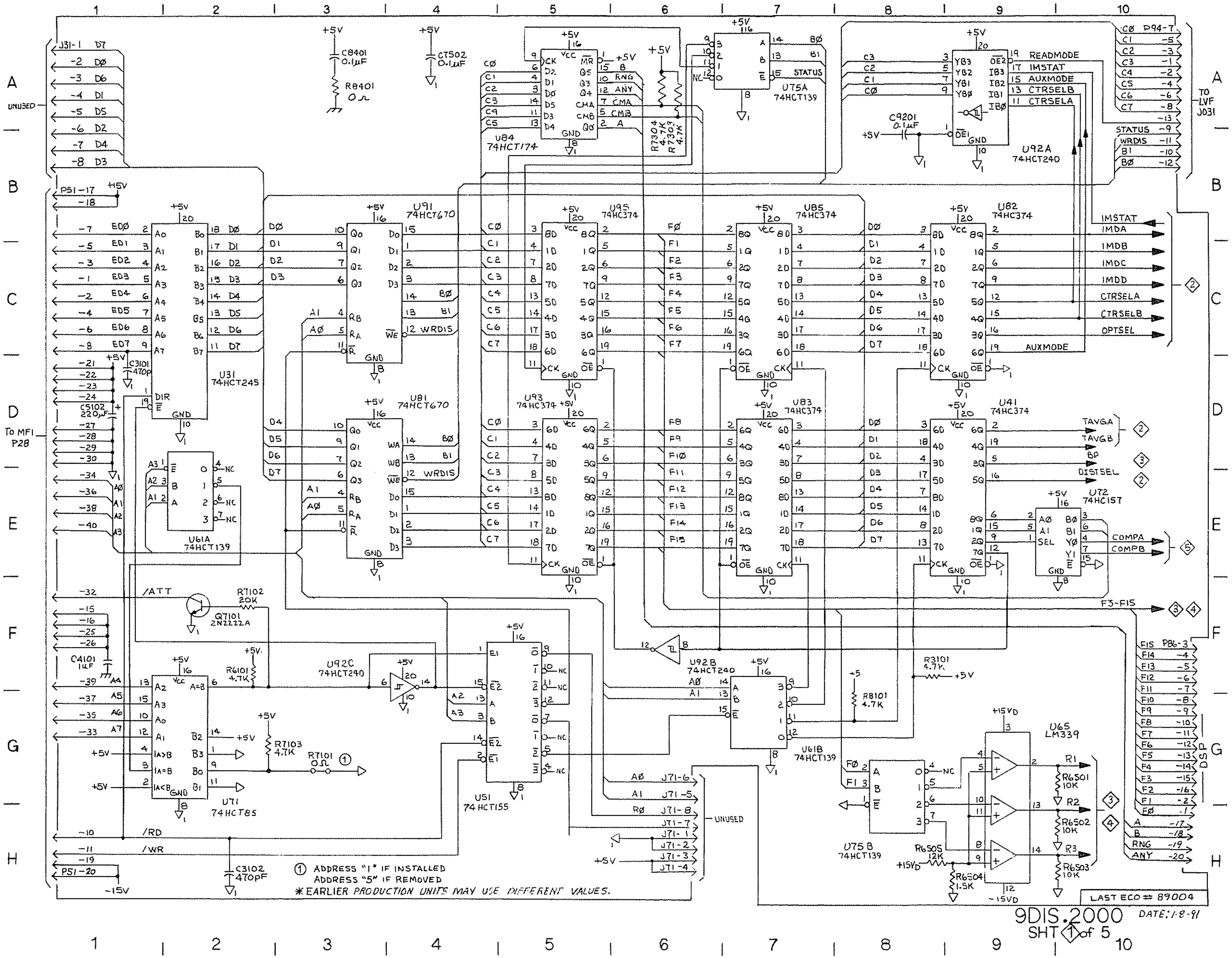
Figure DIS2.1 SIMPLIFIED DIAGRAM OF BANDPASS/BANDREJECT FILTER



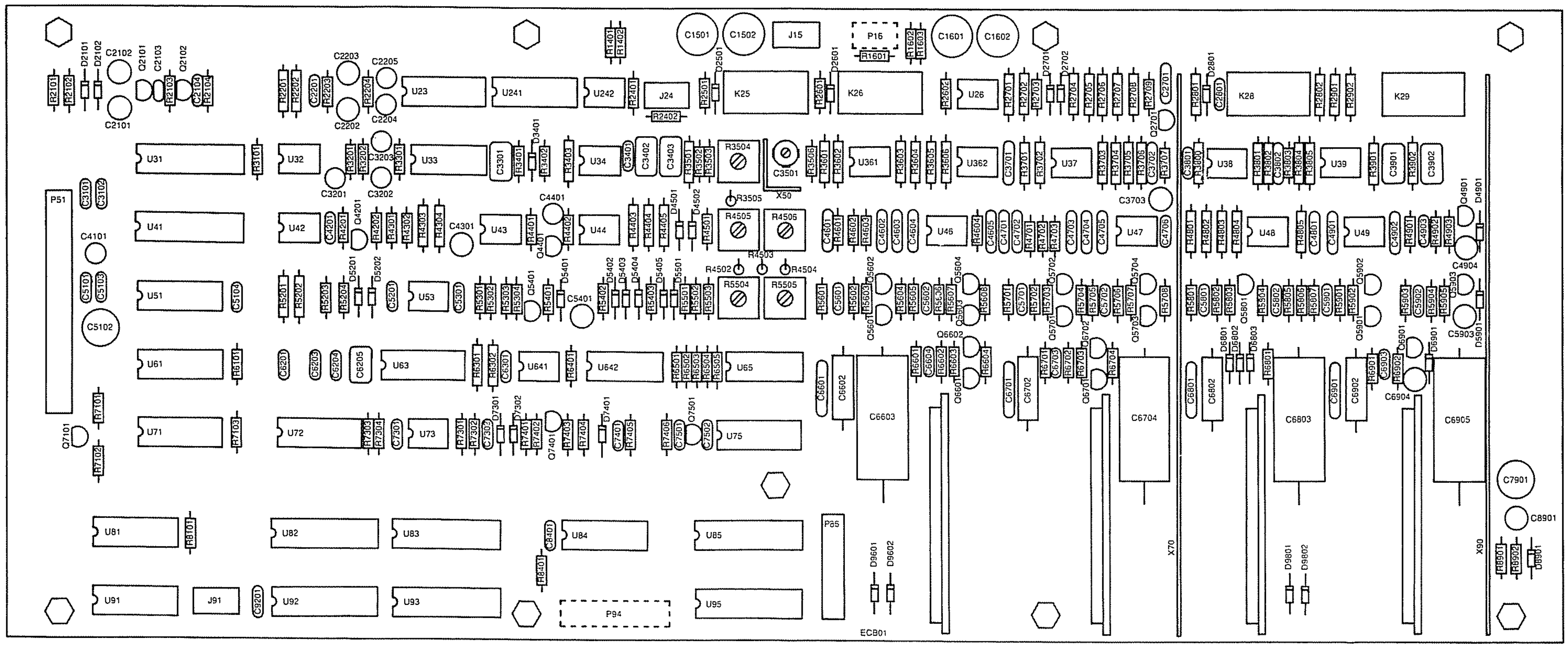
INTERMODULATION DISTORTION ANALYZER (J17)
LEVEL FREQUENCY MEASUREMENT (J951)
(UNUSED)
TP4502 "NULL"
TP3505 "BUFFER OFFSET"
TP4504
R5504 "TUNE OFFSET"
R4505 "LEVEL OFFSET"
R2402 "IMA JUMPER"
R3504 "BUFFER OFFSET"
C3501 "HF COMP"
R4506 "LEVEL CAL"
R5505 "NULL OFFSET"
(UNUSED)
MAINFRAME INTERFACE (P28)
(UNUSED)
TP4503
INTERMODULATION DISTORTION ANALYZER (J72)
LEVEL FREQUENCY MEASUREMENT (J031)
(P86)



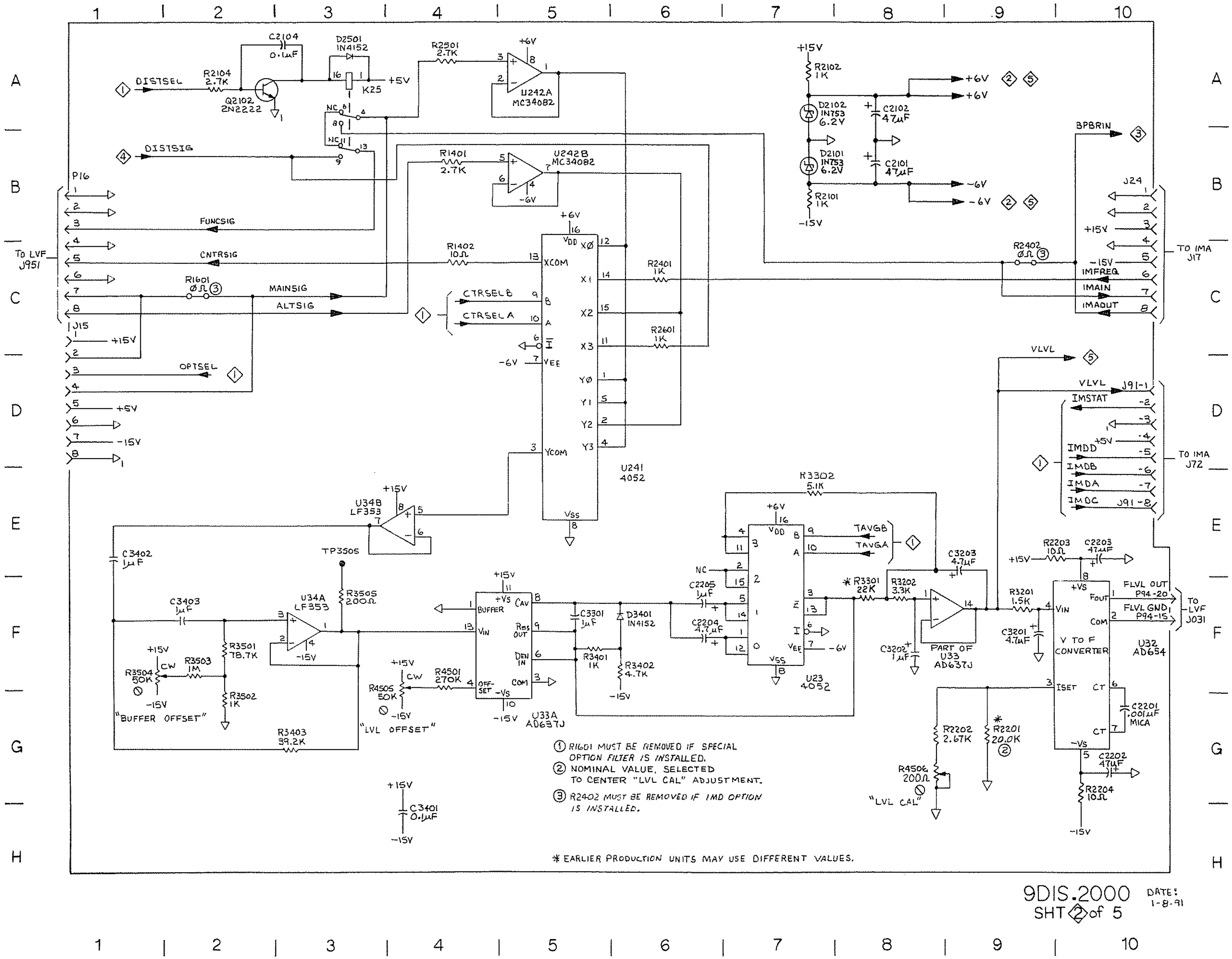
DISTORTION MEASUREMENT MODULE 9DIS.2000 (6200.DIS1.7)



TO LVF J031
TO MFI P28
UNUSED
J31-1
P51-17
P51-20
P94-7
P86-3
DSP
U31 74HCT245
U91 74HCT670
U81 74HCT670
U84 74HCT174
U75A 74HCT139
U75B 74HCT139
U92A 74HCT240
U92B 74HCT240
U92C 74HCT240
U95 74HC374
U93 74HC374
U85 74HC374
U83 74HC374
U82 74HC374
U41 74HC374
U72 74HC157
U61A 74HCT139
U61B 74HCT139
U71 74HCT85
U51 74HCT155
U65 LM339
Q7101 2N2222A
READMODE
IMSTAT
AUXMODE
CTRSELB
CTRSELA
STATUS
WRDIS
IMDA
IMDB
IMDC
IMDD
OPTSEL
TAVGA
TAVGB
BP
DISTSEL
COMPA
COMPB
F3-F15
/ATT
/RD
/WR
① ADDRESS "1" IF INSTALLED
ADDRESS "5" IF REMOVED
* EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.
LAST ECO # 89004
9DIS.2000
DATE: 1-8-91
SHT 1 of 5

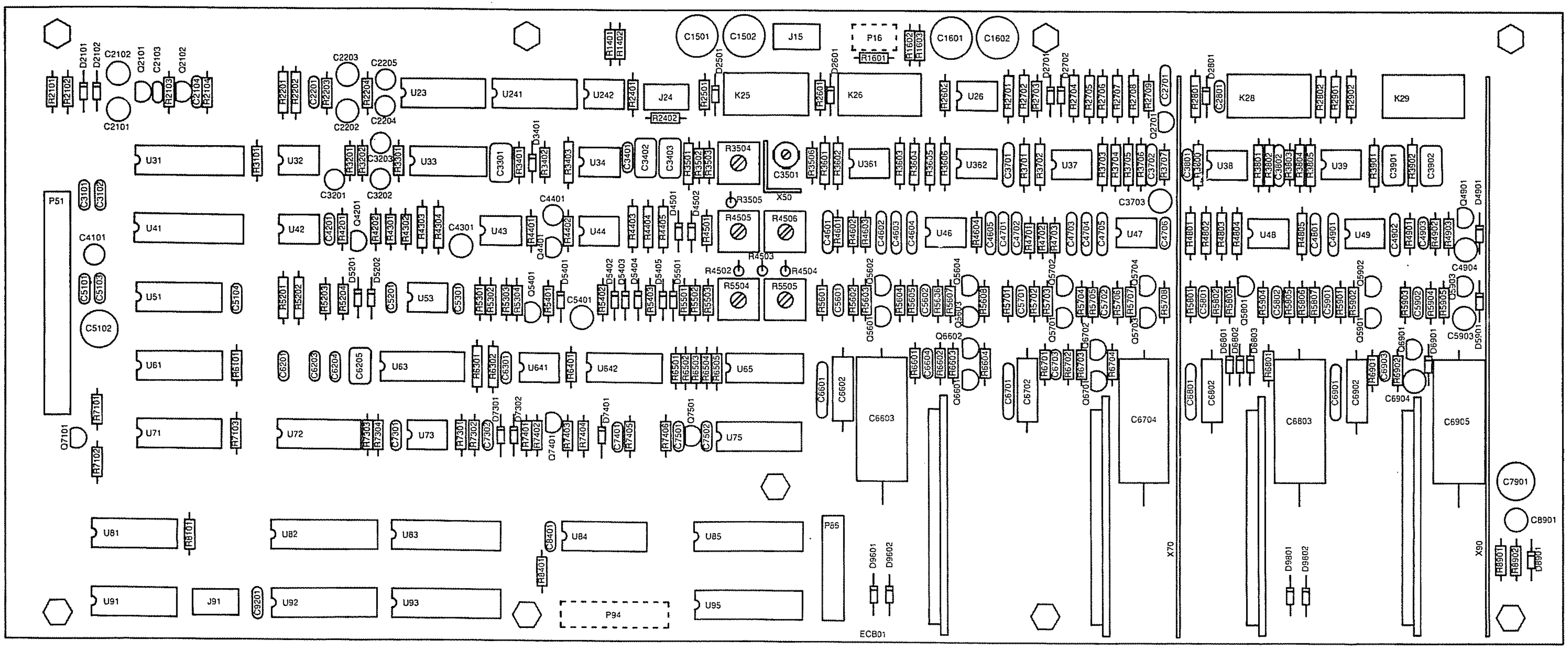


DISTORTION MEASUREMENT MODULE 9DIS.2000 (6200.DIS1.7)

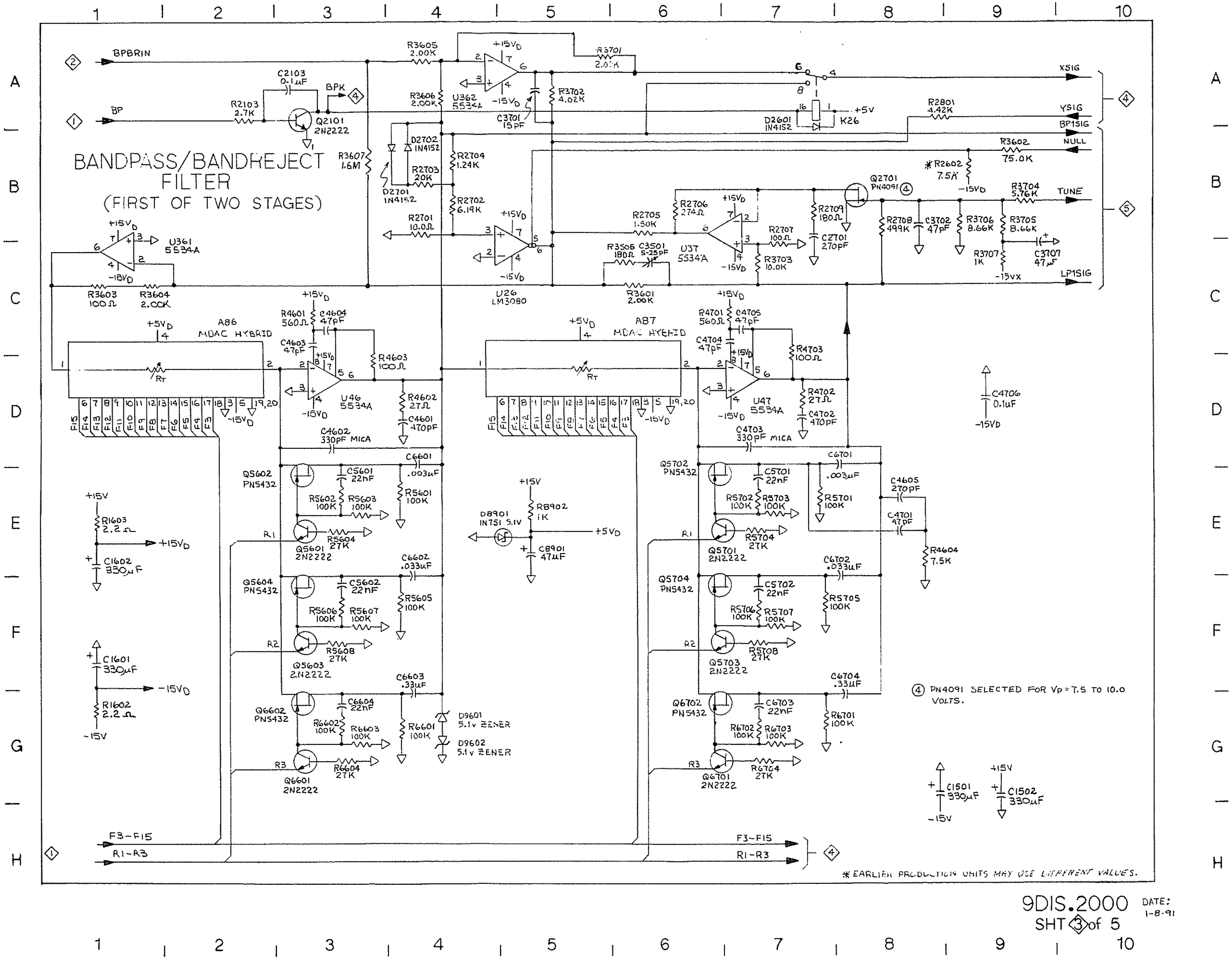


9DIS.2000 SHT 2 of 5

DATE: 1-8-91

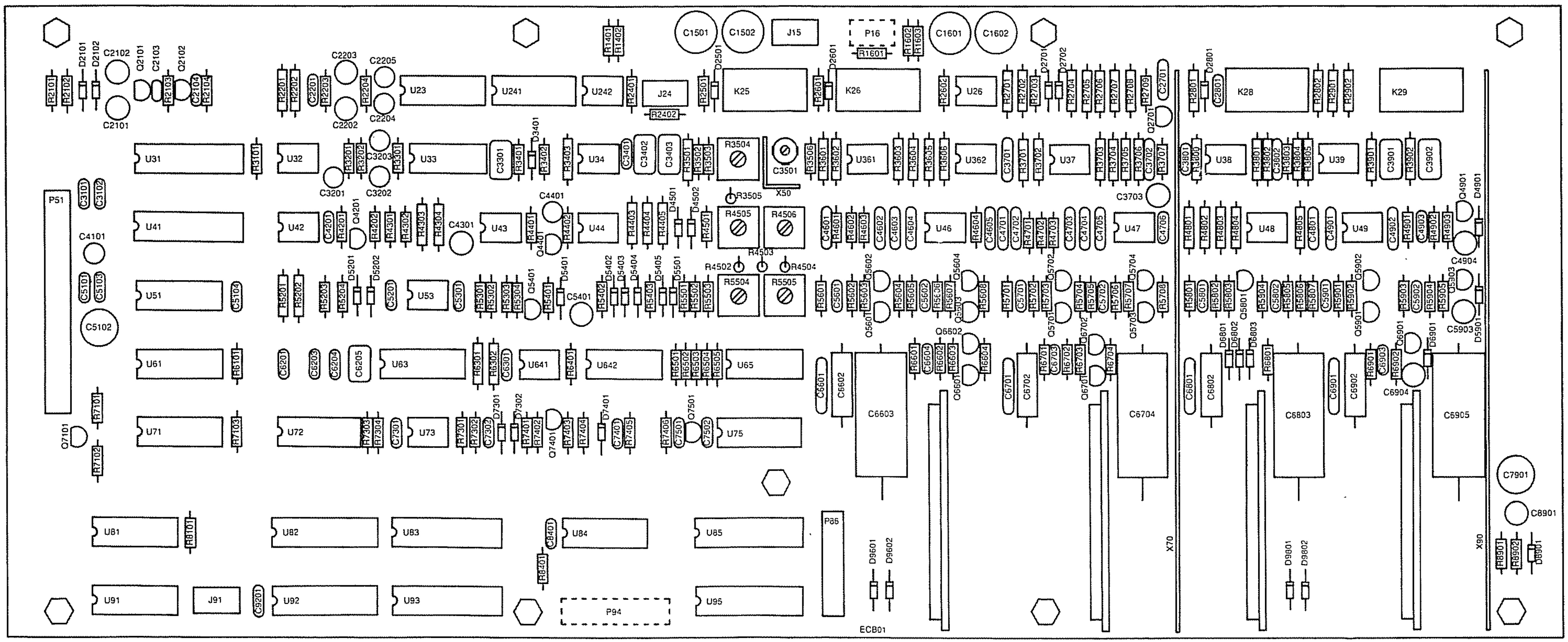


DISTORTION MEASUREMENT MODULE 9DIS.2000 (6200.DIS1.7)

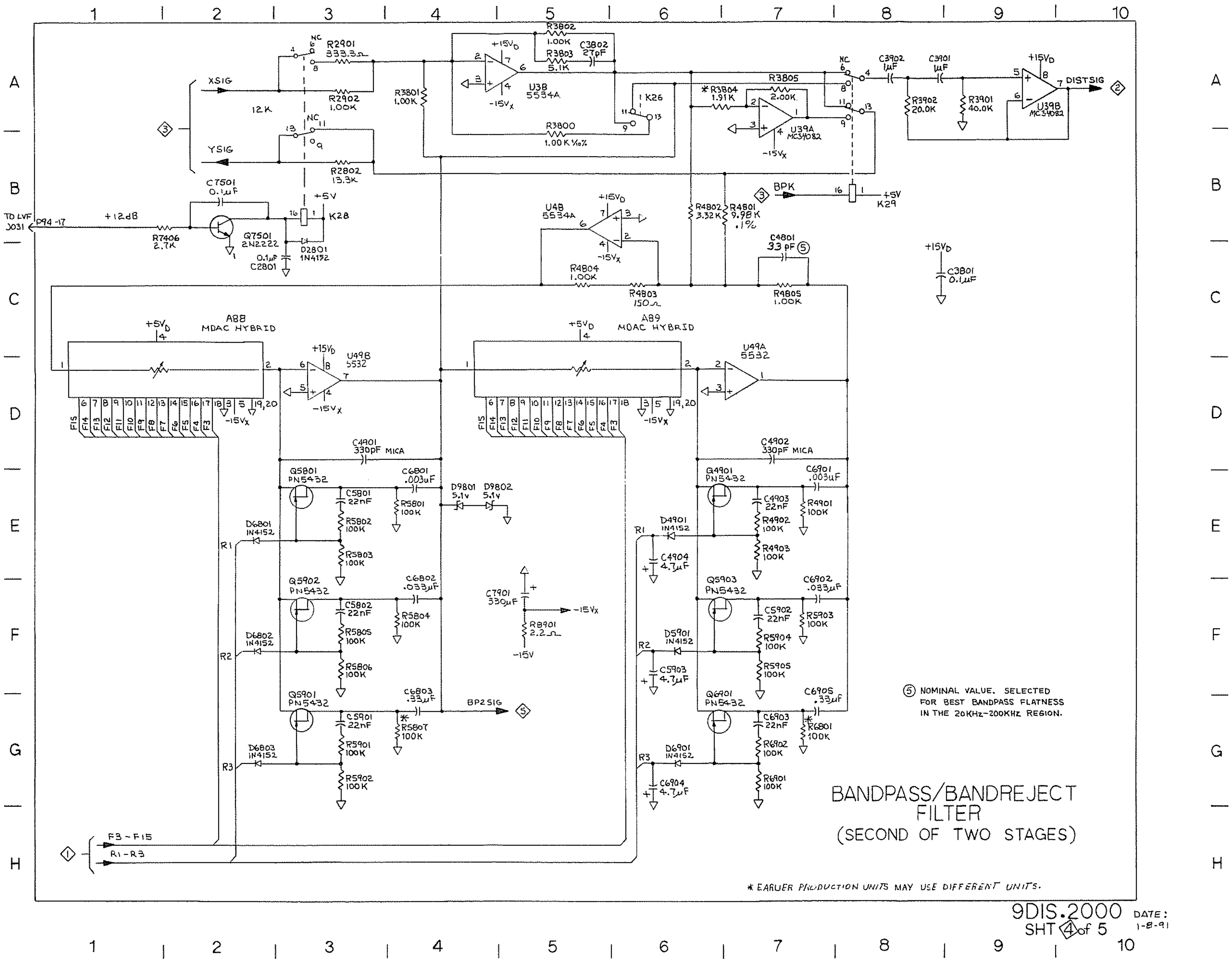


9DIS.2000 DATE: 1-8-91

SHT 3 of 5



DISTORTION MEASUREMENT MODULE 9DIS.2000 (6200.DIS1.7)



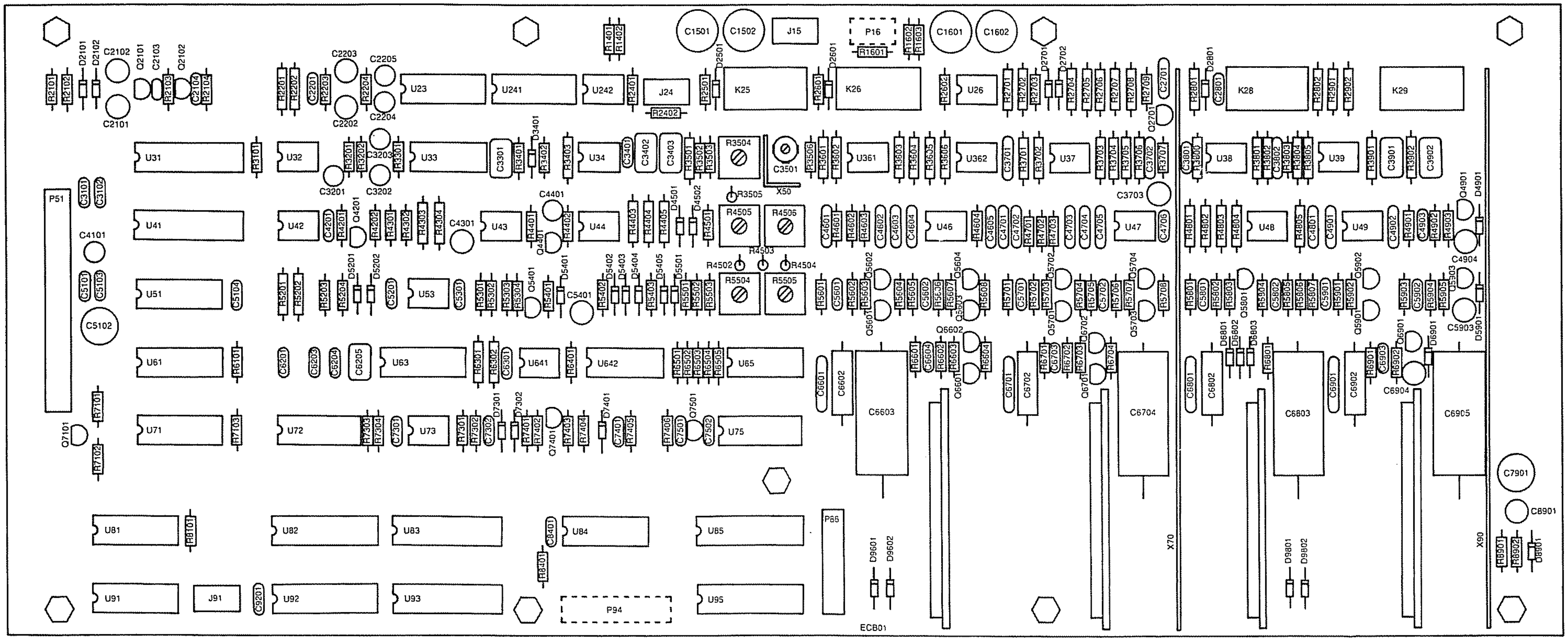
BANDPASS/BANDREJECT FILTER

(SECOND OF TWO STAGES)

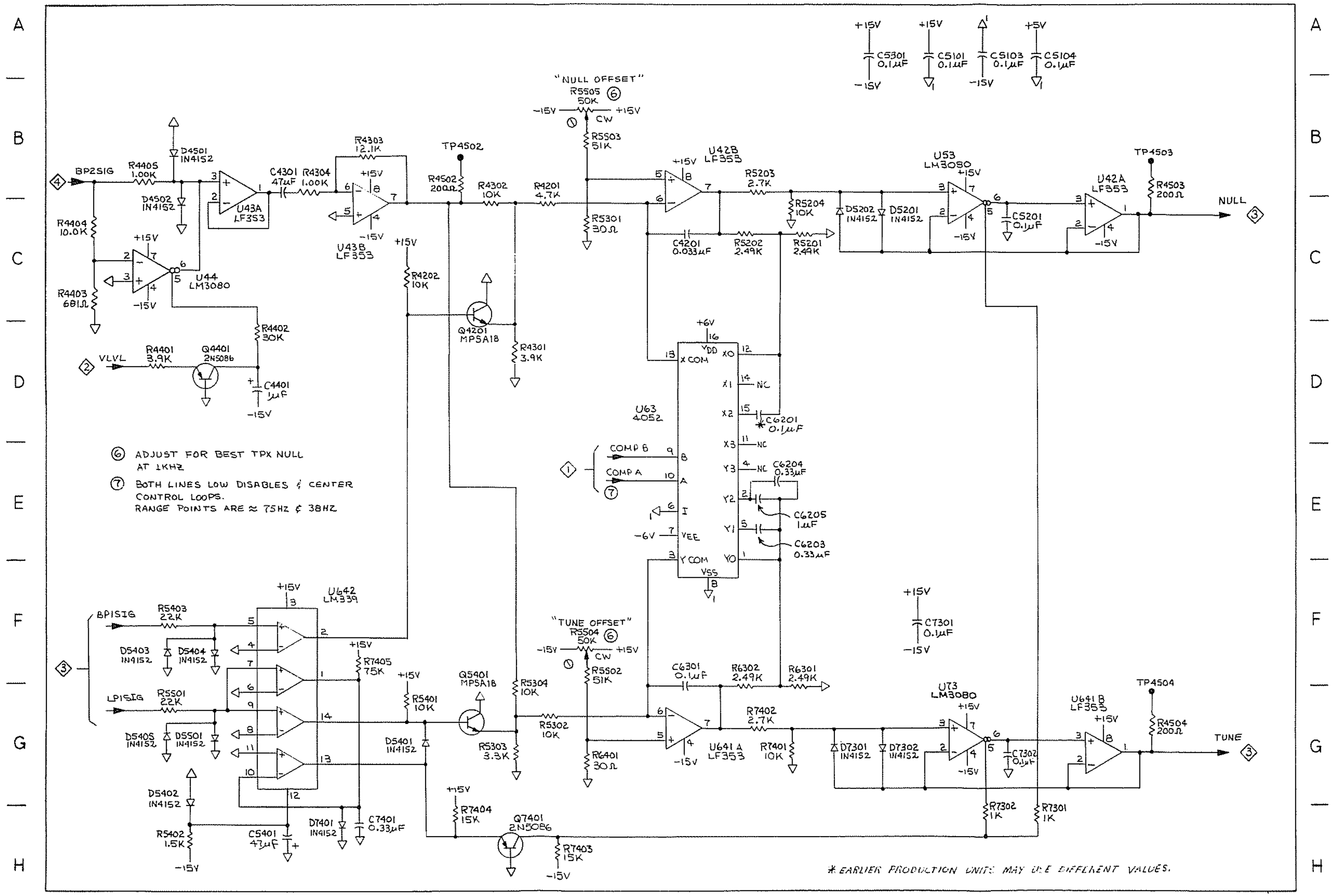
9DIS.2000

SHT 4 of 5

DATE: 1-8-91



DISTORTION MEASUREMENT MODULE 9DIS.2000 (6200.DIS1.7)



9DIS.2000 DATE: 1-8-91
SHT 5 of 5

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
A86	3D1	9DAC.1000	MDAC ECB ASSEMBLY	
A87	3D5	9DAC.1000	MDAC ECB ASSEMBLY	
A88	4D1	9DAC.1000	MDAC ECB ASSEMBLY	
A89	4D5	9DAC.1000	MDAC ECB ASSEMBLY	
C1501	3G8	2932.0337	CAP AL-EL 25V 20%	330uF
C1502	3G9	2932.0337	CAP AL-EL 25V 20%	330uF
C1601	3F1	2932.0337	CAP AL-EL 25V 20%	330uF
C1602	3E1	2932.0337	CAP AL-EL 25V 20%	330uF
C2101	2B8	2932.0476	CAP AL-EL 25V 20%	47uF
C2102	2A8	2932.0476	CAP AL-EL 25V 20%	47uF
C2103	3A3	2172.0104	CAP CERAM 100V 20%	.1uF
C2104	2A3	2172.0104	CAP CERAM 100V 20%	.1uF
C2201	2G10	2276.0102	CAP MICA 100V 1%	.001uF
C2202	2G10	2932.0476	CAP AL-EL 25V 20%	47uF
C2203	2E10	2932.0476	CAP AL-EL 25V 20%	47uF
C2204	2F6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C2205	2F6	2952.0105	CAP AL-EL 50V 20%	1uF
C2701	3B7	2296.0271	CAP MICA 500V 1%	270pF
C2801	4B3	2172.0104	CAP CERAM 100V 20%	.1uF
C3101	1D1	2296.0471	CAP MICA 500V 1%	470pF
C3102	1H2	2296.0471	CAP MICA 500V 1%	470pF
C3201	2F9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3202	2E8	2952.0105	CAP AL-EL 50V 20%	1uF
C3203	2E9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3301	2F5	2454.0105	CAP POLYE 50V 5%	1uF
C3401	2G4	2172.0104	CAP CERAM 100V 20%	.1uF
C3402	2E1	2454.0105	CAP POLYE 50V 5%	1uF
C3403	2F2	2454.0105	CAP POLYE 50V 5%	1uF
C3501	3C6	4450.0250	VAR CAP PC	5-25pF
C3701	3A5	2294.0150	CAP MICA 500V 5%	15pF
C3702	3B8	2294.0470	CAP MICA 500V 5%	47pF
C3703	3C9	2932.0476	CAP AL-EL 25V 20%	47uF
C3801	4C8	2172.0104	CAP CERAM 100V 20%	.1uF
C3802	4A5	2294.0270	CAP MICA 500V 5%	27pF
C3901	4A8	2454.0105	CAP POLYE 50V 5%	1uF
C3902	4A8	2454.0105	CAP POLYE 50V 5%	1uF
C4101	1F1	2952.0105	CAP AL-EL 50V 20%	1uF
C4201	5C6	2454.0333	CAP POLYE 50V 5%	.033uF
C4301	5B2	2932.0476	CAP AL-EL 25V 20%	47uF
C4401	5D2	2952.0105	CAP AL-EL 50V 20%	1uF
C4601	3D4	2296.0471	CAP MICA 500V 1%	470pF
C4602	3D3	2296.0331	CAP MICA 500V 1%	330pF
C4603	3C3	2294.0470	CAP MICA 500V 5%	47pF
C4604	3C3	2294.0470	CAP MICA 500V 5%	47pF
C4605	3E8	2296.0271	CAP MICA 500V 1%	270pF
C4701	3E8	2294.0470	CAP MICA 500V 5%	47pF
C4702	3D7	2296.0471	CAP MICA 500V 1%	470pF
C4703	3D7	2296.0331	CAP MICA 500V 1%	330pF
C4704	3C7	2294.0470	CAP MICA 500V 5%	47pF
C4705	3C7	2294.0470	CAP MICA 500V 5%	47pF
C4706	3D9	2172.0104	CAP CERAM 100V 20%	.1uF

REPLACEABLE ELECTRICAL PARTS LIST: 9DIS.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C4801	4C7	2172.0390	CAP CERAM 100V 20%	39pF
C4901	4D3	2296.0331	CAP MICA 500V 1%	330pF
C4902	4D7	2296.0331	CAP MICA 500V 1%	330pF
C4903	4E7	2454.0223	CAP POLYE 50V 5%	.022uF
C4904	4E6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5101	5A8	2172.0104	CAP CERAM 100V 20%	.1uF
C5102	1D1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5103	5A8	2172.0104	CAP CERAM 100V 20%	.1uF
C5104	5A9	2172.0104	CAP CERAM 100V 20%	.1uF
C5201	5C8	2454.0104	CAP POLYE 50V 5%	.1uF
C5301	5A7	2172.0104	CAP CERAM 100V 20%	.1uF
C5401	5H2	2932.0476	CAP AL-EL 25V 20%	47uF
C5601	3E3	2454.0223	CAP POLYE 50V 5%	.022uF
C5602	3F3	2454.0223	CAP POLYE 50V 5%	.022uF
C5701	3E7	2454.0223	CAP POLYE 50V 5%	.022uF
C5702	3F7	2454.0223	CAP POLYE 50V 5%	.022uF
C5801	4E3	2454.0223	CAP POLYE 50V 5%	.022uF
C5802	4E3	2454.0223	CAP POLYE 50V 5%	.022uF
C5901	4G3	2454.0223	CAP POLYE 50V 5%	.022uF
C5902	4F7	2454.0223	CAP POLYE 50V 5%	.022uF
C5903	4F6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6201	5D6	2454.0104	CAP POLYE 50V 5%	.1uF
C6203	5E6	2454.0334	CAP POLYE 50V 5%	.33uF
C6204	5E6	2454.0334	CAP POLYE 50V 5%	.33uF
C6205	5E6	2454.0105	CAP POLYE 50V 5%	1uF
C6301	5G6	2454.0104	CAP POLYE 50V 5%	.1uF
C6601	3D4	2296.0302	CAP MICA 500V 1%	.003uF
C6602	3E4	2576.0333	CAP POLYP 100V 1%	.033uF
C6603	3G4	2576.0334	CAP POLYP 100V 1%	.333uF
C6604	3G3	2454.0223	CAP POLYE 50V 5%	.022uF
C6701	3D7	2296.0302	CAP MICA 500V 1%	.003uF
C6702	3F8	2576.0333	CAP POLYP 100V 1%	.033uF
C6703	3G7	2454.0223	CAP POLYE 50V 5%	.022uF
C6704	3G8	2576.0334	CAP POLYP 100V 1%	.333uF
C6801	4E4	2296.0302	CAP MICA 500V 1%	.003uF
C6802	4F4	2576.0333	CAP POLYP 100V 1%	.033uF
C6803	4G4	2576.0334	CAP POLYP 100V 1%	.333uF
C6901	4F7	2296.0302	CAP MICA 500V 1%	.003uF
C6902	4F7	2576.0333	CAP POLYP 100V 1%	.033uF
C6903	4G7	2454.0223	CAP POLYE 50V 5%	.022uF
C6904	4G6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6905	4G7	2576.0334	CAP POLYP 100V 1%	.333uF
C7301	5F8	2172.0104	CAP CERAM 100V 20%	.1uF
C7302	5G8	2454.0104	CAP POLYE 50V 5%	.1uF
C7401	5H3	2454.0334	CAP POLYE 50V 5%	.33uF
C7501	4B2	2172.0104	CAP CERAM 100V 20%	.1uF
C7502	1A4	2172.0104	CAP CERAM 100V 20%	.1uF
C7901	4F9	2932.0337	CAP AL-EL 25V 20%	330uF
C8401	1A3	2172.0104	CAP CERAM 100V 20%	.1uF
C8901	3E5	2932.0476	CAP AL-EL 25V 20%	47uF
C9201	1B8	2172.0104	CAP CERAM 100V 20%	.1uF

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
D2101	2B7	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
D2102	2A7	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
D2501	2A3	3110.4152	DIODE SIGNAL	4152
D2601	3A7	3110.4152	DIODE SIGNAL	4152
D2701	3B4	3110.4152	DIODE SIGNAL	4152
D2702	3B4	3110.4152	DIODE SIGNAL	4152
D2801	4C3	3110.4152	DIODE SIGNAL	4152
D3401	2F6	3110.4152	DIODE SIGNAL	4152
D4501	4B1	3110.4152	DIODE SIGNAL	4152
D4502	4C2	3110.4152	DIODE SIGNAL	4152
D4901	4E6	3110.4152	DIODE SIGNAL	4152
D5201	5C7	3110.4152	DIODE SIGNAL	4152
D5202	5C7	3110.4152	DIODE SIGNAL	4152
D5401	5G4	3110.4152	DIODE SIGNAL	4152
D5402	5G2	3110.4152	DIODE SIGNAL	4152
D5403	5F1	3110.4152	DIODE SIGNAL	4152
D5404	5F2	3110.4152	DIODE SIGNAL	4152
D5405	5G1	3110.4152	DIODE SIGNAL	4152
D5501	5G2	3110.4152	DIODE SIGNAL	4152
D5901	4F6	3110.4152	DIODE SIGNAL	4152
D6801	4E2	3110.4152	DIODE SIGNAL	4152
D6802	4F2	3110.4152	DIODE SIGNAL	4152
D6803	4G2	3110.4152	DIODE SIGNAL	4152
D6901	4G6	3110.4152	DIODE SIGNAL	4152
D7301	5G7	3110.4152	DIODE SIGNAL	4152
D7302	5G7	3110.4152	DIODE SIGNAL	4152
D7401	5H3	3110.4152	DIODE SIGNAL	4152
D8901	3E5	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D9601	3G4	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D9602	3G4	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D9801	4E4	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D9802	4E4	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
J15	2C1,2D1	4221.1008	JACK PC 2 X .1	8 PIN
J24	2B10,2C10	4221.1008	JACK PC 2 X .1	8 PIN
J91	2D10,2E10	4221.1008	JACK PC 2 X .1	8 PIN
K25	2B3	4530.0002	RELAY PC LOW POWER	DPDT
K26	3A7,4A6	4530.0002	RELAY PC LOW POWER	DPDT
K28	4B3	4530.0002	RELAY PC LOW POWER	DPDT
K29	4B8	4530.0002	RELAY PC LOW POWER	DPDT
P16	2B1,2C1	4221.0072.1	PLUG PC 2X.1 X.83	72 PIN
P51	1B1,1C1,1D1,1E1,1F1,1G1,1H1	4151.1740	CABLE ASSY .05	RBN 17 40 COND
P86	1G10	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P94	1A10,1B10,2F10	4221.0072.1	PLUG PC 2X.1 X.83	72 PIN
Q2101	3A3	3211.2222	XSTR NPN TO92	PN2222A
Q2102	2A2	3211.2222	XSTR NPN TO92	PN2222A
Q2701	3B8	3214.4091.H	XSTR FET TO92 HI Vp	PN4091
Q4201	5D4	3211.0018	XSTR NPN TO92	MPSA18
Q4401	5D2	3211.5086	XSTR PNP TO92	PN5086

REPLACEABLE ELECTRICAL PARTS LIST: 9DIS.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
Q4901	4E6	3214.5432	XSTR FET TO92	PN5432
Q5401	5G4	3211.0018	XSTR NPN TO92	MPSA18
Q5601	3E3	3211.2222	XSTR NPN TO92	PN2222A
Q5602	3E2	3214.5432	XSTR FET TO92	PN5432
Q5603	3F3	3211.2222	XSTR NPN TO92	PN2222A
Q5604	3F3	3214.5432	XSTR FET TO92	PN5432
Q5701	3E7	3211.2222	XSTR NPN TO92	PN2222A
Q5702	3E7	3214.5432	XSTR FET TO92	PN5432
Q5703	3F7	3211.2222	XSTR NPN TO92	PN2222A
Q5704	3E7	3214.5432	XSTR FET TO92	PN5432
Q5801	4E3	3214.5432	XSTR FET TO92	PN5432
Q5901	4G3	3214.5432	XSTR FET TO92	PN5432
Q5902	4F3	3214.5432	XSTR FET TO92	PN5432
Q5903	4F6	3214.5432	XSTR FET TO92	PN5432
Q6601	3G3	3211.2222	XSTR NPN TO92	PN2222A
Q6602	3G3	3214.5432	XSTR FET TO92	PN5432
Q6701	3G7	3211.2222	XSTR NPN TO92	PN2222A
Q6702	3G7	3214.5432	XSTR FET TO92	PN5432
Q6901	4G6	3214.5432	XSTR FET TO92	PN5432
Q7101	1F2	3211.2222	XSTR NPN TO92	PN2222A
Q7401	5H4	3211.5086	XSTR PNP TO92	PN5086
Q7501	4B2	3211.2222	XSTR NPN TO92	PN2222A
R1401	2B4	1214.0272	RES 1/4W C FLM 5%	2.7K
R1402	2C4	1214.0100	RES 1/4W C FLM 5%	10
R1601	2C2	1214.0000	JUMPER .4 X.25	00
R1602	3G1	1214.0229	RES 1/4W C FLM 5%	2.2
R1603	3E1	1214.0229	RES 1/4W C FLM 5%	2.2
R2101	2B7	1214.0102	RES 1/4W C FLM 5%	1K
R2102	2A7	1214.0102	RES 1/4W C FLM 5%	1K
R2103	3A2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2104	2A2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2201	2G9	1136.2002	RES 1/8W M FLM 1%	20.0K
R2202	2G8	1136.2671	RES 1/8W M FLM 1%	2.67K
R2203	2E9	1214.0100	RES 1/4W C FLM 5%	10
R2204	2G10	1214.0100	RES 1/4W C FLM 5%	10
R2401	2C6	1214.0102	RES 1/4W C FLM 5%	1K
R2402	2C9	1214.0000	JUMPER .4 X.25	00
R2501	2A4	1214.0272	RES 1/4W C FLM 5%	2.7K
R2601	2C6	1214.0102	RES 1/4W C FLM 5%	1K
R2602	3B9	1214.0752	RES 1/4W C FLM 5%	7.5K
R2701	3B4	1136.1009	RES 1/8W M FLM 1%	10.0
R2702	3B4	1136.6191	RES 1/8W M FLM 1%	6.19K
R2703	3B4	1214.0203	RES 1/4W C FLM 5%	20K
R2704	3B4	1136.1241	RES 1/8W M FLM 1%	1.24K
R2705	3B6	1136.1501	RES 1/8W M FLM 1%	1.50K
R2706	3B6	1136.2740	RES 1/8W M FLM 1%	274
R2707	3C7	1136.1000	RES 1/8W M FLM 1%	100
R2708	3B8	1136.4993	RES 1/8W M FLM 1%	499K
R2709	3B7	1214.0181	RES 1/4W C FLM 5%	180
R2801	3A8	1136.4421	RES 1/8W M FLM 1%	4.42K
R2802	4B3	1136.1332	RES 1/8W M FLM 1%	13.3K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R2901	4A3	1139.3330	RES 1/8W M FLM .1%	333.3
R2902	4A3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3101	1F8	1214.0472	RES 1/4W C FLM 5%	4.7K
R3201	2F9	1214.0152	RES 1/4W C FLM 5%	1.5K
R3202	2F8	1214.0332	RES 1/4W C FLM 5%	3.3K
R3301	2F8	1214.0223	RES 1/4W C FLM 5%	22K
R3302		1214.0512	RES 1/4W C FLM 5%	5.1K
R3401	2F5	1214.0102	RES 1/4W C FLM 5%	1K
R3402	2F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R3403	2G3	1136.3922	RES 1/8W M FLM 1%	39.2K
R3501	2F2	1136.7872	RES 1/8W M FLM 1%	78.7K
R3502	2G2	1214.0102	RES 1/4W C FLM 5%	1K
R3503	2F2	1214.0105	RES 1/4W C FLM 5%	1M
R3504	2F1	4412.0503	POT TRIM PC ENC	50K
R3505	2F3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R3506	3C6	1214.0181	RES 1/4W C FLM 5%	180
R3601	3C6	1139.2001	RES 1/8W M FLM .1%	2.00K
R3602	3B9	1136.7502	RES 1/8W M FLM 1%	75.0K
R3603	3C1	1136.1000	RES 1/8W M FLM 1%	100
R3604	3C1	1139.2001	RES 1/8W M FLM .1%	2.00K
R3605	3A4	1139.2001	RES 1/8W M FLM .1%	2.00K
R3606	3A4	1139.2001	RES 1/8W M FLM .1%	2.00K
R3607	3B3	1214.0165	RES 1/4W C FLM 5%	1.6M
R3701	3A5	1139.2001	RES 1/8W M FLM .1%	2.00K
R3702	3A5	1136.4021	RES 1/8W M FLM 1%	4.02K
R3703	3C7	1136.1002	RES 1/8W M FLM 1%	10.0K
R3704	3B9	1136.5761	RES 1/8W M FLM 1%	5.76K
R3705	3B9	1136.8661	RES 1/8W M FLM 1%	8.66K
R3706	3B9	1136.8661	RES 1/8W M FLM 1%	8.66K
R3707	3C9	1214.0102	RES 1/4W C FLM 5%	1K
R3800	4B5	1139.1001	RES 1/8W M FLM .1%	1.00K
R3801	4A4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3802	4A5	1139.1001	RES 1/8W M FLM .1%	1.00K
R3803	4A5	1214.0512	RES 1/4W C FLM 5%	5.1K
R3804	4A6	1136.1911	RES 1/8W M FLM 1%	1.91K
R3805	4A7	1139.2001	RES 1/8W M FLM .1%	2.00K
R3901	4A9	1139.4002	RES 1/8W M FLM .1%	40.0K
R3902	4A8	1139.2002	RES 1/8W M FLM .1%	20.0K
R4201	5B5	1214.0472	RES 1/4W C FLM 5%	4.7K
R4202	5C3	1214.0103	RES 1/4W C FLM 5%	10K
R4301	5D4	1214.0392	RES 1/4W C FLM 5%	3.9K
R4302	5B4	1214.0103	RES 1/4W C FLM 5%	10K
R4303	4B3	1136.1212	RES 1/8W M FLM 1%	12.1K
R4304	4B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R4401	4D1	1214.0392	RES 1/4W C FLM 5%	3.9K
R4402	5D2	1214.0303	RES 1/4W C FLM 5%	30K
R4403	5C1	1136.6810	RES 1/8W M FLM 1%	681
R4404	5C1	1136.1002	RES 1/8W M FLM 1%	10.0K
R4405	5B1	1139.1001	RES 1/8W M FLM .1%	1.00K
R4501	2F4	1214.0274	RES 1/4W C FLM 5%	270K
R4502	5B4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4503	5B10	1214.0201.1	RES 1/4W C FLM 5% VERT	200

REPLACEABLE ELECTRICAL PARTS LIST: 9DIS.2000

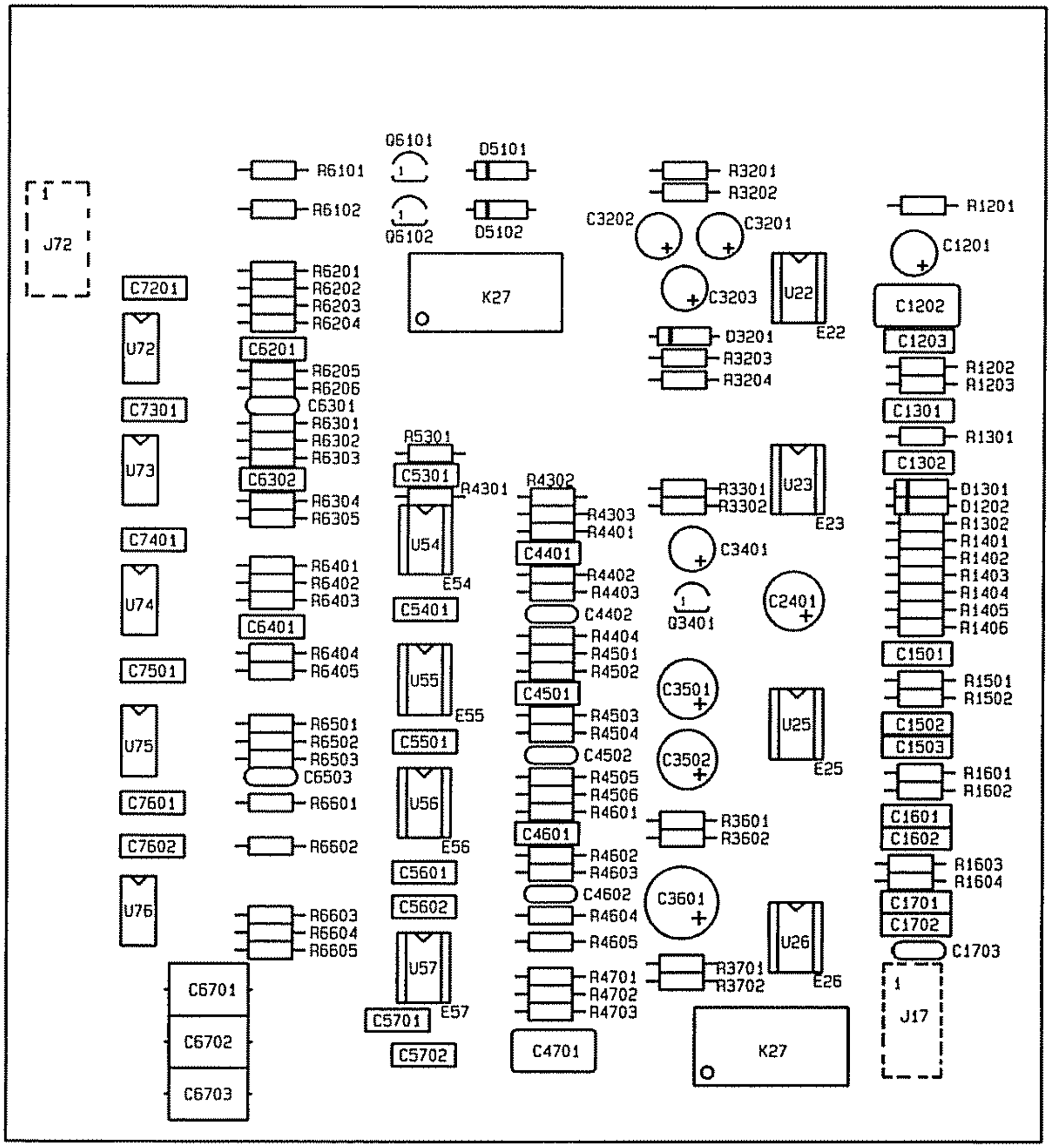
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4504	5G10	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R4505	2F4	4412.0503	POT TRIM PC ENC	50K
R4506	2G8	4412.0201	POT TRIM PC ENC	200
R4601	3C3	1214.0561	RES 1/4W C FLM 5%	560
R4602	3D4	1214.0270	RES 1/4W C FLM 5%	27
R4603	3C3	1214.0101	RES 1/4W C FLM 5%	100
R4604	3E8	1214.0752	RES 1/4W C FLM 5%	7.5K
R4701	3C7	1214.0561	RES 1/4W C FLM 5%	560
R4702	3D7	1214.0270	RES 1/4W C FLM 5%	27
R4703	3C7	1214.0101	RES 1/4W C FLM 5%	100
R4801	4B7	1139.9981	RES 1/8W M FLM .1%	9.98K
R4802	4B6	1136.3321	RES 1/8W M FLM 1%	3.32K
R4803	4C6	1136.1500	RES 1/8W M FLM 1%	150
R4804	4C5	1139.1001	RES 1/8W M FLM .1%	1.00K
R4805	4C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R4901	4E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R4902	4E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R4903	4E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5201	5C7	1136.2491	RES 1/8W M FLM 1%	2.49K
R5202	5C6	1136.2491	RES 1/8W M FLM 1%	2.49K
R5203	5B6	1214.0272	RES 1/4W C FLM 5%	2.7K
R5204	5C7	1214.0103	RES 1/4W C FLM 5%	10K
R5301	5C5	1214.0300	RES 1/4W C FLM 5%	30
R5302	5G5	1214.0103	RES 1/4W C FLM 5%	10K
R5303	5G4	1214.0332	RES 1/4W C FLM 5%	3.3K
R5304	5F4	1214.0103	RES 1/4W C FLM 5%	10K
R5401	5G3	1214.0103	RES 1/4W C FLM 5%	10K
R5402	5H2	1214.0152	RES 1/4W C FLM 5%	1.5K
R5403	5F1	1214.0223	RES 1/4W C FLM 5%	22K
R5501	5G1	1214.0223	RES 1/4W C FLM 5%	22K
R5502	5F5	1214.0513	RES 1/4W C FLM 5%	51K
R5503	5B5	1214.0513	RES 1/4W C FLM 5%	51K
R5504	5F5	4412.0503	POT TRIM PC ENC	50K
R5505	5B5	4412.0503	POT TRIM PC ENC	50K
R5601	3E4	1214.0104	RES 1/4W/C/FLM 5%	100K
R5602	3E3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5603	3E3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5604	3E3	1214.0273	RES 1/4W C FLM 5%	27K
R5605	3F4	1214.0104	RES 1/4W/C/FLM 5%	100K
R5606	3F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5607	3F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5608	3F3	1214.0273	RES 1/4W C FLM 5%	27K
R5701	3E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5702	3E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5703	3E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5704	3E7	1214.0273	RES 1/4W C FLM 5%	27K
R5705	3F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5706	3F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5707	3F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5708	3F7	1214.0273	RES 1/4W C FLM 5%	27K
R5801	3E4	1214.0104	RES 1/4W/C/FLM 5%	100K
R5802	4E3	1214.0104	RES 1/4W/C/FLM 5%	100K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R5803	3E3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5804	4F4	1214.0104	RES 1/4W/C/FLM 5%	100K
R5805	4F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5806	4F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5807	4G4	1214.0104	RES 1/4W/C/FLM 5%	100K
R5901	4G3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5902	4G3	1214.0104	RES 1/4W/C/FLM 5%	100K
R5903	4F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5904	4F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R5905	4F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6101	1F2	1214.0472	RES 1/4W C FLM 5%	4.7K
R6301	5F7	1136.2491	RES 1/8W M FLM 1%	2.49K
R6302	5G6	1136.2491	RES 1/8W M FLM 1%	2.49K
R6401	5G5	1214.0300	RES 1/4W C FLM 5%	30
R6501	1G10	1214.0103	RES 1/4W C FLM 5%	10K
R6502	1H10	1214.0103	RES 1/4W C FLM 5%	10K
R6503	1H10	1214.0103	RES 1/4W C FLM 5%	10K
R6504	1H9	1214.0152	RES 1/4W C FLM 5%	1.5K
R6505	1H8	1214.0123	RES 1/4W C FLM 5%	12K
R6601	3G4	1214.0104	RES 1/4W/C/FLM 5%	100K
R6602	3G3	1214.0104	RES 1/4W/C/FLM 5%	100K
R6603	3G3	1214.0104	RES 1/4W/C/FLM 5%	100K
R6604	3G3	1214.0273	RES 1/4W C FLM 5%	27K
R6701	3G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6702	3G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6703	3G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6704	3G7	1214.0273	RES 1/4W C FLM 5%	27K
R6801	4G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6901	4G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6902	4G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R7101	1G3	1214.0000	JUMPER .4 X.25	00
R7102	1F2	1214.0203	RES 1/4W C FLM 5%	20K
R7103	1F2	1214.0472	RES 1/4W C FLM 5%	4.7K
R7301	5G9	1214.0102	RES 1/4W C FLM 5%	1K
R7302	5G8	1214.0102	RES 1/4W C FLM 5%	1K
R7303	1A6	1214.0472	RES 1/4W C FLM 5%	4.7K
R7304	1A6	1214.0472	RES 1/4W C FLM 5%	4.7K
R7401	5G7	1214.0103	RES 1/4W C FLM 5%	10K
R7402	5G6	1214.0272	RES 1/4W C FLM 5%	2.7K
R7403	5H5	1214.0153	RES 1/4W C FLM 5%	15K
R7404	5H4	1214.0153	RES 1/4W C FLM 5%	15K
R7405	5F3	1214.0753	RES 1/4W C FLM 5%	75K
R7406	4B1	1214.0272	RES 1/4W C FLM 5%	2.7K
R8101	1G8	1214.0472	RES 1/4W C FLM 5%	4.7K
R8401		1214.0000	JUMPER .4 X.25	00
R8901	4F5	1214.0229	RES 1/4W C FLM 5%	2.2
R8902	3E5	1214.0102	RES 1/4W C FLM 5%	1K
U23	2E7	3321.4052	MULTIPLEX 4X DIFF	4052
U241	2C5	3321.4052	MULTIPLEX 4X DIFF	4052
U242	2A5,2B5	3412.0082	OP AMP DUAL	MC34082

REPLACEABLE ELECTRICAL PARTS LIST: 9DIS.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U26	3C4	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U31	1C2	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U32	2F10	3441.0654	CONVERTER VOLT TO FREQ	AD654J
U33	2F5,2F8	3441.0637	CONVERTER RMS TO DC	AD637J
U34	2F3,2E4	3412.0353	OP AMP DUAL	TL072/LF353
U361	3C1	3411.5534	OP AMP SINGLE	5534A
U362	3A4	3411.5534	OP AMP SINGLE	5534A
U37	3B7	3411.5534	OP AMP SINGLE	5534A
U38	4A5	3411.5534	OP AMP SINGLE	5534A
U39	4A7,4A9	3412.0082	OP AMP DUAL	MC34082
U41	1D9	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U42	5B6,5C9	3412.0353	OP AMP DUAL	TL072/LF353
U43	4B2,5C3	3412.0353	OP AMP DUAL	TL072/LF353
U44	4C1,5C1	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U46	3D3	3411.5534	OP AMP SINGLE	5534A
U47	3D7	3411.5534	OP AMP SINGLE	5534A
U48	4B6	3411.5534	OP AMP SINGLE	5534A
U49	4D3,4D7	3412.5532	OP AMP DUAL	5532
U51	1F5	3313.0155	DECODER 2 X 2-LN/4-LN	74LS155
U53	5B8	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U61	1E2,1G7	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
U63	5D6	3321.4052	MULTIPLEX 4X DIFF	4052
U641	5F6,5G9	3412.0353	OP AMP DUAL	TL072/LF353
U642	5F2	3424.0339	COMPARATOR QUAD	LM339
U65	1G9	3424.0339	COMPARATOR QUAD	LM339
U71	1G2	3313.0085	COMPARATOR 4-BIT MAG	74LS85
U72	1E10	3323.0157	MULTIPLEXER 4 X 2CH	74HC157
U73	5G8	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U75	1A7,1G8	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
U81	1D3	3313.0670	REGISTER FILE 4X4	74LS670
U82	1C9	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U83	1D7	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U84	1A5	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U85	1C7	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U91	1C3	3313.0670	REGISTER FILE 4X4	74LS670
U92	1A9,1F4,1F6	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U93	1D5	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374
U95	1C5	3323.0374	FLIP-FLOP 8X D TRI-ST	74HC374

IMA-1 IMD ANALYZER OPTION



IMD ANALYZER OPTION 9IMA.1000 (6200.IMA1.2)

IMA-1, IMD ANALYZER OPTION

SMPTE Demodulator & Signal Switching <1>

The IMD analyzer input is derived from J17-7 and is connected to the option bypass relay K27. In its off state K27 redirects the signal back to the DIS module through J17-8. If an IMD analysis mode is selected, K27 is energized and routes the signal to a 7-pole highpass filter at approximately 2 kHz. The purpose of this filter is to remove the lower 40-500 Hz tone from the two-tone SMPTE IMD test signal. U26A, U26B, U25B and their components comprise 6 of the 7 poles of this filter. C1501 adds the seventh pole and provides coupling into the variable gain amplifier U25A.

The output of the variable gain amplifier is fed into a precision full-wave rectifier consisting of U23A and U23B and integrated by the action of C1301 and C1302. The resultant dc voltage at this point is proportional to the test signal's high frequency tone amplitude. This voltage is compared with VLVL from J72-1, integrated, and fed back to JFET Q3401 as a gain correction signal. VLVL is derived from the LEVEL voltmeter on the DIS module and represents the composite test signal amplitude. R3201, R3202, C3201, and C3202 filter VLVL to eliminate any ac ripple components that could cause residual SMPTE IMD.

C3201 clamps the output of the amplitude control integrator from excessive positive excursions. R3301 and R3302 allow 1/2 of the ac signal across the variable resistance JFET, Q3401, to be superimposed on its gate control voltage. This linearizes the resistance characteristic of the JFET. Q3401 is also selected for high pinch-off voltage to insure good linearity.

The output of full-wave rectifier U23A is passed through a 700 Hz 3-pole lowpass filter to limit the measurement bandwidth and reduce noise. The demodulated SMPTE IMD signal at this point is coupled through C1201 and presented to the mode selection relay, K42, and J17-6. In the CCIF IMD analysis mode this signal consists of almost pure difference frequency product and is routed to the main frequency counter located on the LVF board. K42 is energized only in the SMPTE mode. For CCIF or DIM measurements, K42 switches the input signal directly into the next stage. Relays K27 and K42 are switched by Q6101 and Q6102 which are driven by control bits from the DIS module through J72.

IMD Analyzer Bandpass Filter <2>

The IMD analyzer bandpass filter consists of two stages of a 2.45 kHz elliptic lowpass cascaded with a 30 Hz highpass. In the CCIF and DIM modes this filter rejects the IM test signal components located above 3 kHz. In the SMPTE mode it rejects demodulator output harmonics that are not completely removed by the 700 Hz 3-pole lowpass filter.

The elliptic filter design is based upon "FDNR" elements (Frequency Dependent Negative Resistors). C4402, C4502, C4602, C6301, C6303, C6501, and C6503 compensate for capacitor dissipation factor and op-amp gain-bandwidth effects. Filter response is typically ±0.3 dB to 2.40 kHz, with an extremely sharp rolloff above 2.45 kHz. Some units may contain selected resistors paralleling R4505, R6401, or R6501 which are used to trim the corner response of the filter.

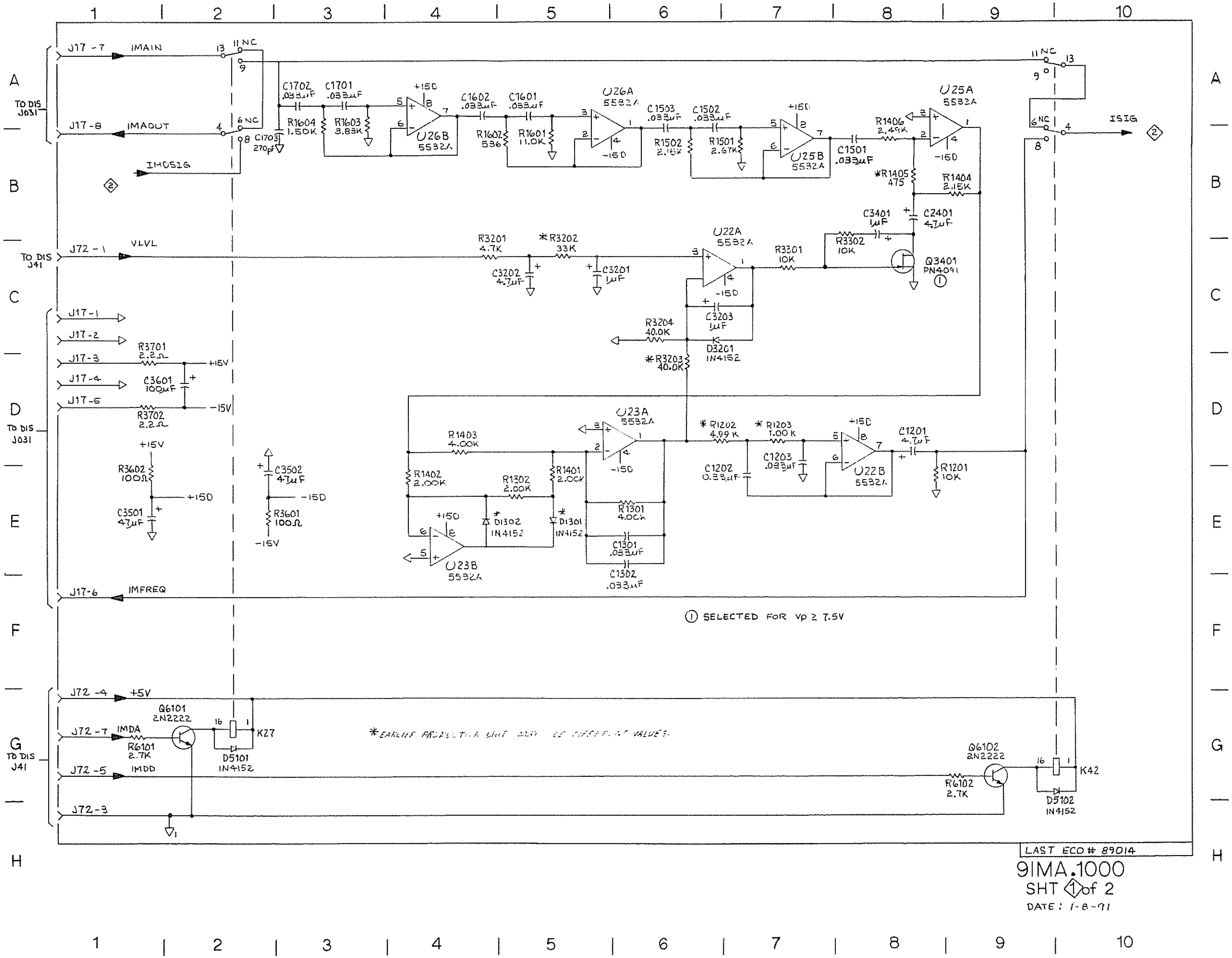
The two sections of the elliptic filter are separated by a +24 dB (x16) gain stage consisting of U57B, R4701, and R4702. This amplifier corrects for the inherent 6 dB losses in both filter stages and scales the IMD measurement ranges to be 4 times more sensitive than THD+N ranges. U57A is a dc servo that senses the offset through U57B and applies a correction voltage through R4302. Due to op-amp bias currents the typical dc voltage present at pin 1 of U57A will be approximately +0.5 to +1 V. The output from the second elliptic stage is buffered through U76A and fed to a 30 Hz highpass filter, U76B and related components.

TABLE IMA1.1
BP/BR FILTER TUNING VS IMD MODE

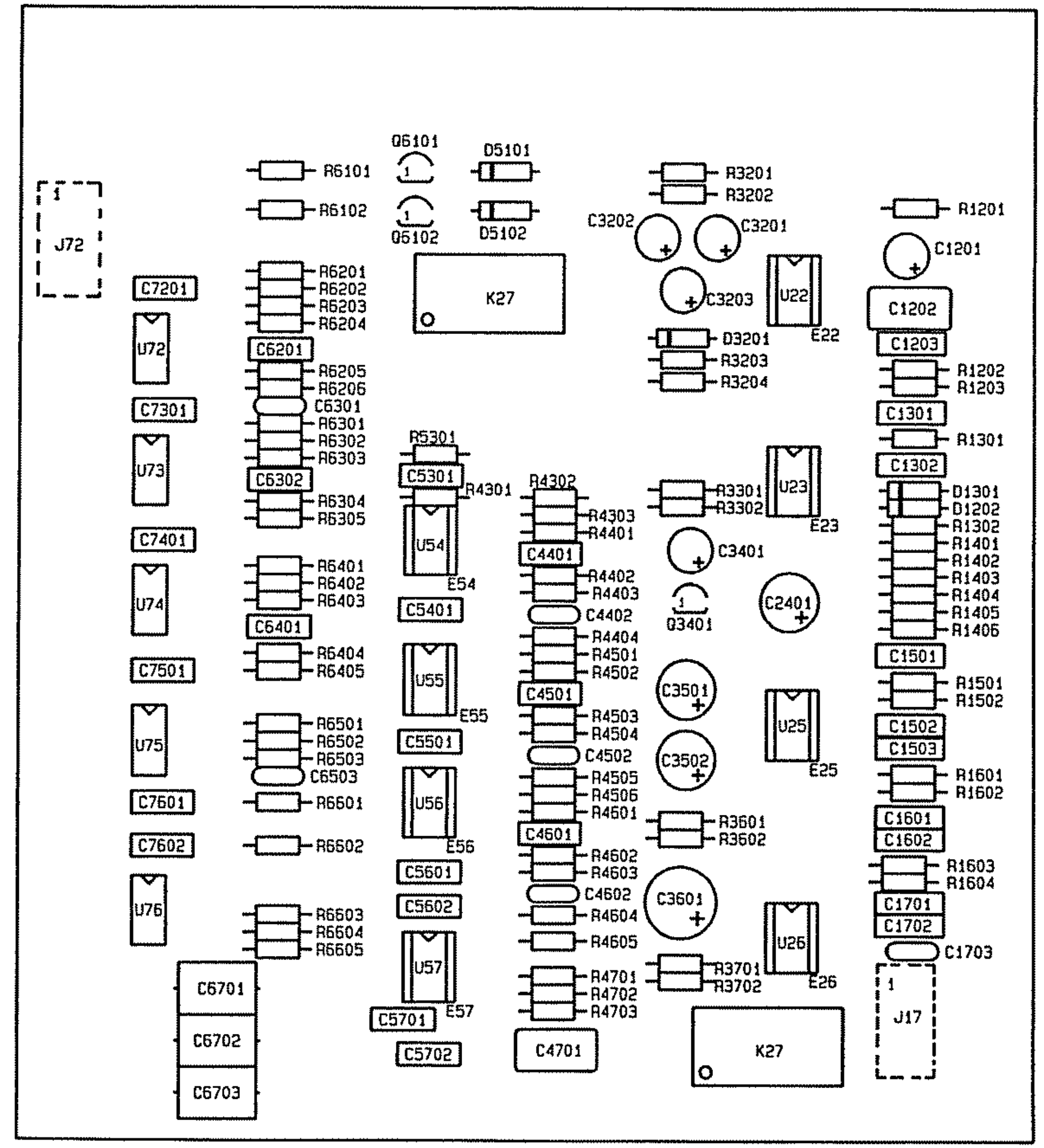
IMD MODE	FILTER MODE	BP/BR TUNING[1]	FREQUENCY COUNTER
SMPTE	BR	1.80 kHz	MAINSIG
CCIF	BP	Diff-Freq	IMFREQ
DIM	BR	180 Hz	MAINSIG

1 *AUTO tuning mode only*

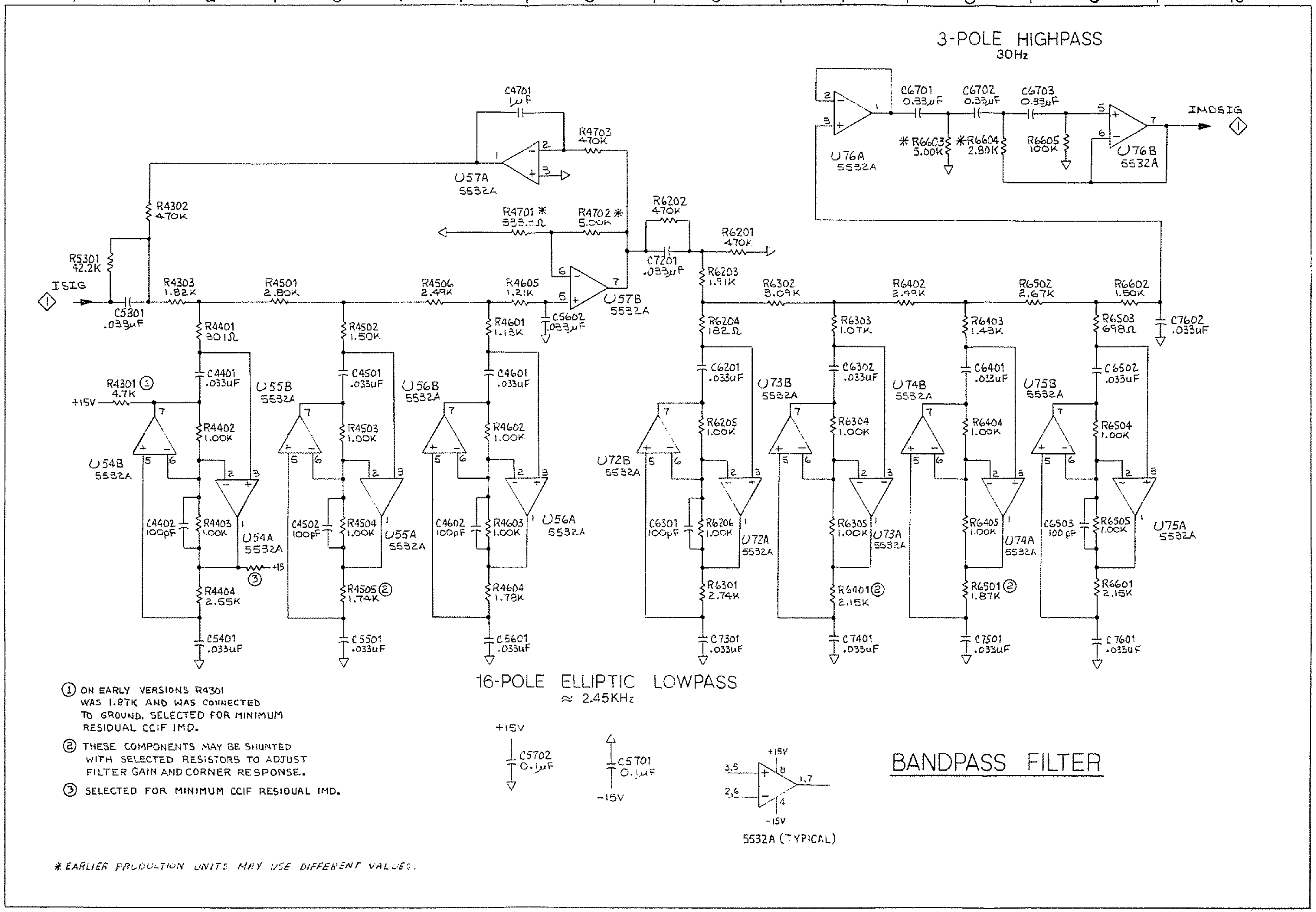
The DIS module tunable bandpass/bandreject filter is also exploited for improved noise performance. With AUTO tuning it is operated as a bandreject at 1.8 kHz in the SMPTE mode to help filter high frequency noise, and as a 180 Hz bandreject in DIM mode to help reject hum products below the lowest expected IMD product. The DIM mode also automatically selects the LVF module 400 Hz highpass filter. In CCIF mode the BP/BR filter is used as a tracking bandpass at the difference frequency.



J17-7 IMAIN
J17-8 IMAOUT
IMOSIG
TO DIS J031
J72-1 VLVL
TO DIS J41
J17-1
J17-2
J17-3
J17-4
J17-5
J17-6 IMFREQ
R3701 2.2Ω
C3601 100µF
R3702 2.2Ω
R3602 100Ω
C3501 47µF
C3502 47µF
R3601 100Ω
C1702 .033µF
C1701 .033µF
C1703 270pF
R1604 1.50K
R1603 3.83K
U26B 5532A
C1602 .033µF
C1601 .033µF
R1602 536
R1601 11.0K
U26A 5532A
C1503 .033µF
C1502 .033µF
R1502 2.15K
R1501 2.67K
U25B 5532A
C1501 .033µF
R1406 2.49K
U25A 5532A
*R1405 475
R1404 2.15K
C3401 1µF
C2401 4.7µF
R3302 10K
R3301 10K
Q3401 PN4091
R3201 4.7K
*R3202 33K
C3202 4.7µF
C3201 1µF
U22A 5532A
C3203 1µF
R3204 40.0K
D3201 1N4152
*R3203 40.0K
U23A 5532A
R1403 4.00K
R1402 2.00K
R1302 2.00K
R1401 2.00K
D1302 1N4152
D1301 1N4152
U23B 5532A
R1301 4.0K
C1301 .033µF
C1302 .033µF
*R1202 4.99K
*R1203 1.00K
C1202 0.33µF
C1203 .033µF
U22B 5532A
C1201 4.7µF
R1201 10K
ISIG
(1) SELECTED FOR Vp ≥ 7.5V
J72-4 +5V
J72-7 IMDA
J72-5 IMDD
J72-3
Q6101 2N2222
R6101 2.7K
K27
D5101 1N4152
*EARLIER PRODUCTION UNIT MAY BE DIFFERENT VALUES.
Q6102 2N2222
R6102 2.7K
K42
D5102 1N4152
LAST ECO# 89014
9IMA.1000
SHT 1 of 2
DATE: 1-8-91



IMD ANALYZER OPTION 9IMA.1000 (6200.IMA1.2)



91MA.1000
SHT 2 of 2
DATE: 1-8-91

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1201	1D8	2942.0475	CAP AL-EL 35V 20%	4.7uF
C1202	1E7	2675.0334	CAP POLYC 100V 2%	.33uF
C1203	1D7	2555.0333	CAP POLYP 50V 2%	.033uF
C1301	1E6	2555.0333	CAP POLYP 50V 2%	.033uF
C1302	1E6	2555.0333	CAP POLYP 50V 2%	.033uF
C1501	1B8	2555.0333	CAP POLYP 50V 2%	.033uF
C1502	1B6	2555.0333	CAP POLYP 50V 2%	.033uF
C1503	1B6	2555.0333	CAP POLYP 50V 2%	.033uF
C1601	1A5	2555.0333	CAP POLYP 50V 2%	.033uF
C1602	1A4	2555.0333	CAP POLYP 50V 2%	.033uF
C1701	1A3	2555.0333	CAP POLYP 50V 2%	.033uF
C1702	1A3	2555.0333	CAP POLYP 50V 2%	.033uF
C1703	1A3	2296.0271	CAP MICA 500V 1%	270pF
C2401	1B8	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3201	1C5	2952.0105	CAP AL-EL 50V 20%	1uF
C3202	1C5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3203	1C6	2952.0105	CAP AL-EL 50V 20%	1uF
C3401	1B8	2952.0105	CAP AL-EL 50V 20%	1uF
C3501	1E1	2932.0476	CAP AL-EL 25V 20%	47uF
C3502	1E2	2932.0476	CAP AL-EL 25V 20%	47uF
C3601	1D2	2952.0107	CAP AL-EL 50V 20%	100uF
C4401	2C2	2555.0333	CAP POLYP 50V 2%	.033uF
C4402	2E2	2296.0101	CAP MICA 500V 1%	100pF
C4501	2C3	2555.0333	CAP POLYP 50V 2%	.033uF
C4502	2E3	2296.0101	CAP MICA 500V 1%	100pF
C4601	2C4	2555.0333	CAP POLYP 50V 2%	.033uF
C4602	2E4	2296.0101	CAP MICA 500V 1%	100pF
C4701	2A4	2454.0105	CAP POLYE 50V 5%	1uF
C5301	2C1	2555.0333	CAP POLYP 50V 2%	.033uF
C5401	2F2	2555.0333	CAP POLYP 50V 2%	.033uF
C5501	2F3	2555.0333	CAP POLYP 50V 2%	.033uF
C5601	2F4	2555.0333	CAP POLYP 50V 2%	.033uF
C5602	2C5	2555.0333	CAP POLYP 50V 2%	.033uF
C5701	2G5	2172.0104	CAP CERAM 100V 20%	.1uF
C5702	2G4	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	2C6	2555.0333	CAP POLYP 50V 2%	.033uF
C6301	2E6	2296.0101	CAP MICA 500V 1%	100pF
C6302	2C7	2555.0333	CAP POLYP 50V 2%	.033uF
C6401	2C8	2555.0333	CAP POLYP 50V 2%	.033uF
C6502	2C9	2555.0333	CAP POLYP 50V 2%	.033uF
C6503	2E9	2296.0101	CAP MICA 500V 1%	100pF
C6701	2A8	2675.0334	CAP POLYC 100V 2%	.33uF
C6702	2A8	2675.0334	CAP POLYC 100V 2%	.33uF
C6703	2A9	2675.0334	CAP POLYC 100V 2%	.33uF
C7201	2B6	2555.0333	CAP POLYP 50V 2%	.033uF
C7301	2F6	2555.0333	CAP POLYP 50V 2%	.033uF
C7401	2F7	2555.0333	CAP POLYP 50V 2%	.033uF
C7501	2F8	2555.0333	CAP POLYP 50V 2%	.033uF
C7601	2F9	2555.0333	CAP POLYP 50V 2%	.033uF
C7602	2C10	2555.0333	CAP POLYP 50V 2%	.033uF
D1301	1E5	3110.4152	DIODE SIGNAL	4152

REPLACEABLE ELECTRICAL PARTS LIST: 9IMA.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
D1302	1E4	3110.4152	DIODE SIGNAL	4152
D3201	1C6	3110.4152	DIODE SIGNAL	4152
D5101	1G2	3110.4152	DIODE SIGNAL	4152
D5102	1G9	3110.4152	DIODE SIGNAL	4152
J17	1A1	4221.1008	JACK PC 2 X .1	8 PIN
J72	1C1,1G1	4221.1008	JACK PC 2 X .1	8 PIN
K27	1G2	4530.0002	RELAY PC LOW POWER	DPDT
K42	1G10	4530.0002	RELAY PC LOW POWER	DPDT
P17	---	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P72	---	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
Q3401	1C8	3214.4091.H	XSTR FET TO92 HI Vp	PN4091
Q6101	1G2	3211.2222	XSTR NPN TO92	PN2222A
Q6102	1G9	3211.2222	XSTR NPN TO92	PN2222A
R1201	1E8	1214.0103	RES 1/4W C FLM 5%	10K
R1202	1D6	1136.4991	RES 1/8W M FLM 1%	4.99K
R1203	1D7	1139.1001	RES 1/8W M FLM .1%	1.00K
R1301	1E6	1139.4001	RES 1/8W M FLM .1%	4.00K
R1302	1E5	1139.2001	RES 1/8W M FLM .1%	2.00K
R1401	1E5	1139.2001	RES 1/8W M FLM .1%	2.00K
R1402	1E4	1139.2001	RES 1/8W M FLM .1%	2.00K
R1403	1D4	1139.4001	RES 1/8W M FLM .1%	4.00K
R1404	1B9	1136.2151	RES 1/8W M FLM 1%	2.15K
R1405	1B8	1136.4750	RES 1/8W M FLM 1%	475
R1406	1B8	1136.2491	RES 1/8W M FLM 1%	2.49K
R1501	1B7	1136.2671	RES 1/8W M FLM 1%	2.67K
R1502	1B6	1136.2151	RES 1/8W M FLM 1%	2.15K
R1601	1B5	1136.1102	RES 1/8W M FLM 1%	11.0K
R1602	1B5	1136.5360	RES 1/8W M FLM 1%	536
R1603	1A3	1136.3831	RES 1/8W M FLM 1%	3.83K
R1604	1A3	1136.1501	RES 1/8W M FLM 1%	1.50K
R3201	1C4	1214.0472	RES 1/4W C FLM 5%	4.7K
R3202	1C5	1214.0333	RES 1/4W C FLM 5%	33K
R3203	1D6	1139.4002	RES 1/8W M FLM .1%	40.0K
R3204	1C6	1139.4002	RES 1/8W M FLM .1%	40.0K
R3301	1C7	1214.0103	RES 1/4W C FLM 5%	10K
R3302	1B8	1214.0103	RES 1/4W C FLM 5%	10K
R3601	1E2	1214.0101	RES 1/4W C FLM 5%	100
R3602	1E1	1214.0101	RES 1/4W C FLM 5%	100
R3701	1D1	1214.0229	RES 1/4W C FLM 5%	2.2
R3702	1D1	1214.0229	RES 1/4W C FLM 5%	2.2
R4301	2D1	1214.0472	RES 1/4W C FLM 5%	4.7K
R4302	2B2	1214.0474	RES 1/4W C FLM 5%	470K
R4303	2C2	1136.1821	RES 1/8W M FLM 1%	1.82K
R4401	2C2	1136.3010	RES 1/8W M FLM 1%	301
R4402	2D2	1139.1001	RES 1/8W M FLM .1%	1.00K
R4403	2E2	1139.1001	RES 1/8W M FLM .1%	1.00K
R4404	2E2	1136.2551	RES 1/8W M FLM 1%	2.55K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4501	2C3	1136.2801	RES 1/8W M FLM 1%	2.80K
R4502	2C3	1136.1501	RES 1/8W M FLM 1%	1.50K
R4503	2D3	1139.1001	RES 1/8W M FLM .1%	1.00K
R4504	2E3	1139.1001	RES 1/8W M FLM .1%	1.00K
R4505	2E3	1136.1741	RES 1/8W M FLM 1%	1.74K
R4506	2C4	1136.2491	RES 1/8W M FLM 1%	2.49K
R4601	2C4	1136.1131	RES 1/8W M FLM 1%	1.13K
R4602	2D4	1139.1001	RES 1/8W M FLM .1%	1.00K
R4603	2E4	1139.1001	RES 1/8W M FLM .1%	1.00K
R4604	2E4	1136.1781	RES 1/8W M FLM 1%	1.78K
R4605	2C4	1136.1211	RES 1/8W M FLM 1%	1.21K
R4701	2B4	1139.3330	RES 1/8W M FLM .1%	333.3
R4702	2B5	1139.5001	RES 1/8W M FLM .1%	5.00K
R4703	2B5	1214.0474	RES 1/4W C FLM 5%	470K
R5301	2C1	1136.4222	RES 1/8W M FLM 1%	42.2K
R6101	1G1	1214.0272	RES 1/4W C FLM 5%	2.7K
R6102	1G9	1214.0272	RES 1/4W C FLM 5%	2.7K
R6201	2B6	1214.0474	RES 1/4W C FLM 5%	470K
R6202	2B6	1214.0474	RES 1/4W C FLM 5%	470K
R6203	2C6	1136.1911	RES 1/8W M FLM 1%	1.91K
R6204	2C6	1136.1820	RES 1/8W M FLM 1%	182
R6205	2D6	1139.1001	RES 1/8W M FLM .1%	1.00K
R6206	2E6	1139.1001	RES 1/8W M FLM .1%	1.00K
R6301	2E6	1136.2741	RES 1/8W M FLM 1%	2.74K
R6302	2C6	1136.3091	RES 1/8W M FLM 1%	3.09K
R6303	2C7	1136.1071	RES 1/8W M FLM 1%	1.07K
R6304	2D7	1139.1001	RES 1/8W M FLM .1%	1.00K
R6305	2E7	1139.1001	RES 1/8W M FLM .1%	1.00K
R6401	2E7	1136.2151	RES 1/8W M FLM 1%	2.15K
R6402	2C7	1136.2491	RES 1/8W M FLM 1%	2.49K
R6403	2C8	1136.1431	RES 1/8W M FLM 1%	1.43K
R6404	2D8	1139.1001	RES 1/8W M FLM .1%	1.00K
R6405	2E8	1139.1001	RES 1/8W M FLM .1%	1.00K
R6501	2E8	1136.1871	RES 1/8W M FLM 1%	1.87K
R6502	2C9	1136.2671	RES 1/8W M FLM 1%	2.67K
R6503	2C9	1136.6980	RES 1/8W M FLM 1%	698
R6504	2D9	1139.1001	RES 1/8W M FLM .1%	1.00K
R6505	2E9	1139.1001	RES 1/8W M FLM .1%	1.00K
R6601	2E9	1136.2151	RES 1/8W M FLM 1%	2.15K
R6602	2C9	1136.1501	RES 1/8W M FLM 1%	1.50K
R6603	2B8	1139.5001	RES 1/8W M FLM .1%	5.00K
R6604	2B8	1136.2801	RES 1/8W M FLM 1%	2.80K
R6605	2B9	1136.1003	RES 1/8W M FLM 1%	100K
U22	1C6,1D8	3412.5532	OP AMP DUAL	5532
U23	1D5,1E4	3412.5532	OP AMP DUAL	5532
U25	1A8,1B7	3412.5532	OP AMP DUAL	5532
U26	1A4,1A5	3412.5532	OP AMP DUAL	5532
U54	2D2	3412.5532	OP AMP DUAL	5532
U55	2D3	3412.5532	OP AMP DUAL	5532
U56	2D4	3412.5532	OP AMP DUAL	5532
U57	2B4,2C5	3412.5532	OP AMP DUAL	5532

REPLACEABLE ELECTRICAL PARTS LIST: 9IMA.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U72	2D6	3412.5532	OP AMP DUAL	5532
U73	2D7	3412.5532	OP AMP DUAL	5532
U74	2D8	3412.5532	OP AMP DUAL	5532
U75	2D9	3412.5532	OP AMP DUAL	5532
U76	2A7,2B9	3412.5532	OP AMP DUAL	5532

Audio precision

SYSTEM ONE

SERVICE MANUAL

Volume 2 of 2

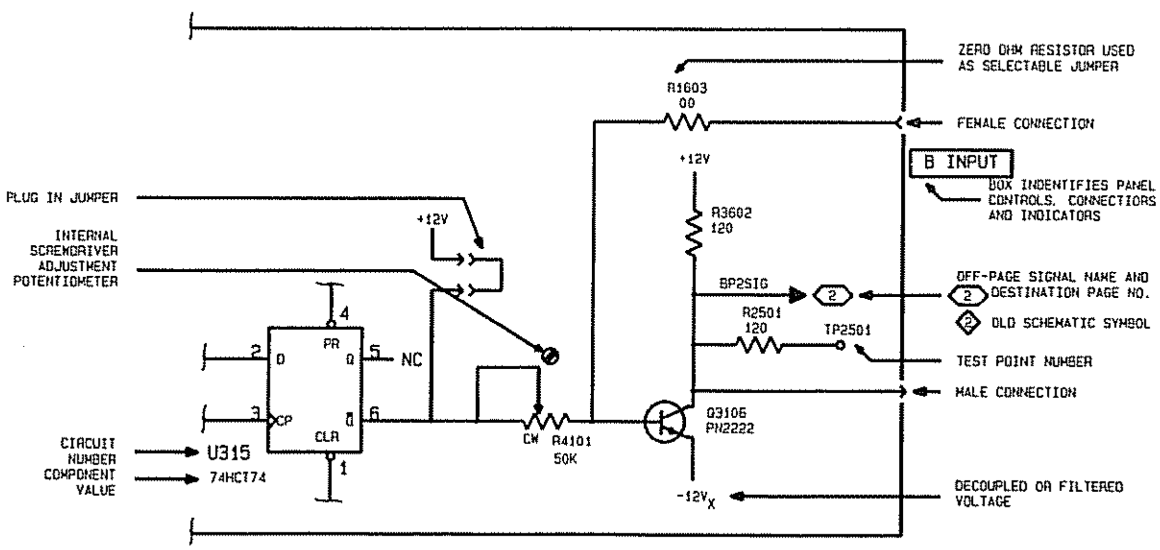
SECTION 4
SYSTEM ONE CIRCUIT DESCRIPTIONS, SCHEMATICS, & ELECTRICAL PARTS LISTS

This section contains schematics, circuit descriptions, and electrical parts lists for the System One. All information is believed to be accurate as of the publication date, however Audio Precision reserves the right to make changes without prior notice. If a component value differs from that shown on the schematics use the value of the existing component for replacement purposes, or contact Audio Precision.

COMPONENT AND ASSEMBLY DESIGNATIONS

A	Assembly
BT	Battery
C	Capacitor, fixed or variable
D	Diode
E	Socket or mechanical part
F	Fuse
H	Heat sink or radiator
HS	Heatsink or mounting hardware
J	Connector, female
K	Relay
L	Inductor, fixed or variable
P	Connector, male
Q	Transistor, FET, or SCR
R	Resistor, fixed or variable
S	Switch or contact
TP	Test Point
U	Integrated Circuit
W	Wirestrap or Cable
X	Transformer
Y	Crystal

SPECIAL SCHEMATIC SYMBOLS



DSP-1

DIGITAL SIGNAL PROCESSING MODULE

DSP-1, DIGITAL SIGNAL PROCESSING MODULE

NOTE: There have been two versions of the DSP module. The version can be determined from the production code number located on the decal attached to the metal shield. The code number will have the format "DSPx-yyyyy-zz" where "x" is the DSP version.

Introduction

The DSP-1 module, diagrammed in Figure DSP1.1, provides a "dsp" (digital signal processor) core with both analog and digital input and output capabilities. The system is built around three digital signal processors, one for the dsp core functions, one for the analog interface and one for the digital interface. The dsp core and the analog input and output circuitry are on one circuit board. It normally occupies the compartment underneath the analog generator module in a System One. The DSP-1 module itself provides analog signal generation and measurement using on board D/A and A/D converters. In SYS-322 and SYS-302 configurations the DIO module adds additional memory and digital input and output functions. In SYS-222 and SYS-202 configurations the MEM option board provides additional memory only.

The Audio Precision System One provides all commonly used analog audio test and measurement functions. The DSP-1 module expands these functions into the digital audio domain, as well as enhancing the operation of the system for analog measurements. The digital signal processing can be used in conjunction with the System One analog notch filter to measure analog signals to a much wider dynamic range. For example the analog hardware can be used to remove the fundamental in a THD measurement and the dsp may then measure the harmonics individually, with a dynamic range far in excess of its A/D converters capabilities.

All dsp chips in the system are Motorola DSP56001 24-bit digital signal processors operating at 24.576 MHz. The manufacturer's block diagram is reproduced in Figure DSP1.2. It uses a 6-bus architecture for internal processing, providing separate address and data busses for program memory, and for two data memories. On chip resources include two 256-word data memories, a 256 point sine table, 512 words of zero wait state program memory, 24-bit serial inputs and outputs, an 8-bit host interface, interrupt controller with two external interrupts, a 24x24 multiplier and an ALU which supports double precision operations. A single external address and data bus are provided for expanding program or data memory size off chip.

The external busses of all three processors are tied together on the same expansion memory. A bus arbitrator controls access to the shared resources and prevents conflicts. Program memory is expanded to 8k words of 0 wait state static RAM and is used by the main dsp only. The other two dsps rely completely on their internal 512 word program memory. The DSP-1 board provides 32k words of additional static data RAM, split equally between X and Y data memory spaces. The DIO board adds another 64k words of static data RAM, again split equally between X and Y memory. The DSP-1 board also contains a hardware random number generator and simple real time clock. The data RAM and peripherals are available for use by all processors. Only the main and decimator dsps can communicate directly with the host personal computer.

A single ROM contains the program code which fills the internal program memory of all three processors. Each processor reads its respective portion of the ROM when released from reset and fills internal program memory. The main dsp can then communicate with the host computer to download larger programs into external program RAM as well as modifying its own internal RAM. This ROM also contains serial number information and calibration constants. The calibration information eliminates the need for offset or gain adjustments in the A/D converters.

The decimator dsp receives signals from two on board A/D converters and decimates the data to lower sampling rates. The A/D's always run at a 192 kilosample rate or a 176.4 kilosample rate. The decimator reduces these rates to 48 kHz, 44.1 kHz or 32 kHz for compatibility with professional audio sampling rates. This allows compatibility with all professional and consumer digital audio sampling rates. The decimator can also provide 8 kHz and 1 kHz sample rates for use when measuring very low frequency signals. Analog signals from the various portions of the System One analog measurement modules or from dedicated front panel inputs are routed to the anti-alias filters by CMOS switch selectors. The filters are designed to remove energy above 80 kHz before feeding the A/D converters. The converters are dithered by an analog output from the same random number generator which supplies the dsps with digital dither. After filtering, the decimator dsp passes its data serially to the main dsp for further processing.

In SYS-322 and SYS-302 configurations the third dsp processor located on the DIO board is used for AES/EBU communications. Data encoding, decoding, synchronization, parity checking, and extracting the serial status bit stream are accomplished by dedicated logic circuits. However, complete implementation of the AES/EBU interface requires the ability to write and read quite a few status bits in real time. These bits provide sample counts, pre-emphasis flags, channel allocation information, source and destination codes, etc. Additionally, it is necessary to send and receive pre-emphasized data.

The DIO board also contains parallel input and output ports for connection to external test circuits and dsp devices. Each port multiplexes two channels of data onto one set of 24 data lines. Each output channel is buffered by a two stage FIFO to prevent jitter in the transmitted data. Each input channel consists of latches which are written by the external device and read by the main dsp. A sample clock generator is provided to strobe the data inputs and outputs or an external clock may be used for either or both functions. The internal sample clock generator may be programmed for a variety of digital audio rates. Appropriate hardware generates interrupts for the processor when data is read from the output or received at the input.

The digital interface circuits, either AES/EBU or parallel, serve the same function as the balancing amplifiers in an analog system. They provide an interface between the format of the device under test and the internal hardware of the test equipment. They also double buffer data to allow for timing differences between the two pieces of equipment.

PC/Host Computer Interface <1>

Power, address and data from the System One mainframe enters on connector P492. The data bus from the System One interface is buffered by tri-state transceiver U790. The same signal which enables U790 is used to drive the wired-OR attention feature of the System One interface through D2901. Resistor network R7901 prevents the host data bus from drifting to intermediate logic levels when it is tri-stated, reducing power consumption.

The DSP-1 module occupies module address 3 on the System One interface. Each System One module address has associated with it 16 individual data addresses. The upper four bits of the eight bit address bus are used to decode the module address. The lower four address bits are used to select one of 16 addresses on the board. These addresses are decoded by U290.

Reset generator U280 provides the power up reset signal to the processors and guards the EEROM memory against writes during power-up and power-down cycles. If the +5 Volt power supply drops below 4.75 Volts the open collector output (/PWRFAIL) on pin 5 will go low, clearing octal latch U691. The PROTECT signal on pin 6 is an open collector pnp transistor output which simultaneously goes high. This is used to clamp the write enable pin of EEROM U380, preventing accidental modification of its contents. The mainframe reset signal /RST on connector P492 is combined with the supply voltage sensing to also force reset when it is asserted low.

The host data bus drives dual port register files U490, U590, and U690 and latch U691. Latch U691 is used to reset the dsps and bring them out of reset under control of the host computer. The lower two bits drive the reset lines of the two dsps on the DSP-1 board. The third bit resets the dsp on the DIO board in SYS-322/SYS-302 configurations.

The three register files are used to hold data from the dsps which can be read by the host computer to indicate when new readings are available. U590 and U690 are written to as 4 bit words by the dsp and are read as bytes by the host. To allow dsp read-modify-write instructions to be used on this data, U490 provides a read back function of the data written to either U590 or U690. When one of the processors writes to the register files flip-flop U390 is clocked low, asserting the open collector RDG line. When the host reads one of the register files the flip-flop is set, releasing the RDG line. All remaining communication between the host and the processors is accomplished through their host port interfaces.

The main processor U680 and the decimator processor U670 host ports (shown on schematic <2>) normally occupy 8 addresses each. U290 maps the main processor U680 into the lower 8 board addresses and the decimator processor into the upper 8. Pin 15 of U290 drives the main processor host port enable (/HEN), while pin 19 drives the decimator processor host port enable (/DHEN). Pin 16 provides a read/write signal for both processors (HR/W). The decoder U290 also maps other hardware functions on top of unused addresses in the processor host ports. The address map in TABLE 1 details this board address allocation. A special host port mode, used for dma transfers, is selected by the /HACK inputs of the processors. This is also decoded in U290.

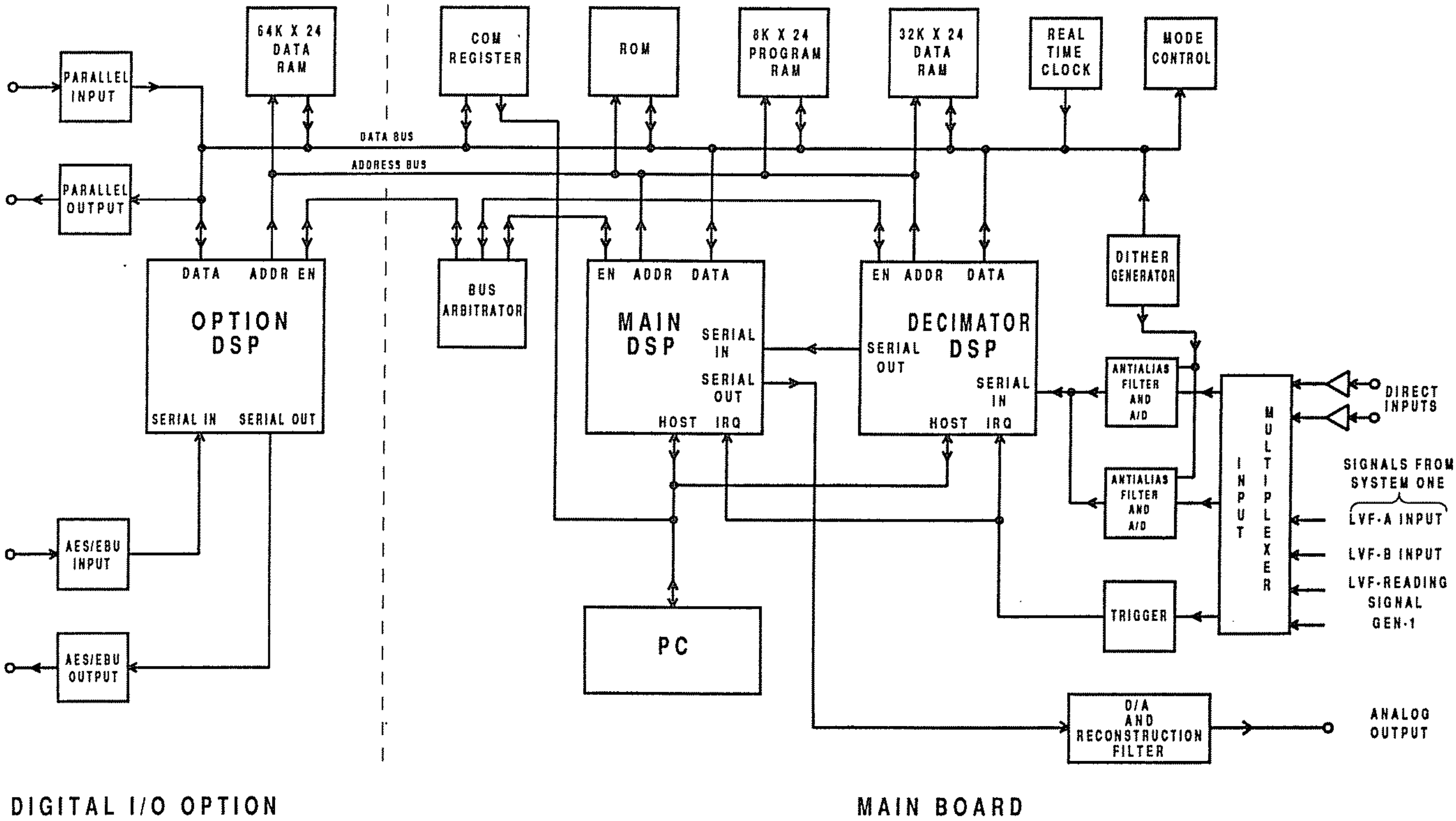


Figure DSP1.1 DSP-1 BLOCK DIAGRAM

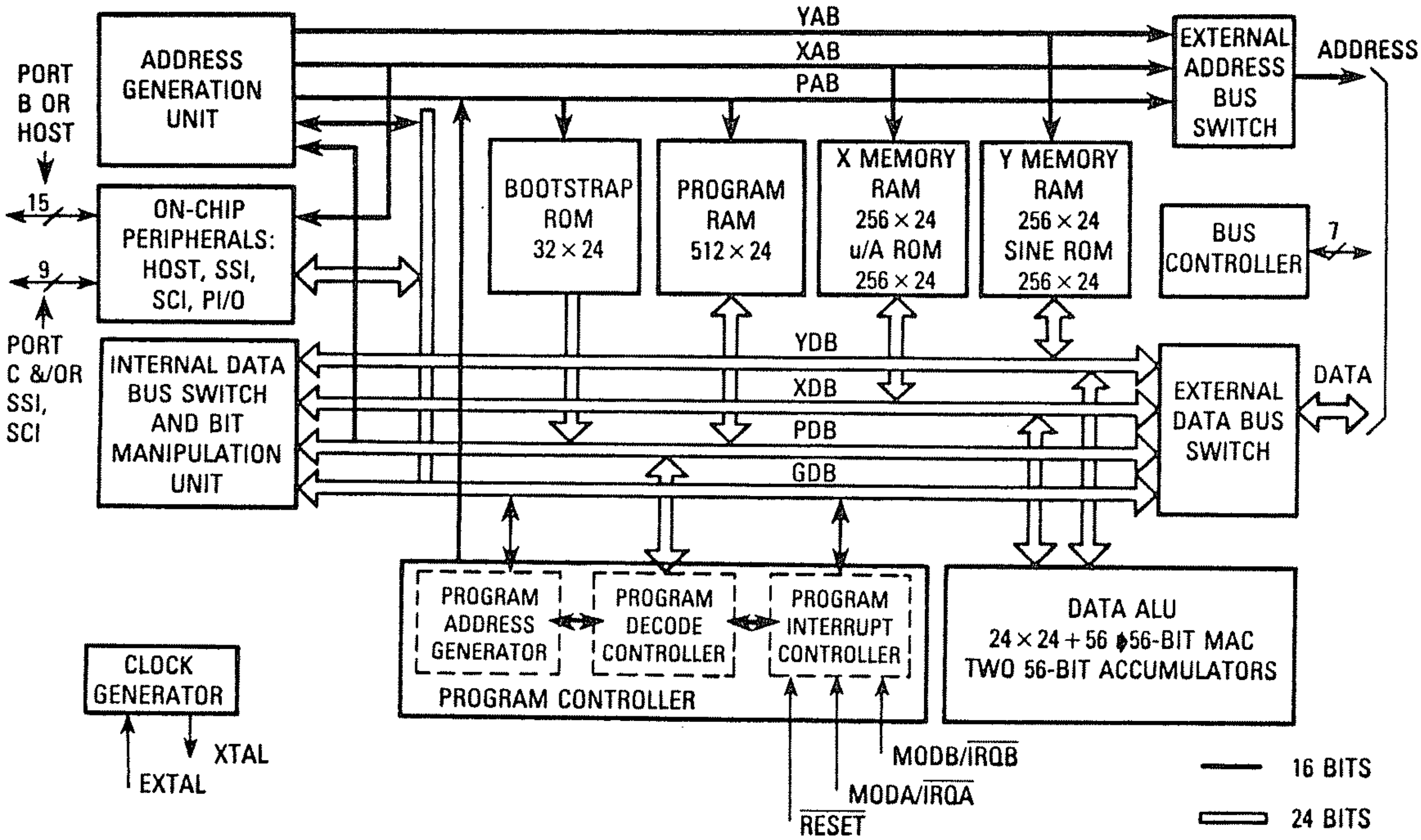


Figure DSP1.2 DSP56001 BLOCK DIAGRAM

Low Voltage Power Supplies <1>

The ±15 Volt supplies are regulated down to ±6 Volts by U150 and U151. Diodes D1502 and D1503 provide reverse voltage protection. Capacitors C1602 and C1601 bypass the 15 Volt supplies and insure low inductance supply inputs. Resistor dividers R1502/R1503 and R1504/R1505 set the output voltages to approximately 5.8 volts. Output bypass capacitors C1501 and C1502 reduce the supply impedances at high frequencies. Capacitor C1402 and C1410 reduce output noise on the negative supply, a critical parameter for the D/A converters. Diode D1504 prevents damage to the regulator during power down.

Processors and Bus Arbitration <2>

The dsp data bus is buffered by tri-state octal transceivers U370, U361 and U360. Programmable logic device U860 arbitrates between the three processors for access to the common address and data bus. Each processor has three pins dedicated to bus arbitration; bus request out (/BUSREQ#), bus enable in (BUSEN#) and bus grant out (/BUSGT#) where # represents the processor number. The bus request output pin is pulled low by the processor to signal the arbitrator that access is needed. The bus enable input is driven high by the arbitrator to allow access to the bus. The bus grant output goes low to signal that bus access is given up. The arbitrator normally examines the state of each bus request and bus grant to determine which processor needs the bus and which currently has the bus. However when the memory select bits MEM1 and MEM0 are asserted during boot from EEROM they force the arbitrator to give access to the appropriate processor regardless of the bus request signal states. During normal operation the bus access priority is set by the three bits PTY2, PTY1, and PTY0 from U640 on schematic <4>. When a processor with higher priority than the one currently using the bus requests bus access the arbitrator takes access away from the current user. After the current user has released the bus, the arbitrator gives the bus to the highest priority requestor. Arbitrator pin 21 is asserted when the bus is idle (no processors currently given access). This state should occur for one clock cycle between any change in bus access. Pin 22 is asserted if any two or three processors claim access at the same time, representing an error condition.

Memory and Address Decode <3>

The address bus is buffered by U660 and U661, shown on schematic <3>. The unbuffered data lines drive the RAMs on the DSP-1 board and are extended through connector J96 to the optional DIO or MEM boards. These RAMs consist of one bank of three 8k-by-8 program memories U362, U371 and U381 and one bank of three 32k-by-8 data memories U460, U470, and U480. The RAM address lines are all driven from the buffered address bus. The lower 13 buffered address lines drive the program RAMs directly, the lower 14 lines are used to drive the data RAMs. The most significant bit of the data RAM address is derived from the X/Y memory select line. Programmable array logic chip U760 acts as a very high speed address decoder. The upper 8 unbuffered address lines and some of the lower address lines are used to decode the various memory enable signals and the buffer enable signals. The enable for the I/O buffers is further decoded by U651 and U751 to create individual enable signals for the I/O devices on the DSP-1 board. U651 decodes read operations while U751 decodes write operations.

EEROM U380 contains the boot code for each of the three processors. It is enabled by address decoder U642. The lower 11 buffered address lines directly drive the lower 11 address inputs of the ROM. The two most significant ROM address lines pass through two sections of exclusive OR U281. The other inputs of the exclusive OR come from latch U691 under control of the host computer. This allows the host to map any one of four pieces of the EEROM to the base address ($C000) used by the dsp processors when they boot. These two memory select lines are also used to drive the bus priority logic, described later, giving control of memory to the processor being brought out of reset. The eight data lines of the EEROM are connected to buffered data lines D0 through D7. The processor automatically reads three consecutive addresses from the ROM, starting at $C000, and uses these bytes to fill one location of internal program RAM. This is repeated at succeeding ROM addresses until internal program memory is filled. The processor then begins executing the code loaded into internal memory. After the processors are operational, the host computer may load additional memory locations as required.

Random Number Generator <4>

Programmable logic device U451 and shift registers U440, U442 and U450 form a maximum length pseudo-random number generator. This is used to generate uniformly distributed random numbers for use in digital dither and to provide analog dither to the A/D converters. U451 contains a 7-bit shift register and a multiple input exclusive NOR gate to provide feedback. Shift registers U440 and U442 are cascaded with the internal shift register to lengthen the sequence to 23 bits. Shift register U450 shadows the data in U451s internal flip flops. The generated data is latched by additional latches in U440, U442 and U450 when /BRD goes high to guarantee that the data does not change during a read operation. The outputs are tri-stated until /RNDRD is asserted low during a read from the generator. A tri-state buffer in U451 copies the most significant bit from U450 and outputs it into the sign bit of the data word. This guarantees that the random values are always between ±0.5. The /RNDRST signal resets the shift registers to guarantee startup on power up or to allow restarting under program control. One of the shift register outputs is gated by transistor Q4501 and filtered by U641 (located on schematic <10>) to produce an analog dither signal for the A/D converters. The /DITHER signal shuts this analog dither down when asserted high.

DIS Signal Monitor <4>

The 16-bit value used to program the tuning DACs on the DIS module is routed through a cable via P25. Also on this cable are four signals from the 6805 microprocessor on the LVF module which indicate when an change in level range occurs. Octal tri-state inverting buffers U341 and U350 buffer the bandpass/notch filter frequency and compensate for the complemented data format in the DIS mdacs. Half of octal buffer U242 buffers the four range-change indication signals. Read enable signal /DISFREQ activates all three buffers when low, placing the data on the bus.

Mode and MUX Control <4>

Octal latch U640 latches bus priority and sample rate control bits. It is strobed by /MEMW when the processor performs a write operation to the appropriate memory location. These latches may be read back by the processor when a read is performed from the same address. This readback is enabled by /MEMR.

Octal latches U540 and U541 latch input and trigger selection control bits. Also included on latch U541 are the data memory page control and the dither enable signals. They are strobed by /MODE when the processor performs a write operation to the appropriate memory location. These latches may be read back by the processor when a read is performed from the same address. This readback is enabled by /MODR.

Read-modify-write instructions are used by the processors to set the latches. Any failure of the readback function may cause bad data to be written into the defective latch.

Status Bits <4>

Octal buffer U340 monitors various status bits on the DSP board. Bits 0 and 1 monitor the bus request activity of the main and decimator processors respectively so that the processor in control of the bus may check to see if other access is requested. A high level on bit 2 indicates that the host computer has routed the D/A converter output through the analog generator. This is used to override the digital output level and resolution if necessary. The trigger signal is available on bit 3 for the processor to use in programs as required.

The YRAM signal on bit 4 is used to determine the presence or absence of an option board. The buffer may be read from either of two addresses, one odd and one even. A resistor from the lowest buffered address line is used to pull the input high or low, depending on the address accessed. If a read from the odd address finds the bit high and a read from the even address finds it low there is no option board present. If a read from either address finds the bit high, the MEM option is present. If a read from either address finds the bit low, the DIO module is present.

Bits 5 and 6 monitor the memory selection bits MEM0 and MEM1 to let the processors know when the boot process is finished and the EEROM is returned to its natural addressing mode. Bit 7 is used to monitor the sync signal from the analog generator.

Clock Generation <5>

Crystal oscillator Y85 provides the master clock for the DSP-1 and DIO modules. It oscillates at 24.576 MHz, driving three sections of U850 through C7501. One section drives the dsp processor master clock inputs, one drives the processor on the DIO board and the third clocks all remaining synchronous logic. Potentiometer R8402 and R8403 adjust the bias at the input of the buffers to obtain a 50% duty cycle at the processor clock inputs.

Interrupt Selection <5>

The processors each have only two hardware interrupt inputs. Programmable logic chip U650 is used to select between the available interrupt sources. Octal latch U550 latches interrupt selection information for both processors on the DSP board. It is strobed by /IRQW when the processor performs a write operation to the appropriate memory location. This latch may be read back by the processor when a read is performed from the same address. This readback is enabled by /IRQR. Read-modify-write instructions are used by the processors to set the latches. Any failure of the readback function may cause bad data to be written into the defective latch.

The lowest two bits of the latch select the main processor (U680) input data interrupt source (IRQA). The next two bits of the latch select the main processor (U680) output data interrupt source (IRQB). The trigger interrupt is also combined with the output data interrupt selection. The next two bits of the latch select the decimator processor (U670) input data interrupt source (IRQA). The top two bits of the latch select the decimator processor (U670) output data interrupt source (IRQB). The trigger interrupt is also combined with the output data interrupt selection.

One section of NAND gate U850 combines the main and decimator reset signals, causing selector U650 to tri-state its outputs when either is asserted low. When this occurs the interrupt inputs are driven through resistors R6403-R6406 from the MODE0 and MODE1 bits of U691. The processor latches the levels on its interrupt inputs as it exits reset and uses the two bit value to select the memory map and reset vector. This allows the host computer to control the memory mode of each processor as they exit reset.

Trigger Comparator <5>

The trigger signal is routed to one half of comparator U840. Resistor R6408 and capacitor C6403 eliminate high frequency noise from the signal, preventing false transitions at the output of U840. R7405 and R7402 introduce hysteresis to prevent oscillations at the output of U840 when operating with low frequency inputs. R7404 and R7403 offset the hysteresis when using the opposite signal edge to insure triggering at zero crossings. The trigger invert bit TRIG_INV causes U650 to invert the trigger signal before passing it to the processor interrupt input.

Sync Output Comparator <5>

The second section of U840 is used to create a sync signal when the D/A output is routed through the analog generator. Resistor R8305 and capacitor C7305 eliminate high frequency noise from the signal, preventing false transitions at the output of U840. R8306 and R6407 introduce hysteresis to prevent oscillations at the output of U840 when operating with low frequency inputs. By setting SYNC_EN high the comparator positive input will be held high and the output will be shut down. Since the output is open collector, when this occurs diode D7401 allows the processor to drive the sync output directly. This is used if the sync signal must follow the waveform envelope rather than its zero crossings. The sync signal is sent to the GEN module via P84.

Trigger Time Comparator <5>

8-bit counters U443 and U441 latch the time between a trigger event and the last sample interrupt. C4403, D4401 and R4401 form a one shot which clears the counters at each sample interval. The next input interrupt signal edge is inverted and used to latch the count in the counters. The counter outputs are enabled by /CNTRD going low, placing the count on the lowest 16 bits of the bus.

D/A Converter <6>

The digital audio signal from the main processors serial output port drives the programmable logic chip U180 and digital filter U190. Part of U180 selects between the input and output of the digital filter. When operating at standard digital audio sample rates of 32 kHz, 44.1 kHz, or 48 kHz the data is passed through the digital filter and oversampled by a factor of 8. When operating at a sample rate of 176.4 kHz or 192 kHz, the data is passed directly to the converters and does not pass through the digital filter. The master clock to run the digital filter must be a prescribed multiple of the input sample rate. The clock is applied at pin 6 of U190 and is derived from the PCLOCK signal on U841 pin 15 when the sample rate is derived from the internal crystal oscillators. The PCLOCK signal is 256 times the 44.1 kHz or 48 kHz sample rates. When operating at 32 kHz sample rates the PCLOCK signal is a 384 times clock. Pins 3 and 4 of U190 set the clock ratio for the filter. When pin 3 is high and pin 4 is low the filter will operate with a 384 times clock. When pin 3 is low and pin 4 is high the filter will operate with a 256 times clock. If the D/A signal is derived from the DIO option board the clock will always be 256 times the sample rate. This is sent down from the option board as OPTMCLK (pin 7) and is selected inside U180 when the MAIN/OPT bit (pin 13) goes low.

The digital filter has internal registers which must be programmed to set the operating mode of the chip. This is performed immediately after reset by a serial data word applied to pin 13 of the filter by BD0. This data word is clocked into the filter by /DACM. Buffered address lines BA0 and BA1 select which internal register is to be programmed.

The output of the selector is applied to D/A converters U240 and U241. They each handle one channel of data but their outputs are combined into a single channel by U130 before passing to the analog reconstruction filter.

The converter power supplies are heavily bypassed and decoupled to reduce noise pickup. Potentiometers R2306 and R2305 adjust the MSB scale factor to trim the converters for minimum distortion.

DAC Reconstruction Filter <7>

The DAC reconstruction filter is an analog lowpass filter used to smooth the D/A converter output. It is a "FDNR" (Frequency Dependent Negative Resistance) ladder filter as are the A/D antialias filters. A conventional LC ladder filter consists of series arms which are inductors and shunt arms which are capacitors. As the signal frequency increases, the series inductor impedance increases and the shunt capacitor impedance decreases. Above the corner frequency of the filter the attenuation rises rapidly, reducing out of band signals at the filter output. A FDNR ladder filter may be thought of as an LC lowpass ladder filter in which each inductor has been replaced by a resistor and each capacitor has been replaced by a FDNR element. Using this transformation, resistors in the original filter become capacitors in the transformed filter. Its impedance decreases with frequency twice as fast as a conventional capacitor. This doubly sharp shunt impedance, in combination with the fixed impedance in the series arms of the filter produces the same rolloff as the original LC filter.

The input signal is applied to the filter at C1301 and R1311. R1311 and R1307 provide a dc bias current path for U231, U230, U221, and U220. C1301 and C2207 are the source and load capacitances respectively. They are ratio matched to within .1% because their ratio directly determines the passband gain of the filter. R1308, R2303, R1301, and R2203 are the series elements of the ladder. R1310, U231, C2307, R2304, R1306, R1305 and C2305 comprise the first FDNR element, shunting the node between R1308 and R2303 to ground. Similarly, R2302, U230, C2306, R1304, C2210, R1303, R1302 and C2301 form the second FDNR element shunting the next node of the ladder. C2303 and C2304 parallel C2301 in the de-energized state of relay K220, reducing its resonant frequency for use in the 20 kHz lowpass circuit. R1207, U221, C2206, R1210, R1209, R1208, C2208 comprise the third and final FDNR. R2202 and R1206 are the main gain setting resistors for buffer U220, providing a gain of 2 to compensate for the loss in the ladder network. R1203 and C2203 provide mid-band flatness compensation, and R2301 provides offset compensation.

Relay K220 is activated in when the 192 kHz or 176.4 kHz sample rates are selected. This sets the filter to an elliptic lowpass response with a corner frequency of 80 kHz. When the relay is de-energized the filter is changed to a 20 kHz lowpass for use with the 48 kHz, 44.1 kHz and 32 kHz sample rates. U220A, R2202, C2204, C2205 and R1205 provide sinX/X compensation for the high sample rates. Clamp diodes D2103 and D2104 prevent damage to the CMOS input and trigger multiplexers. The front panel DAC output bnc is driven with this signal through R1201. The signal to the analog generator module is highpass filtered by U220B, C2201, C2202 and R2201 at approximately 5 Hz. Ground potential differences between the GEN and DSP-1 modules are compensated by the differential amplifier action of U220B R1204, R2107, R2106 and R2108. When DAEN is low relay K120 is de-energized and mutes the signal to the GEN module, thus preventing crosstalk in the analog generator modes.

Analog Signal Switching <8>

The analog input signal for each input channel is selected from one of seven sources. All analog signals entering the DSP-1 module are handled differentially to reduce the effect of ground loops. The signals from the three MONITOR OUTPUTS of the LVF module (CHANNEL A, CHANNEL B and READING) plus the analog MONITOR OUTPUT from the GEN module are routed though shielded cables from the appropriate boards to the DSP-1 board. Dc-coupled fixed range inputs are provided from two bnc connectors (DSP INPUT A and DSP INPUT B) located on the front lower left panel in SYS-2xx configurations and on the lower left back panel in SYS-3xx configurations. A seventh input signal is derived from the D/A converter output which is made available for calibration purposes only. The eighth input of the multiplexers is connected to ground to allow auto-zeroing of input offsets.

The dc coupled inputs are buffered by dual op-amp U210. Resistors R1102 and R2101 limit input current during overload conditions. The op-amp outputs are clamped by diodes D2101, D2102, D1101 and D1102 to prevent damage to the multiplexers if the op-amp outputs attempt to exceed 6 Volts.

The differential 1-of-8 input multiplexer for channel A is created with dual one-of-four CMOS switches U611 and U510. Each CMOS switch is used to select among one of four inputs by the logic levels on pin 9 and pin 10. If none of the four input signals is required the switch output is tri-stated by a high logic level on pin 6. The differential multiplexer outputs are buffered by op-amps U711, U612A and U410A. The differential signals are converted to ground referenced signals compatible with the anti-alias filters by U712A and U411A. The channel B hardware is identical.

Multiplexer U610 selects between the eight available hardware trigger signals. The selected signal is routed to the trigger comparator U840 on schematic <5> through buffer U641. The sync signal from the analog generator arrives via P34 and appears as a status bit as well as a trigger source. To match the threshold of the trigger comparator, the generator sync signal is attenuated by resistors R3401 and R5103 and centered around ground by R5102.

Antialias Filters <9>

The antialiasing filters are analog lowpass filters used to eliminate signals above the Nyquist rate from the A/D converter input. It is a "FDNR" (Frequency Dependent Negative Resistance) ladder filter as is the D/A reconstruction filter. A conventional LC ladder filter consists of series arms which are inductors and shunt arms which are capacitors. As the signal frequency increases, the series inductor impedance increases and the shunt capacitor impedance decreases. Above the corner frequency of the filter the attenuation rises rapidly, reducing out of band signals at the filter output. A FDNR ladder filter may be thought of as an LC lowpass ladder filter in which each inductor has been replaced by a resistor and each capacitor has been replaced by a FDNR element. Using this transformation, resistors in the original filter become capacitors in the transformed filter. Its impedance decreases with frequency twice as fast as a conventional capacitor. This doubly sharp shunt impedance, in combination with the fixed impedance in the series arms of the filter produces the same rolloff as the original LC filter.

Since the two filters are nominally identical, only one will be described here. The input signal is applied to the filter at C7103 and R8103. R8103 and R8101 provide a dc bias current path for U712, U720, U721, and U731. C7103 and C8302 are the source and load capacitances respectively. They are ratio matched to within 0.1% because their ratio directly determines the passband gain of the filter. R8102, R8202, R8211, and R8304 are the series elements of the ladder. R8104, U712, C7204, R8109, R8201, R8110 and C7205 comprise the first FDNR element, shunting the node between R8102 and R8202 to ground. Similarly, R8203, U720, C7207, R8204, C7208, R8206, R8205 and C7206 form the second FDNR element shunting the next node of the ladder. R8210, U721, C7301, R8209, R8212, R8208, C7302, R8207 comprise the third and final FDNR. R8301 and R8302 are the main gain setting resistors for buffer U731, providing a gain of 2 to compensate for the loss in the ladder network. R8303 and C8304 provide mid-band flatness compensation. C7303 and R8111 provide a dc signal path to exclude dc offsets from the filter.

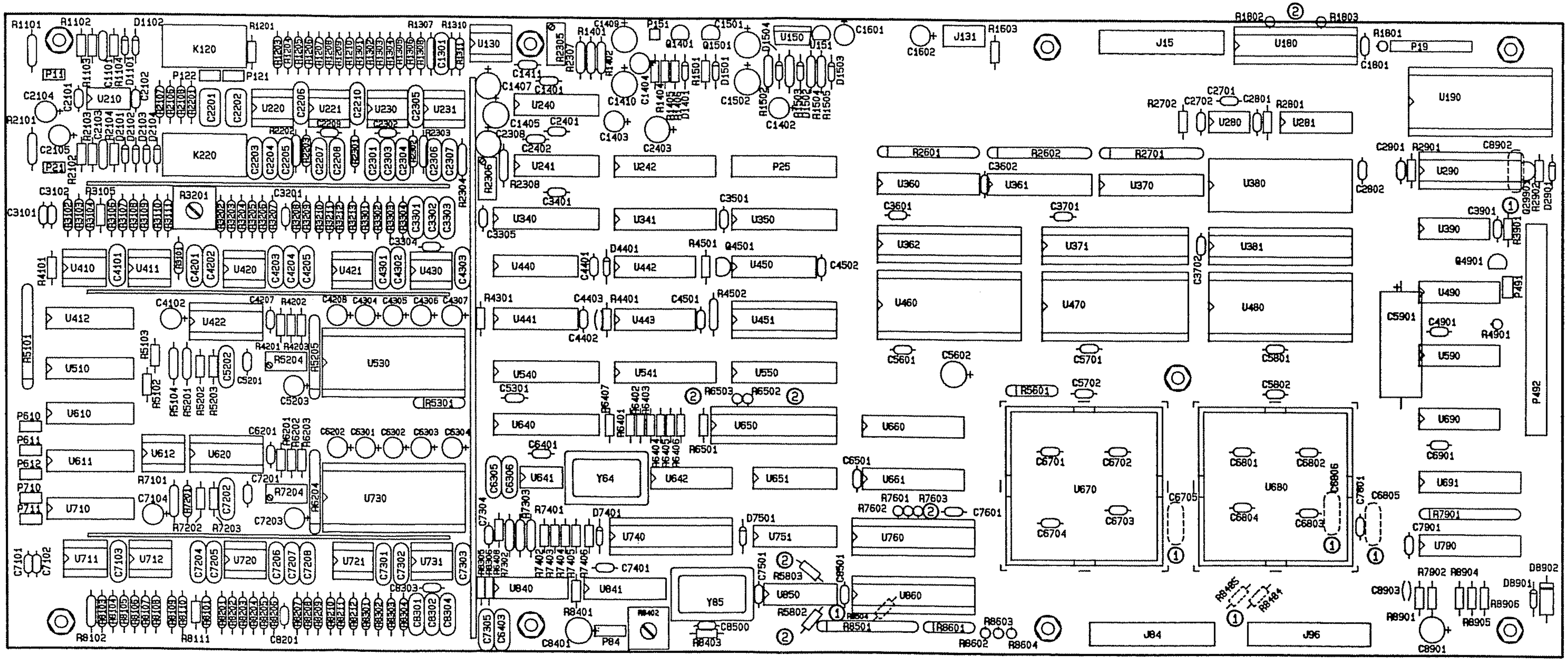
A/D Converters <10>

Analog signals are converted to digital signals for later processing by two 16-bit A/D converters and their associated sample-and-hold amplifiers. There are two nominally identical channels of A/D conversion. Only channel A will be described. The input signals from the antialiasing filters are applied to sample-and-hold amplifier U620. It operates in an inverting configuration with gain set by R7201 and R7101. The R7203-C7202 network peaks the response of the sample and hold U620, reducing the error signal during hold mode with fast slewing signals. Narrowband dither is added from U641 into the summing junction through R7202 to reduce quantization distortion. The sample and hold mode is controlled by the conversion complete signal out of the A/D converter.

The output of the sample and hold drives the analog input of the A/D converter. The full scale signal at this point is approximately ±3 Volts peak. The conversion clock applied to pin 16 is a divide-by-6 version of the master clock. When operating at the 192 kHz sample rate this is 4.096 MHz, at 176.4 kHz this is 3.7627 MHz. The conversion clock is stopped momentarily by U740 during the start conversion pulse to insure proper operation of the converter. The data is clocked out of the converter by a higher frequency clock applied to pin 21. This is a divide-by-4 signal from the master clock. Data output from the converter on pin 13 is routed through U740 to the serial input of the decimator dsp. Part of U740 acts as a dual input data selector, switching between data from the two A/D converters.

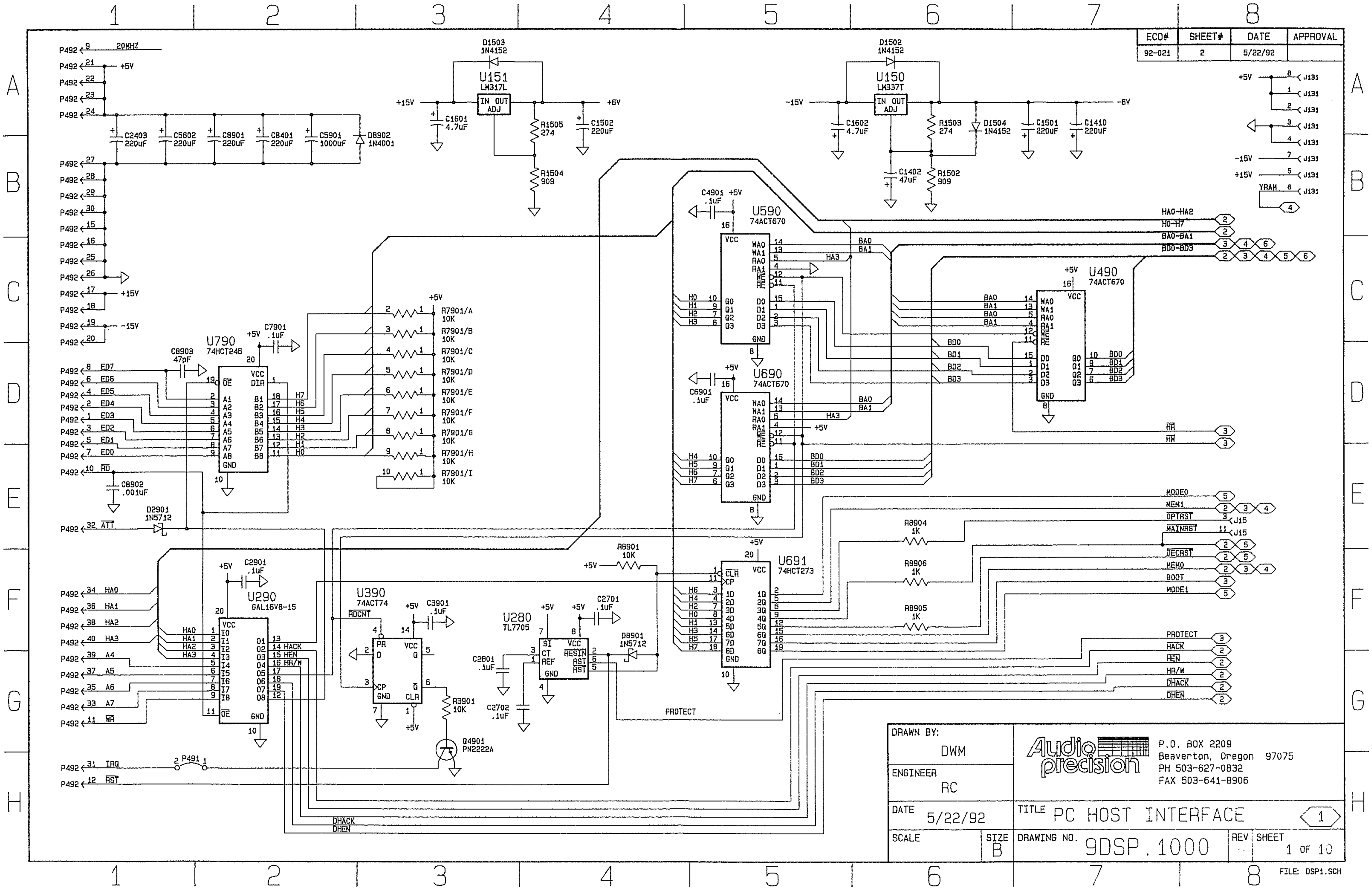
The converter MSB is adjusted by potentiometer R7204. The converter is heavily decoupled from the power supplies by sip network R6204 and capacitors C6304, C7203, C6302, and C6303 to reduce noise pickup. Resistor network R5301 shuts down the internal conversion clock. Capacitors C6301 and C6202 filter the internal reference voltage circuits.

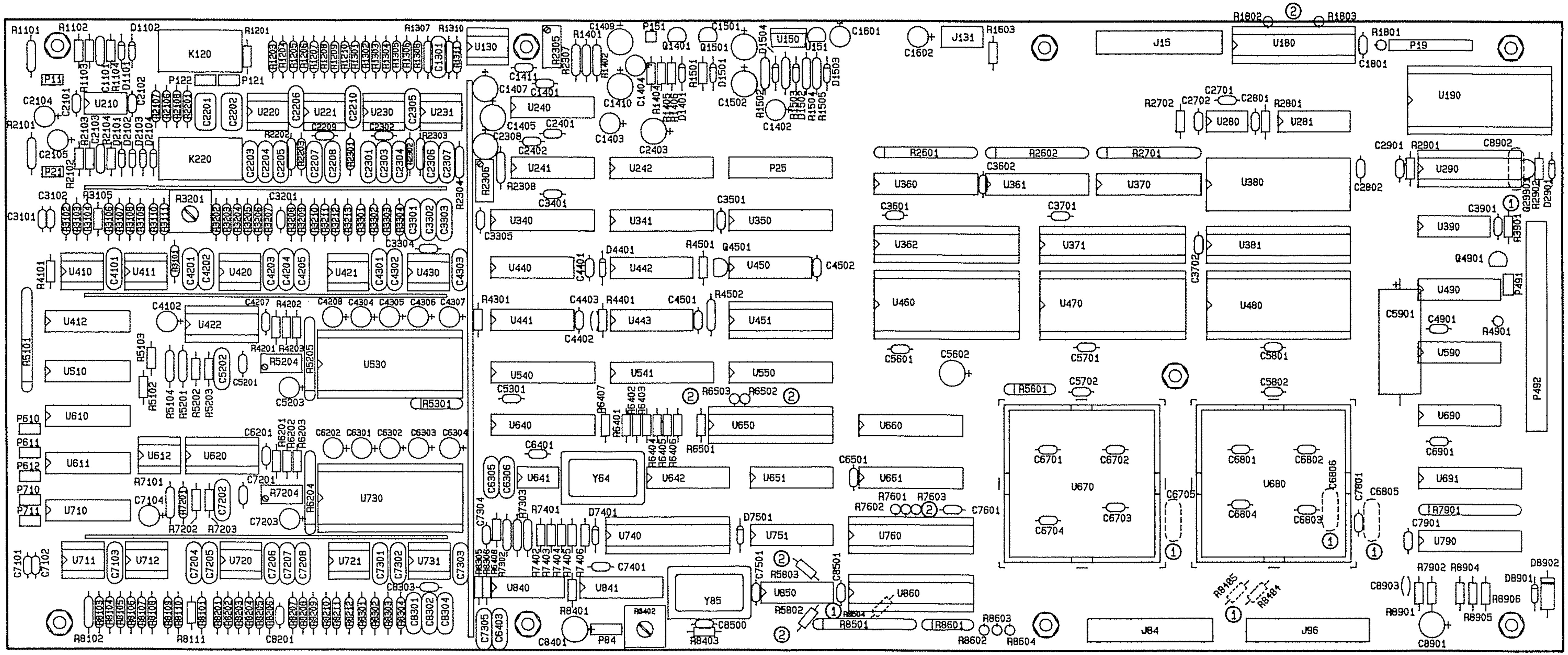
8-bit counter U841 and programmable logic chip U740 generate the A/D converter clock signals. Crystal oscillator Y64 supplies a 22.5792 MHz clock to the pal for use in generating 44.1 kHz and 176.4 kHz sample rate signals. All other sample rates are derived from the 24.576 MHz clock. The SAMPLEF line from U640 routes the 24.576 MHz clock to U740 pin 22 when high and the 22.5792 MHz clock when low. Counter U841 derives binary sub-multiples of the selected clock which are combined in U740 to obtain the gated clocks required by the A/D converters and by the dsp's serial input port.



DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

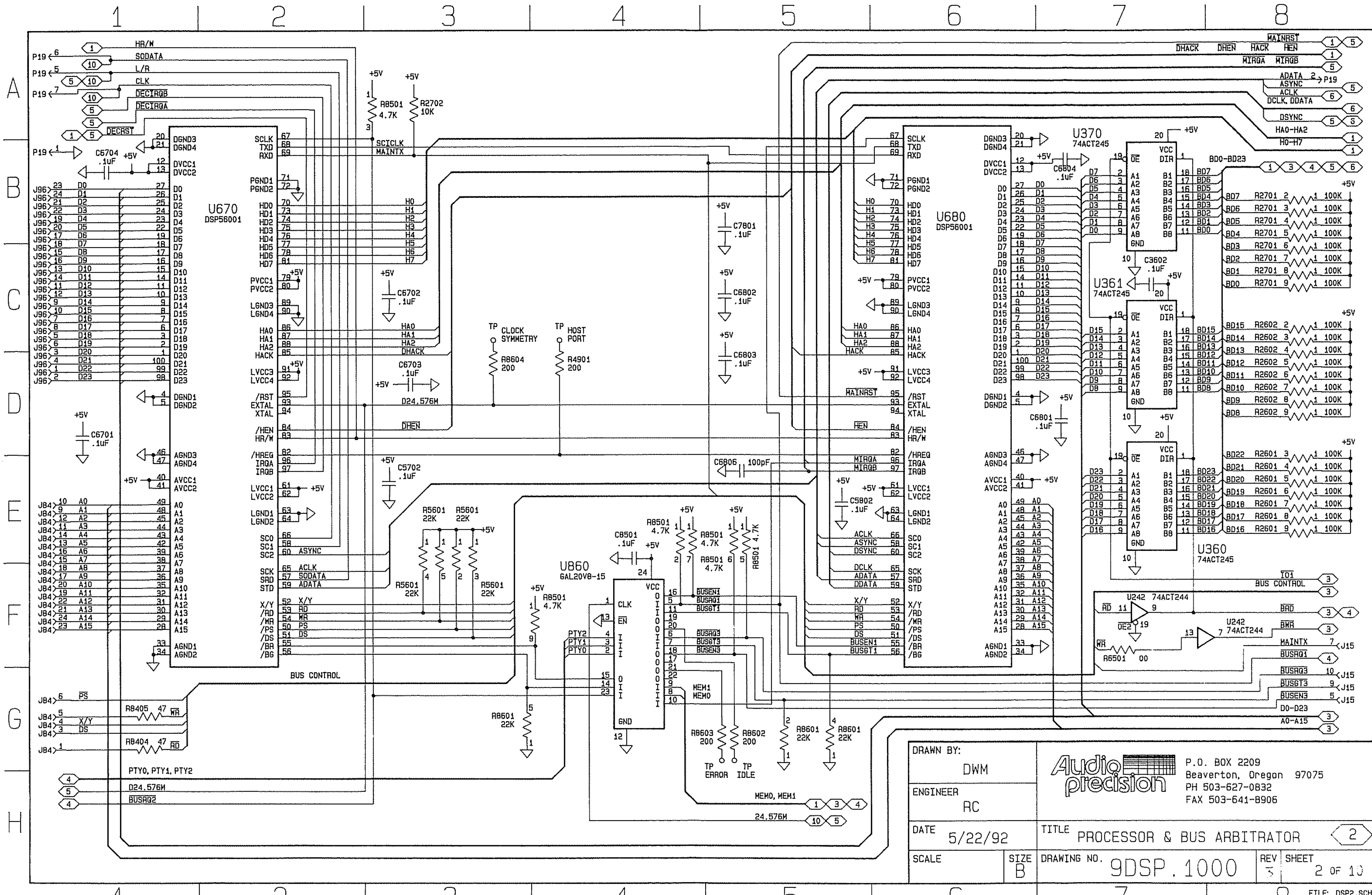
① Parts on solder side.
② Parts on component side.

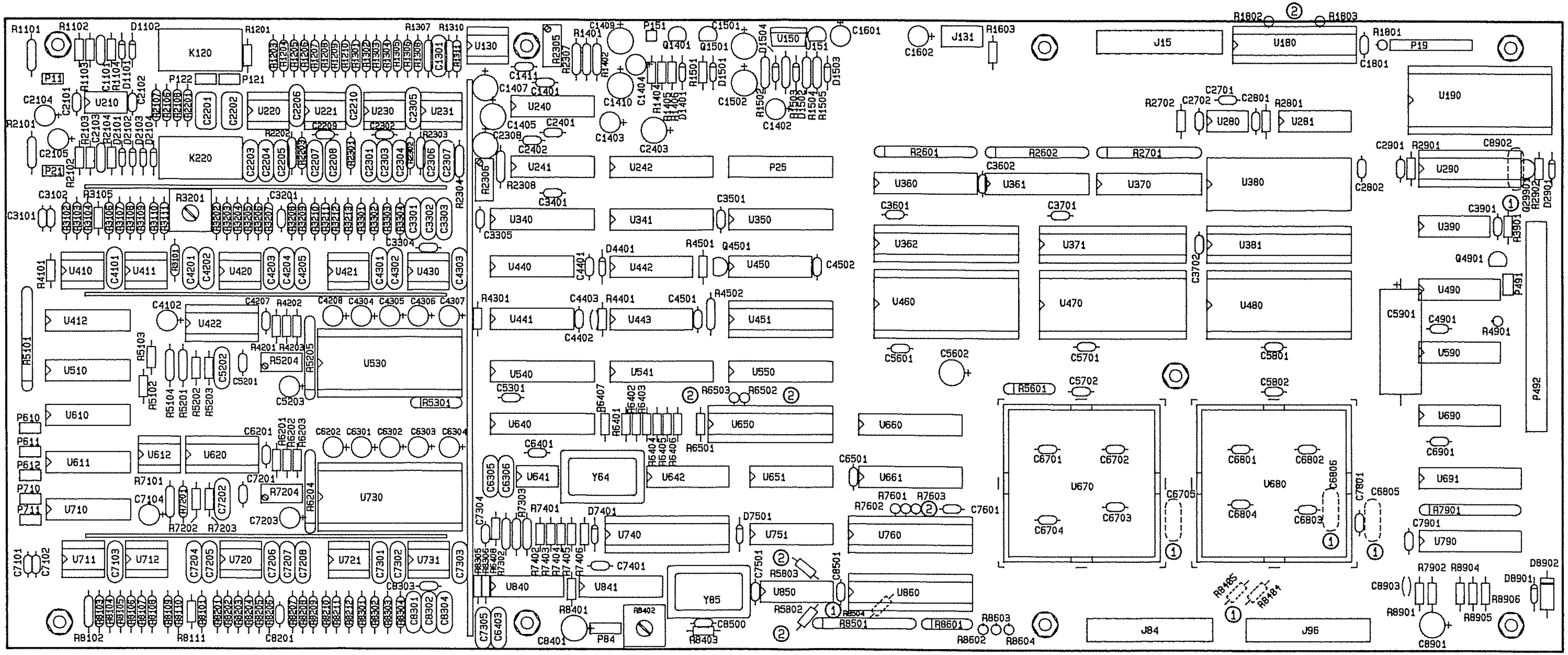

ECO# 92-021
SHEET# 2
DATE 5/22/92
APPROVAL
P492
20MHZ
+5V
+15V
-15V
+6V
-6V
C2403 220uF
C5602 220uF
C8901 220uF
C8401 220uF
C5901 1000uF
D8902 1N4001
D1503 1N4152
U151 LM317L
IN OUT ADJ
C1601 4.7uF
R1505 274
R1504 909
C1502 220uF
D1502 1N4152
U150 LM337T
C1602 4.7uF
R1503 274
D1504 1N4152
C1501 220uF
C1410 220uF
C1402 47uF
R1502 909
J131
YRAM
C4901 .1uF
U590 74ACT670
U690 74ACT670
C6901 .1uF
U490 74ACT670
HA0-HA2
H0-H7
BA0-BA1
BD0-BD3
HA3
HR
HW
ED7
ED6
ED5
ED4
ED3
ED2
ED1
ED0
RD
ATT
C8903 47pF
U790 74HCT245
C7901 .1uF
R7901/A 10K
R7901/B 10K
R7901/C 10K
R7901/D 10K
R7901/E 10K
R7901/F 10K
R7901/G 10K
R7901/H 10K
R7901/I 10K
C8902 .001uF
D2901 1N5712
MODE0
MEM1
OPTRST
MAINRST
DECRST
MEM0
BOOT
MODE1
J15
R8904 1K
R8906 1K
R8905 1K
R8901 10K
U691 74HCT273
C2901 .1uF
U290 GAL16V8-15
HA0
HA1
HA2
HA3
A4
A5
A6
A7
WR
HACK
HEN
HR/W
U390 74ACT74
RDCNT
C3901 .1uF
R3901 10K
Q4901 PN2222A
U280 TL7705
C2701 .1uF
C2801 .1uF
C2702 .1uF
D8901 1N5712
PROTECT
DHACK
DHEN
IRQ
P491
RST
DRAWN BY: DWM
ENGINEER RC
DATE 5/22/92
SCALE
SIZE B
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
TITLE PC HOST INTERFACE
DRAWING NO. 9DSP.1000
REV
SHEET 1 OF 10
FILE: DSP1.SCH



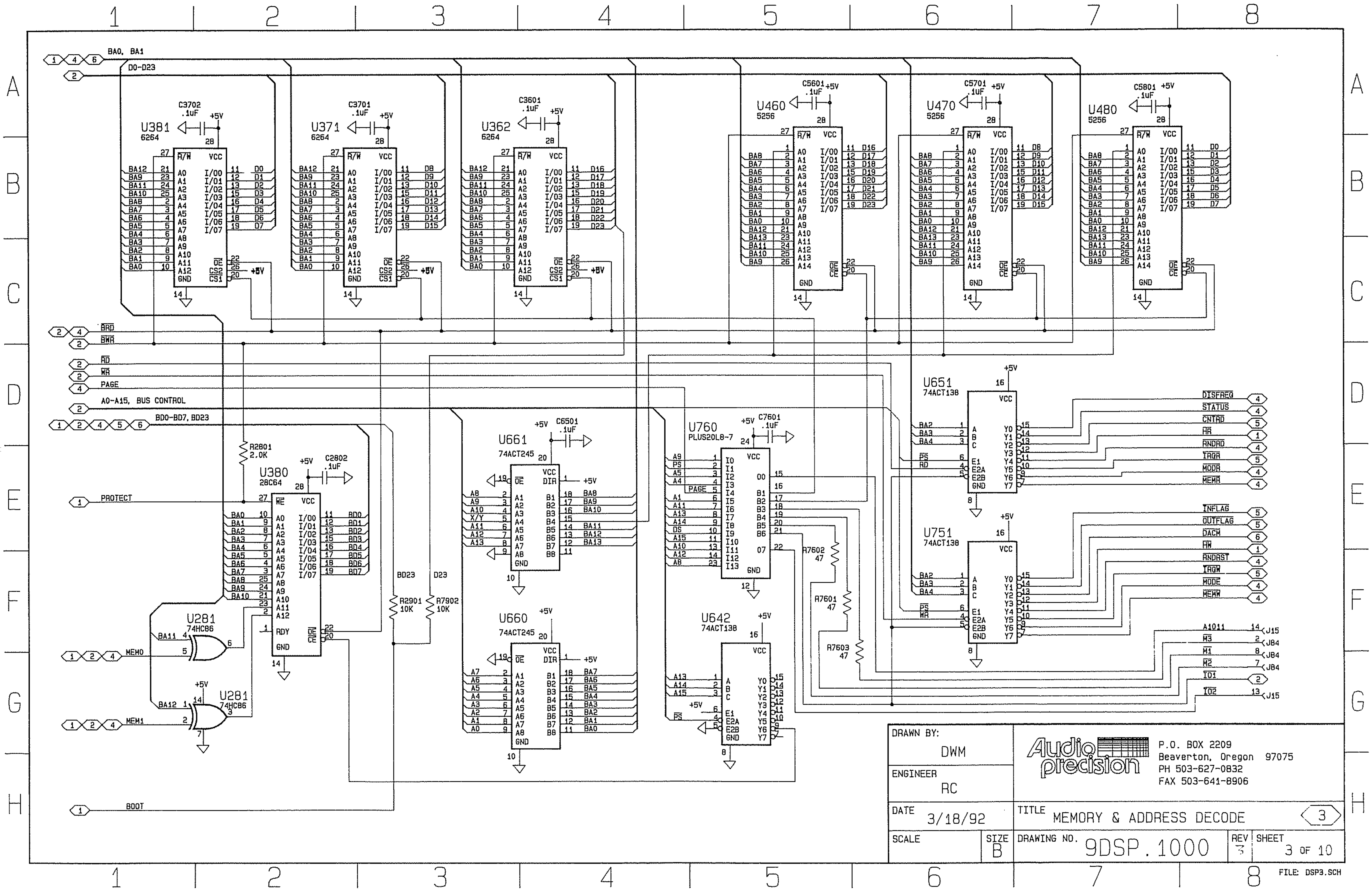
DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

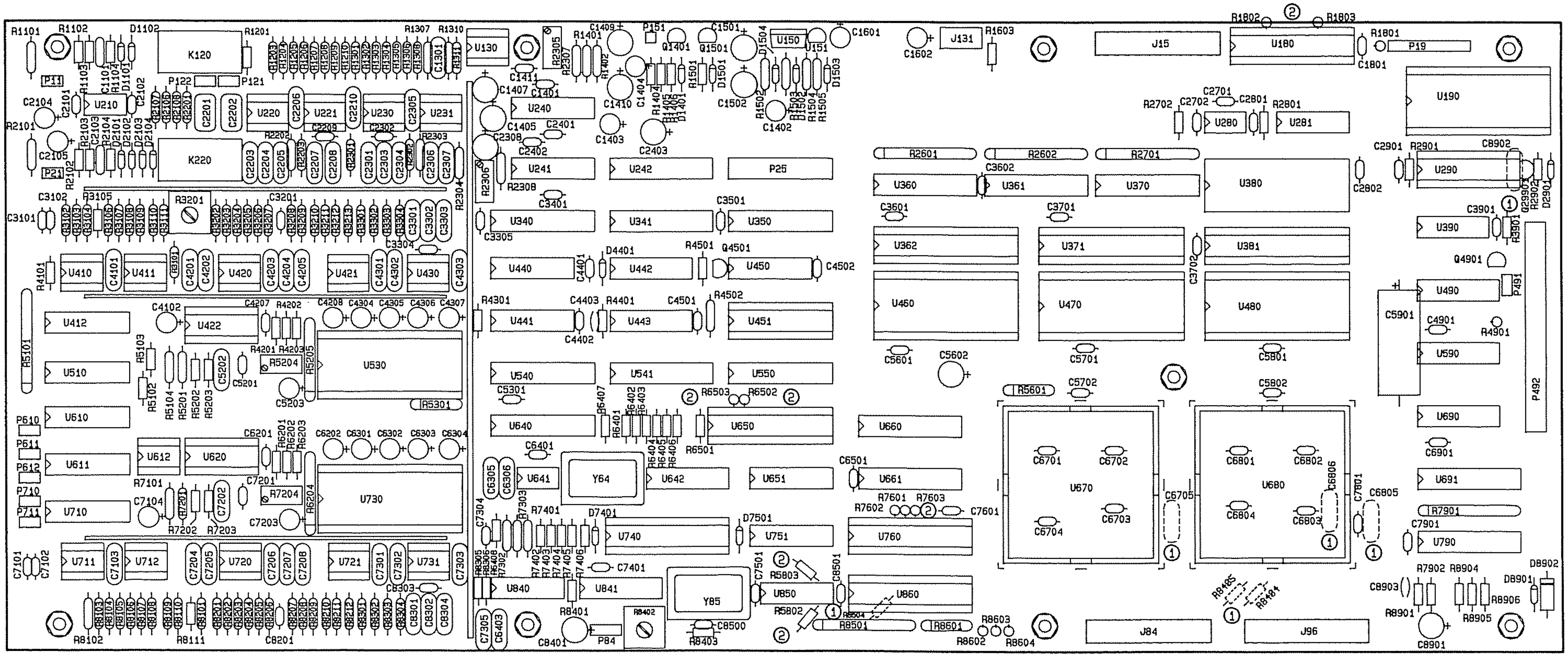
① Parts on solder side.
② Parts on component side.


U670
DSP56001
U680
DSP56001
U860
GAL20V8-15
U370
74ACT245
U361
74ACT245
U360
74ACT245
U242 74ACT244
BUS CONTROL
TP CLOCK SYMMETRY
TP HOST PORT
TP ERROR
TP IDLE
MEM0, MEM1
24.576M
PTY0, PTY1, PTY2
D24.576M
BUSRQ2
D0-D23
A0-A15
BD0-BD23
HA0-HA2
H0-H7
DRAWN BY:
DWM
ENGINEER
RC
DATE
5/22/92
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
TITLE PROCESSOR & BUS ARBITRATOR
2
SCALE
SIZE B
DRAWING NO. 9DSP.1000
REV 3
SHEET 2 OF 10
FILE: DSP2.SCH



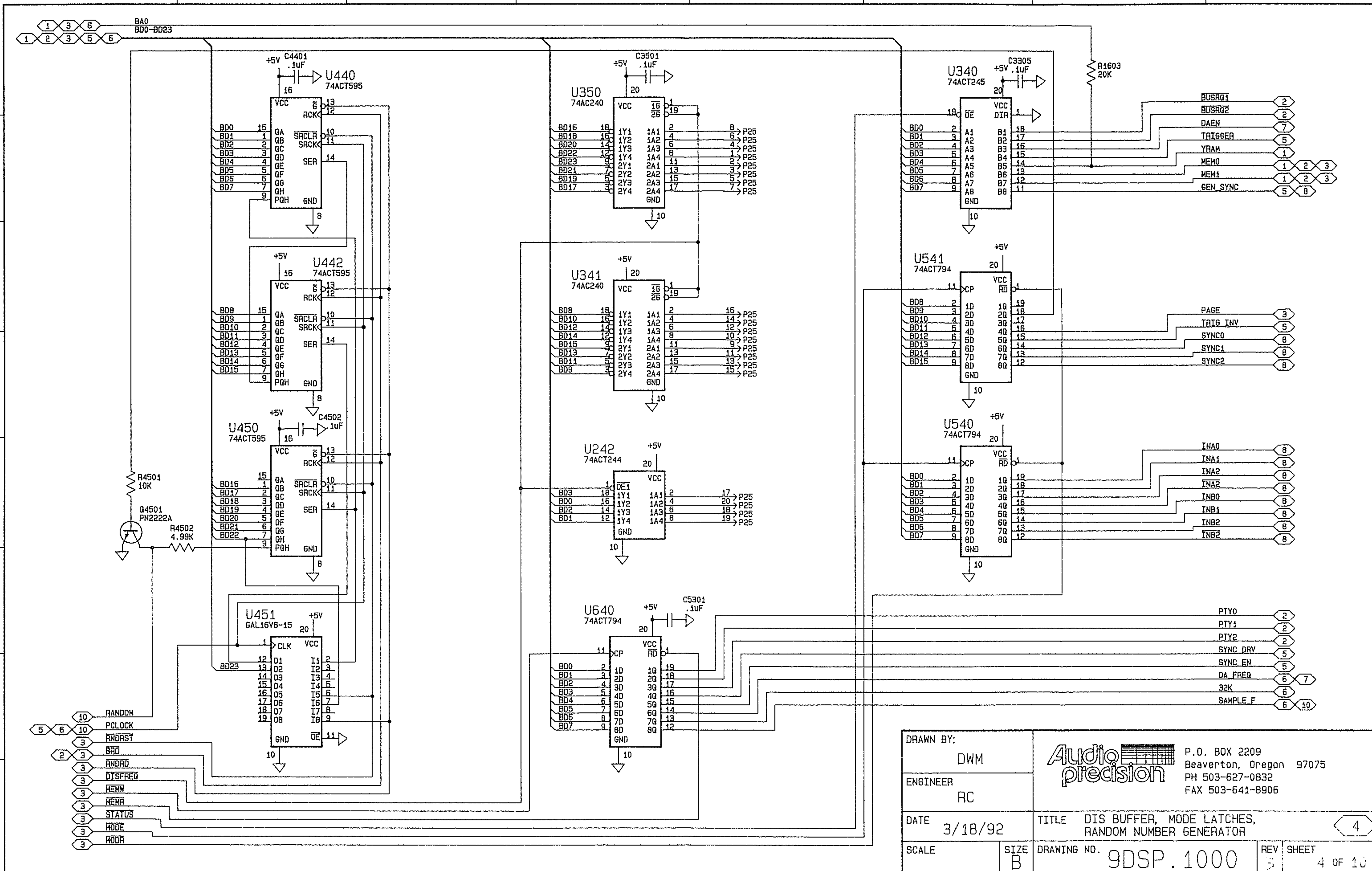
DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)


DRAWN BY: DWM
ENGINEER RC
DATE 3/18/92
SCALE
SIZE B
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
TITLE MEMORY & ADDRESS DECODE
3
DRAWING NO. 9DSP.1000
REV 3
SHEET 3 OF 10
FILE: DSP3.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

① Parts on solder side.
② Parts on component side.



DRAWN BY: DWM

ENGINEER RC

DATE 3/18/92

SCALE

SIZE B

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

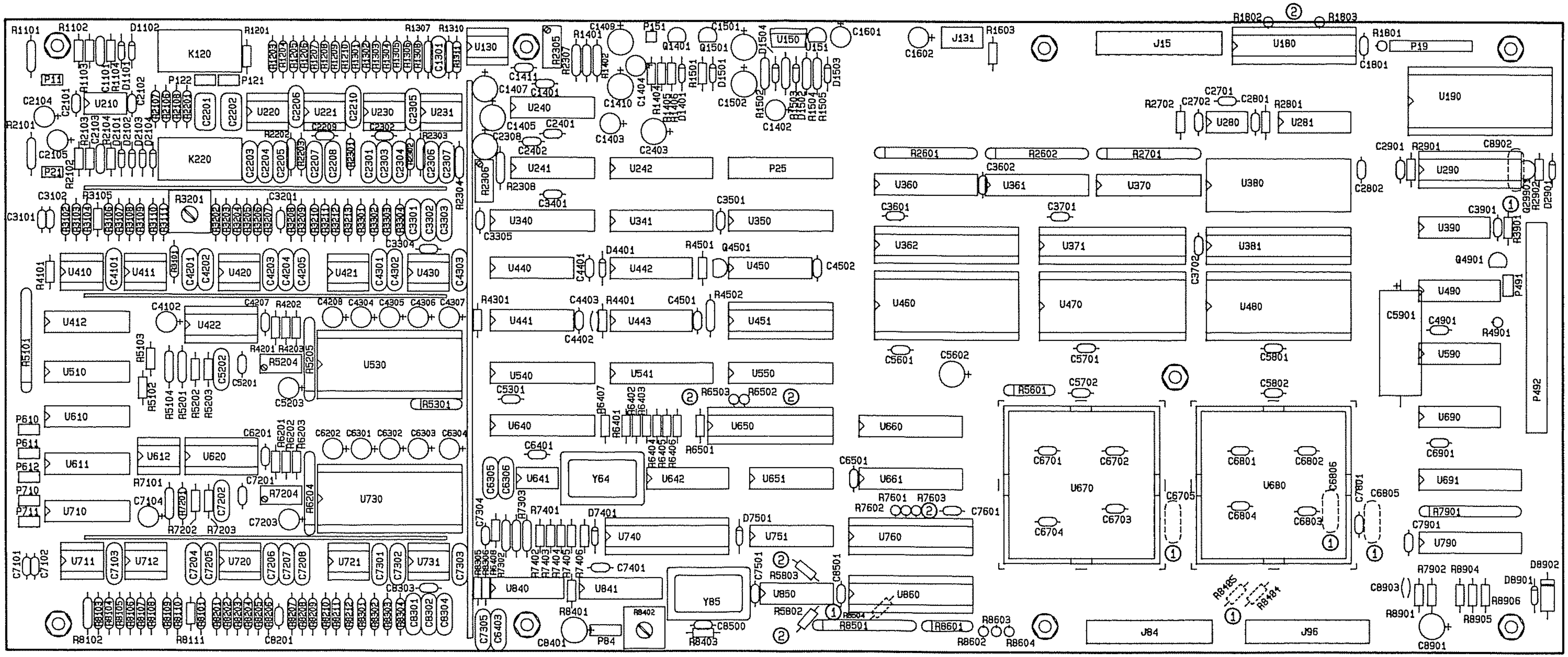
TITLE DIS BUFFER, MODE LATCHES, RANDOM NUMBER GENERATOR

DRAWING NO. 9DSP.1000

REV 5

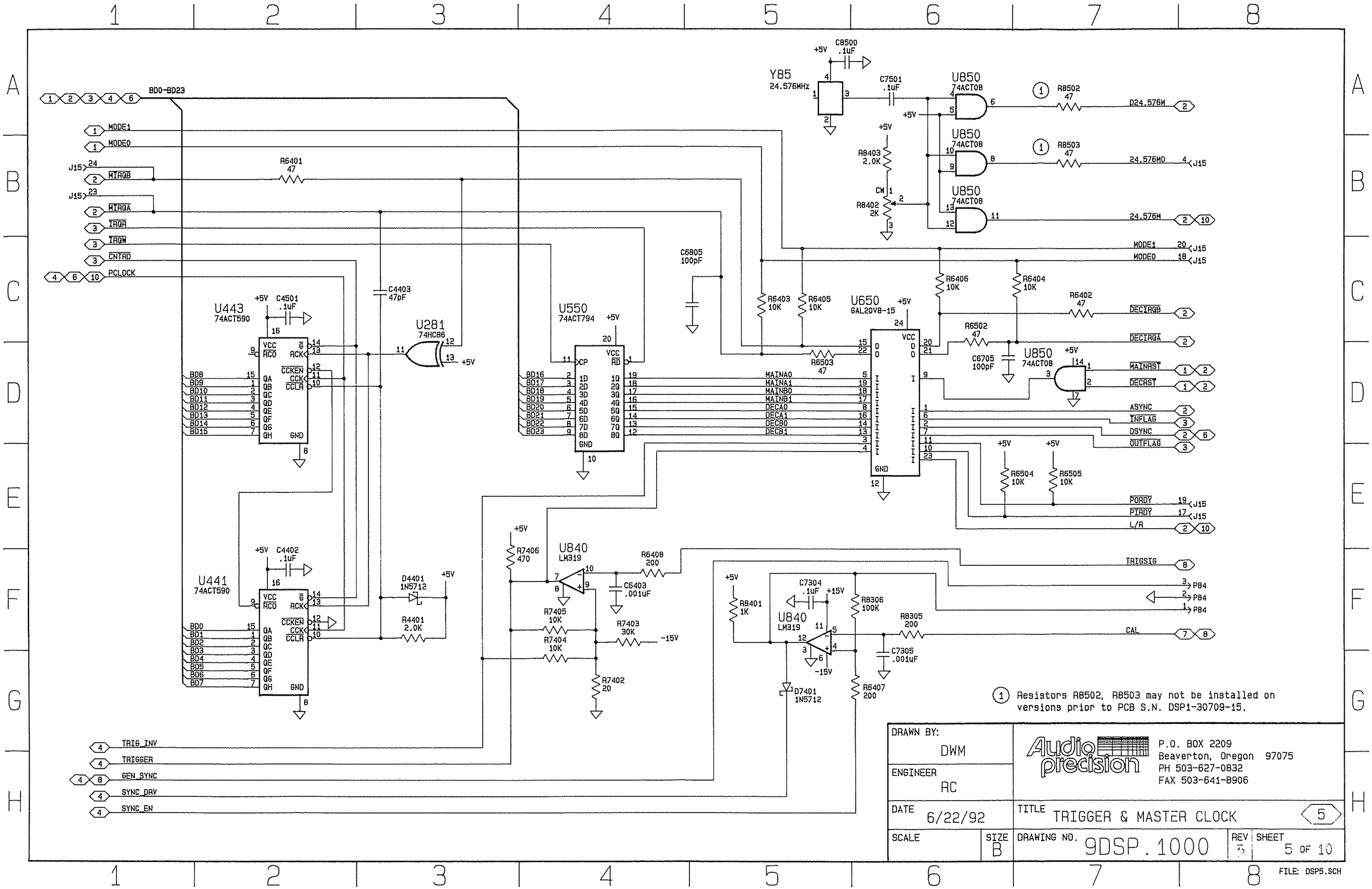
SHEET 4 OF 10

FILE: DSP4.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

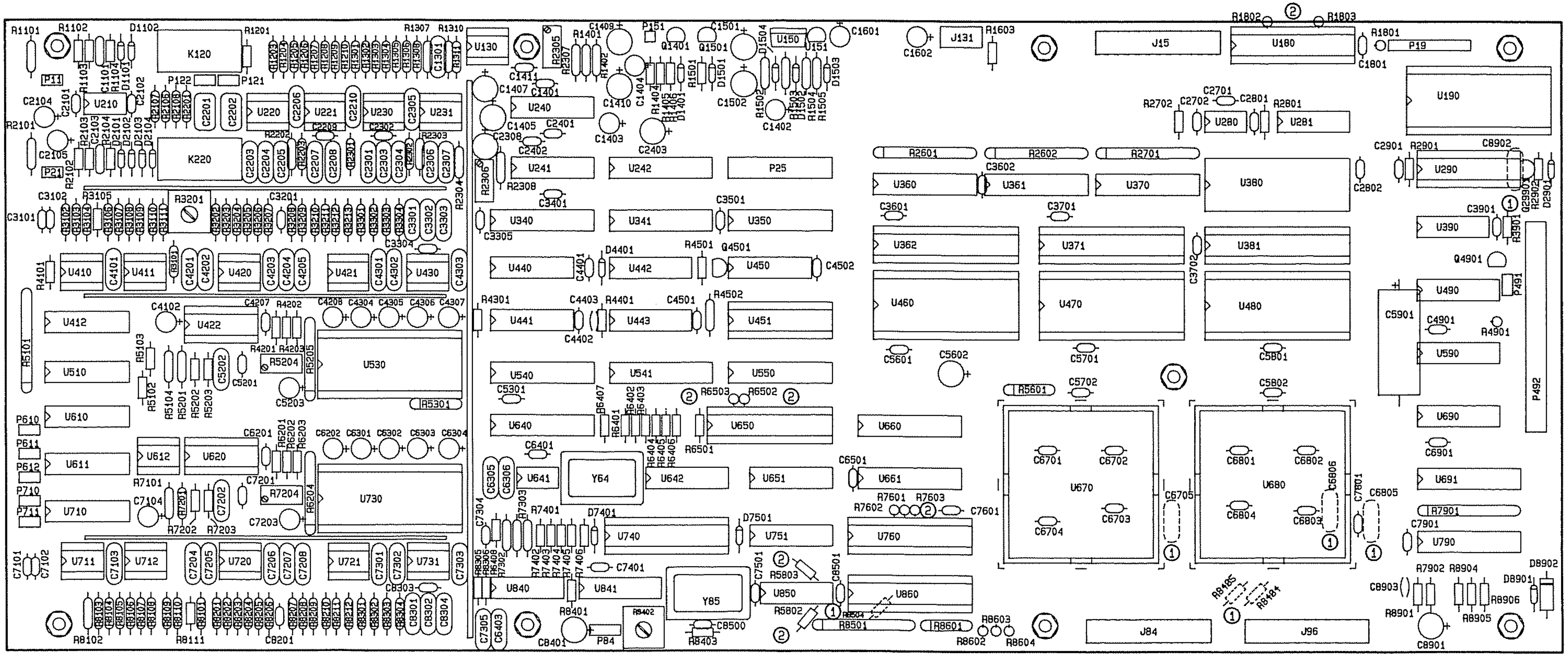
① Parts on solder side.
② Parts on component side.



(1) Resistors R8502, R8503 may not be installed on versions prior to PCB S.N. DSP1-30709-15.

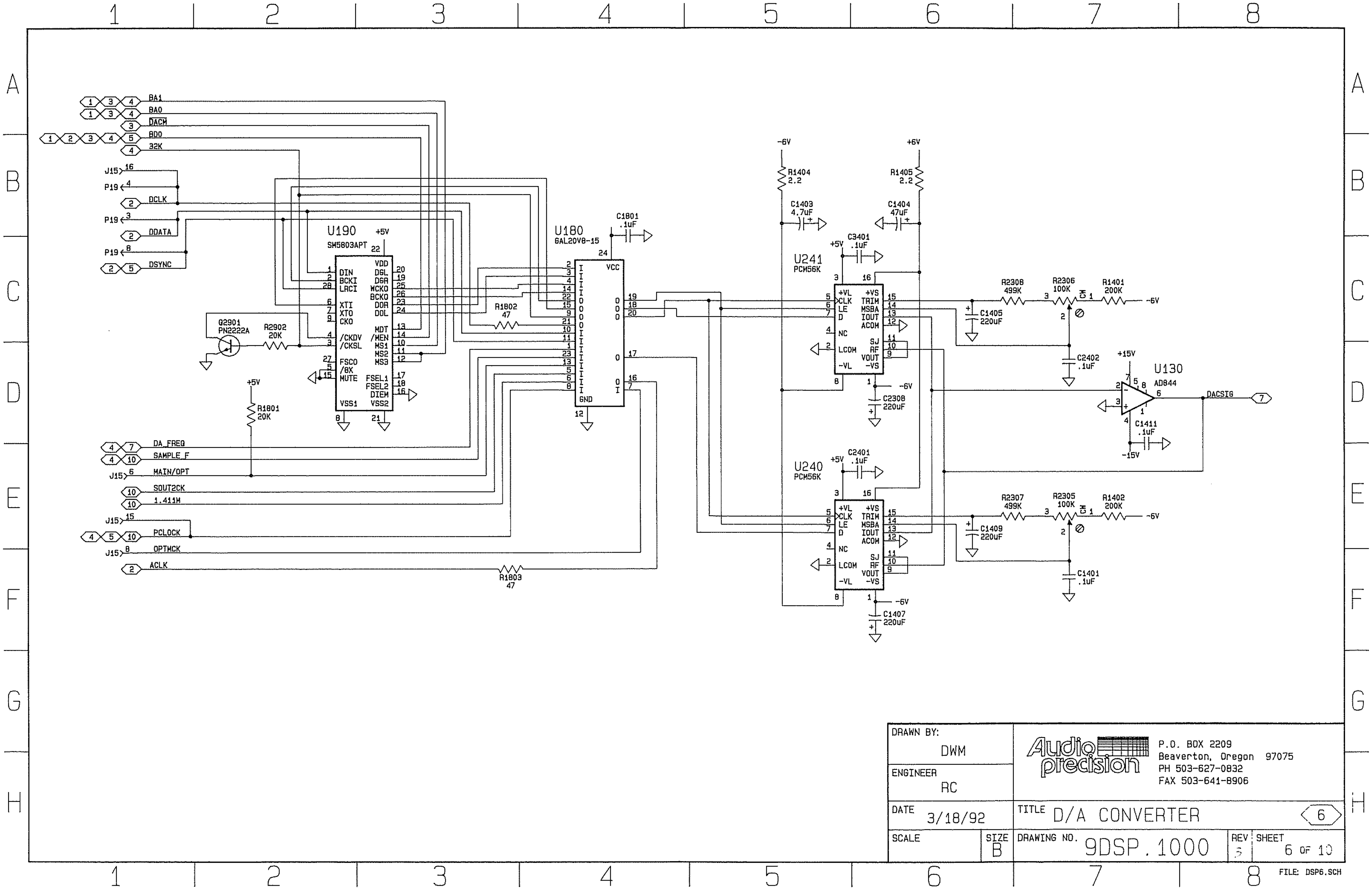
DRAWN BY: DWM	Audio precision P.O. BOX 2209 Beaverton, Oregon 97075 PH 503-627-0832 FAX 503-641-8906
ENGINEER RC	
DATE 6/22/92	TITLE TRIGGER & MASTER CLOCK (5)
SCALE / SIZE B	DRAWING NO. 9DSP.1000 / REV 3 / SHEET 5 OF 10

FILE: DSP5.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

① Parts on solder side.
② Parts on component side.



DRAWN BY: DWM

ENGINEER: RC

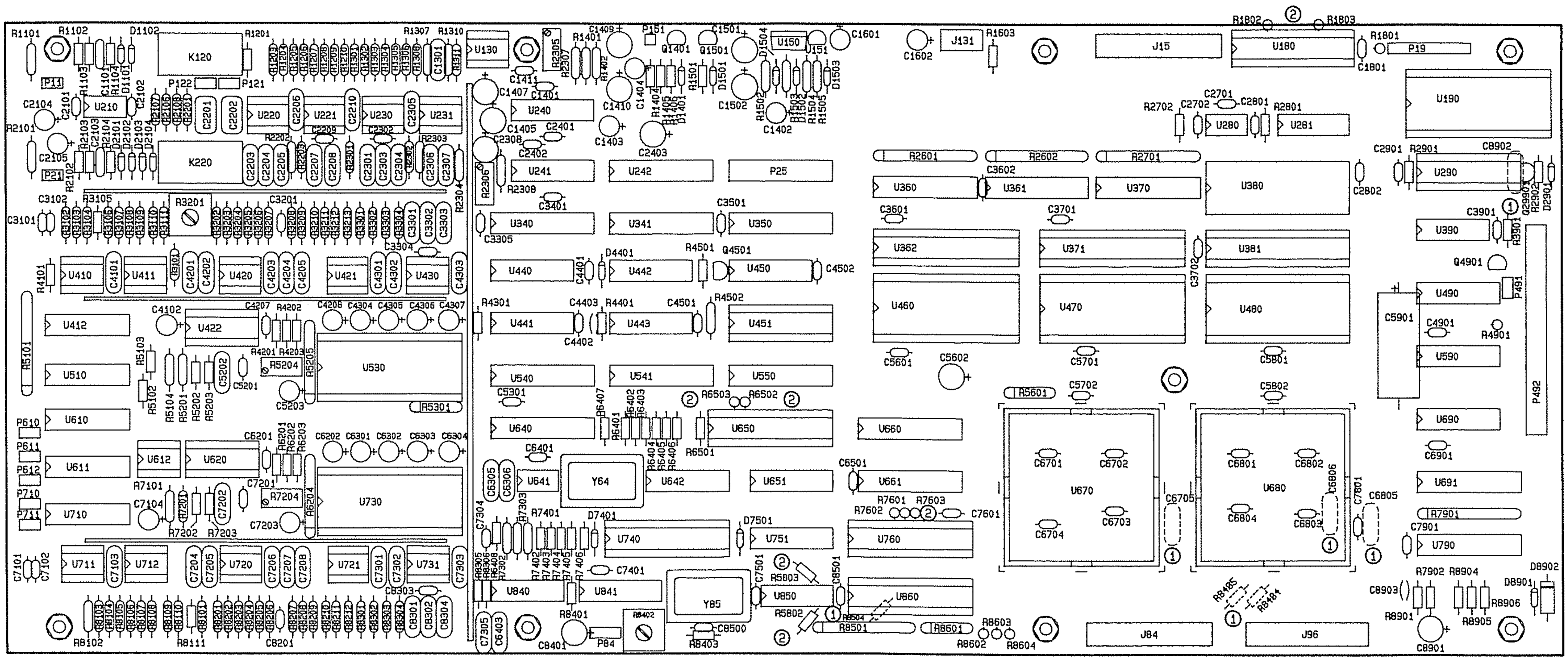
DATE: 3/18/92

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

TITLE: D/A CONVERTER (6)

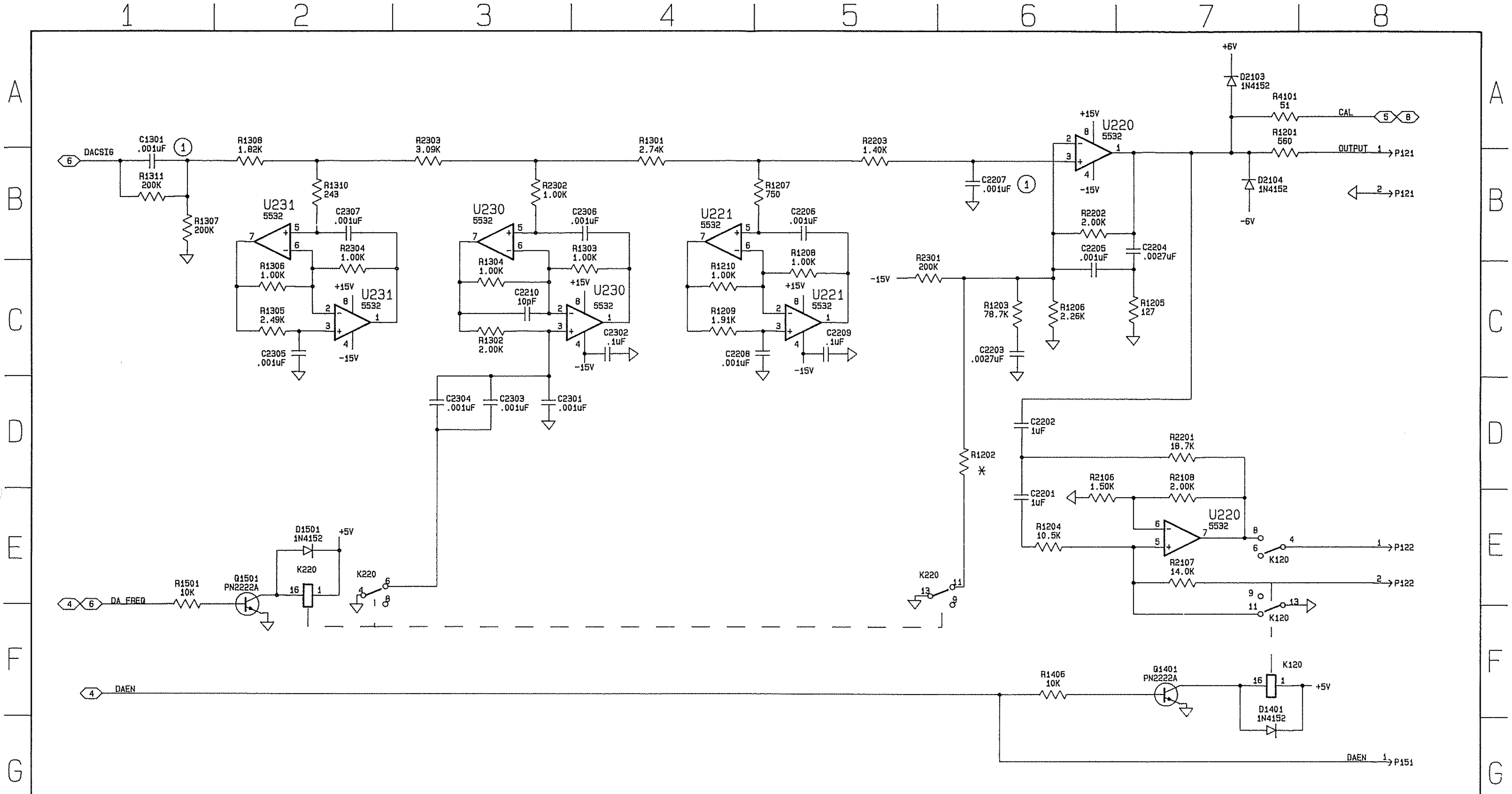
SCALE | SIZE: B | DRAWING NO. 9DSP.1000 | REV 5 | SHEET 6 OF 10

FILE: DSP6.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

① Parts on solder side.
② Parts on component side.



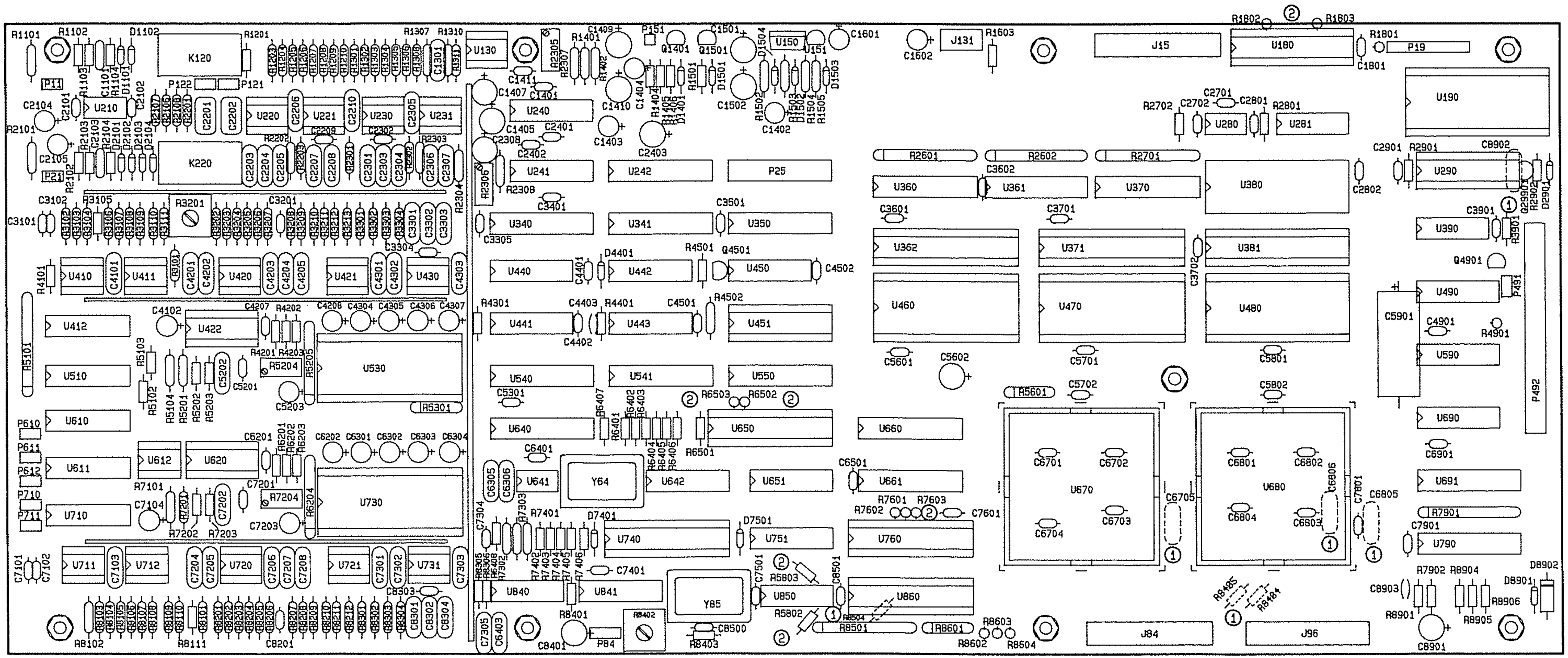
NOTES:

* NOT INSTALLED

(1) RATIO MATCHED PAIR WITHIN 1/2%.

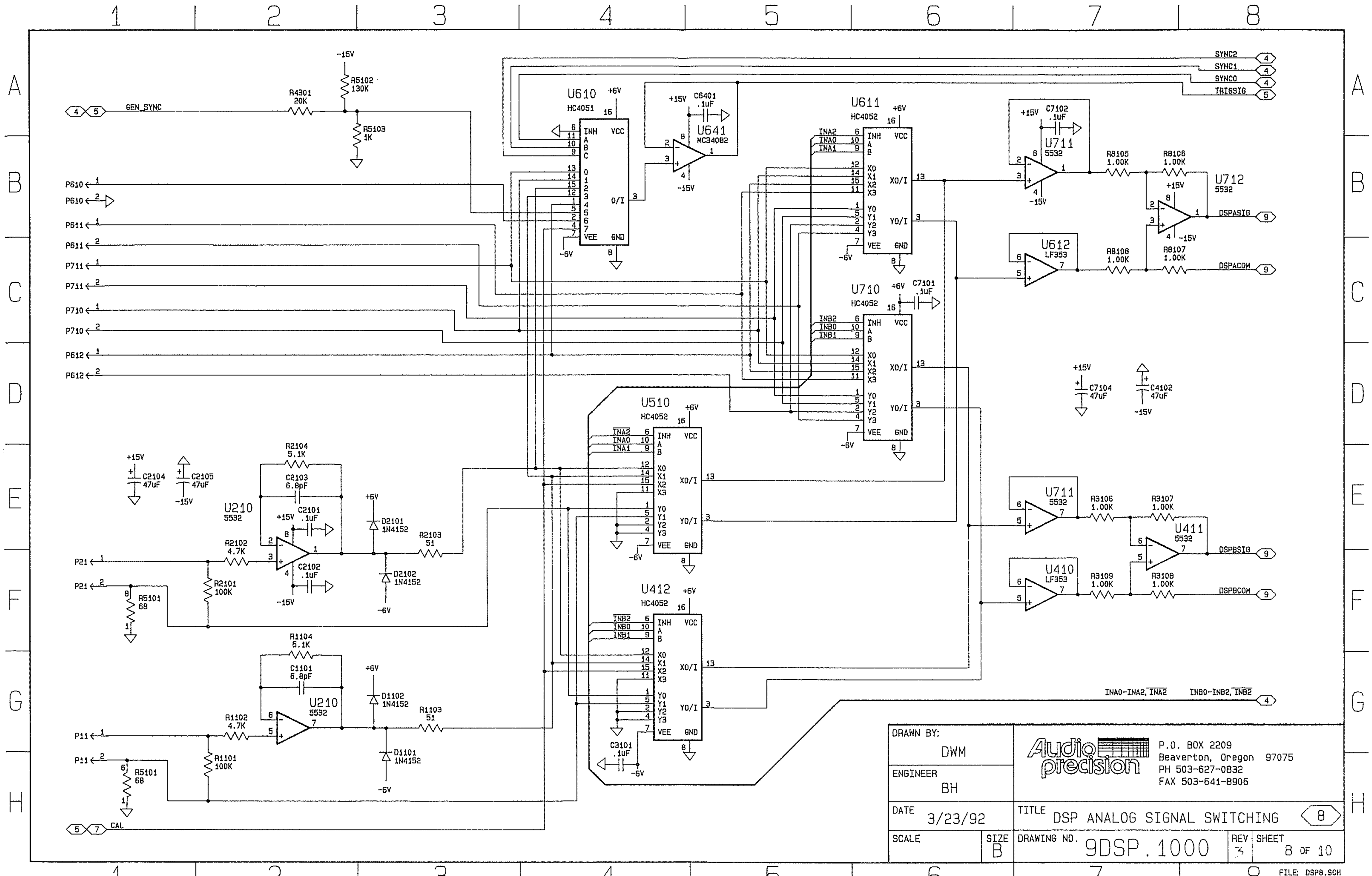
DRAWN BY: DWM	Audio precision — P.O. BOX 2209, Beaverton, Oregon 97075, PH 503-627-0832, FAX 503-641-8906
ENGINEER BH	
DATE 3/18/92	TITLE DAC RECONSTRUCTION FILTER (7)
SCALE — SIZE B	DRAWING NO. 9DSP.1000 — REV 3 — SHEET 7 OF 10

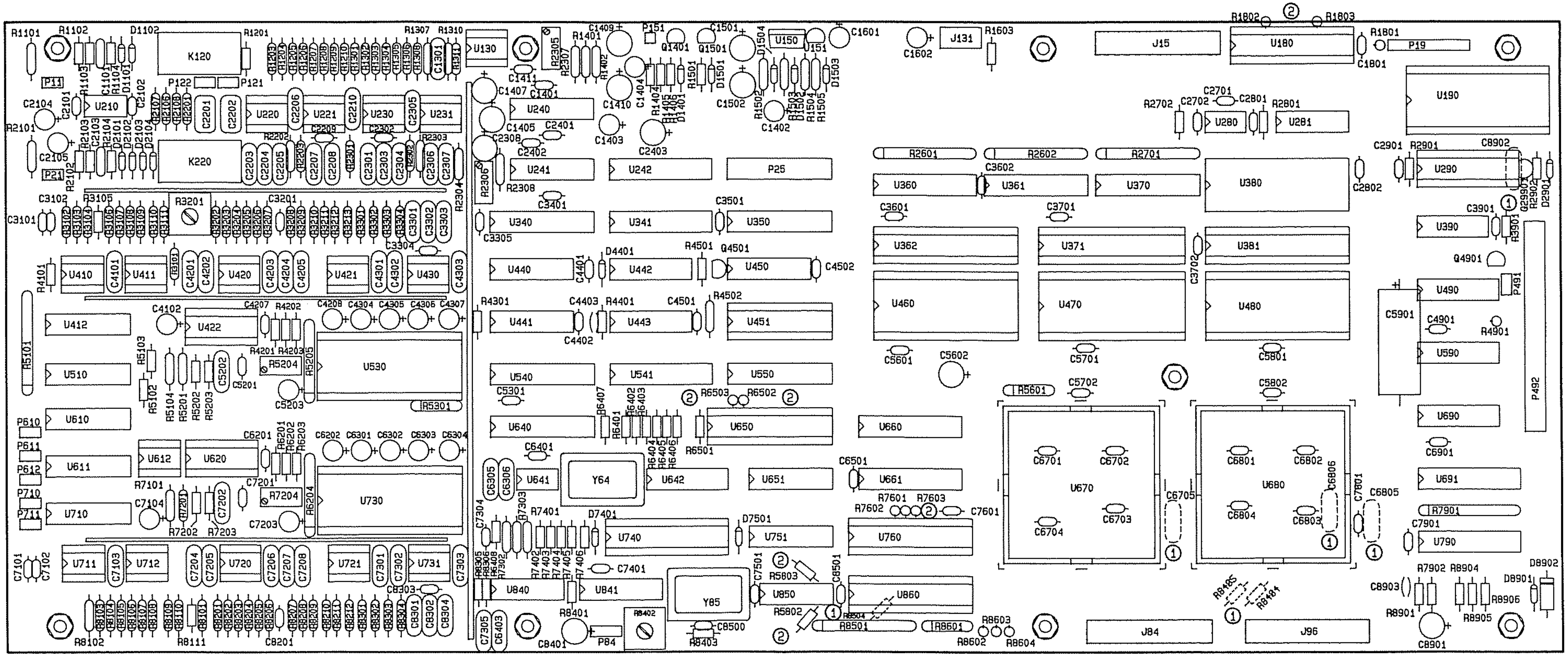
FILE: DSP7.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

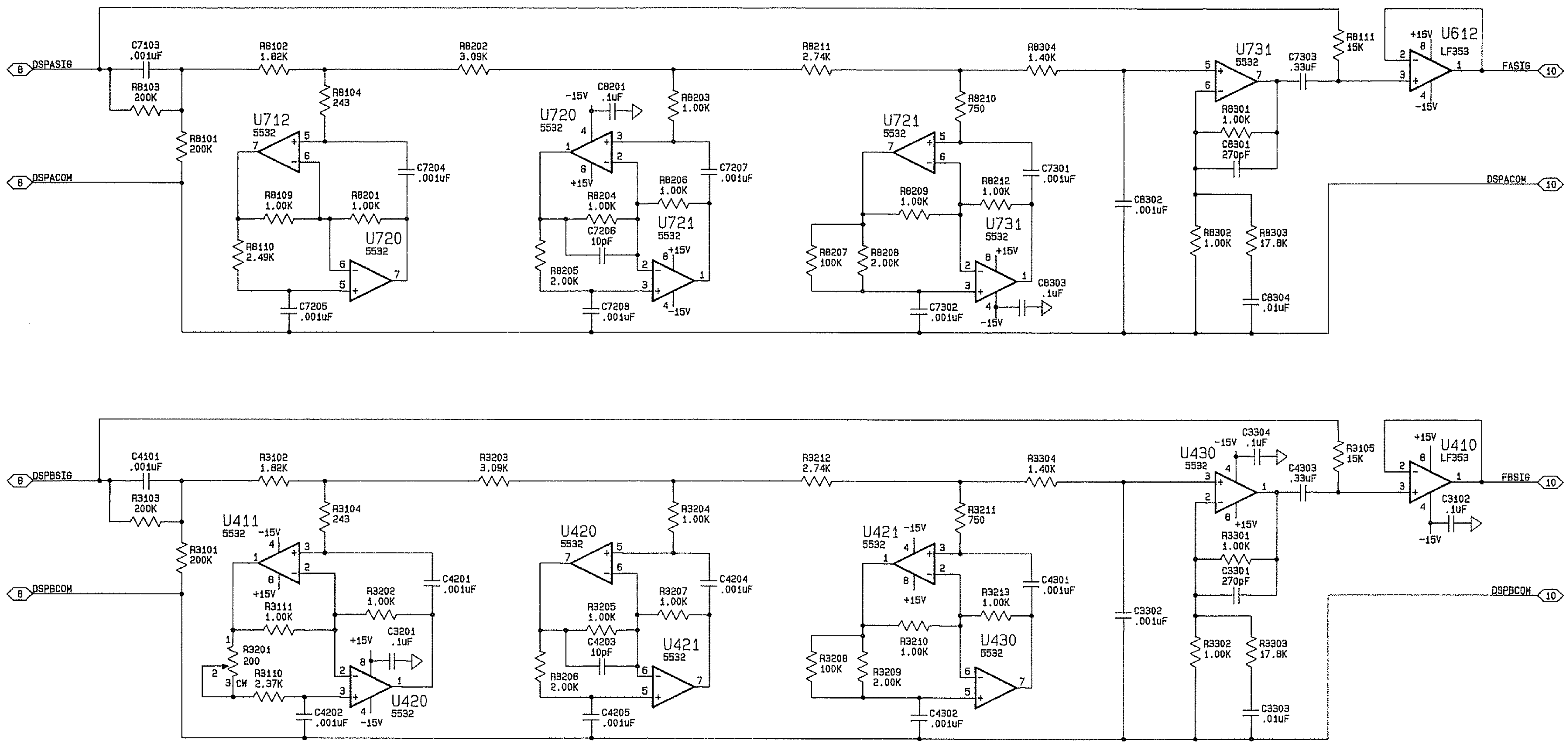
① Parts on solder side.
② Parts on component side.


GEN_SYNC
R4301 20K
R5102 130K
R5103 1K
-15V
U610 HC4051
U641 MC34082
C6401 .1uF
U611 HC4052
U710 HC4052
C7101 .1uF
U711 5532
C7102 .1uF
U712 5532
U612 LF353
R8105 1.00K
R8106 1.00K
R8108 1.00K
R8107 1.00K
SYNC2
SYNC1
SYNC0
TRIGSIG
DSPASIG
DSPACOM
P610
P611
P711
P710
P612
C7104 47uF
C4102 47uF
U510 HC4052
U412 HC4052
C3101 .1uF
U210 5532
R2104 5.1K
C2103 6.8pF
C2101 .1uF
C2102 .1uF
R2102 4.7K
R2101 100K
R5101 68
D2101 1N4152
D2102 1N4152
R2103 51
C2104 47uF
C2105 47uF
P21
R1104 5.1K
C1101 6.8pF
R1102 4.7K
R1101 100K
D1102 1N4152
D1101 1N4152
R1103 51
P11
CAL
U711 5532
U411 5532
U410 LF353
R3106 1.00K
R3107 1.00K
R3109 1.00K
R3108 1.00K
DSPBSIG
DSPBCOM
INA0-INA2, INA2
INB0-INB2, INB2
DRAWN BY: DWM
ENGINEER BH
DATE 3/23/92
SCALE
SIZE B
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
TITLE DSP ANALOG SIGNAL SWITCHING
8
DRAWING NO. 9DSP.1000
REV 3
SHEET 8 OF 10
FILE: DSP8.SCH



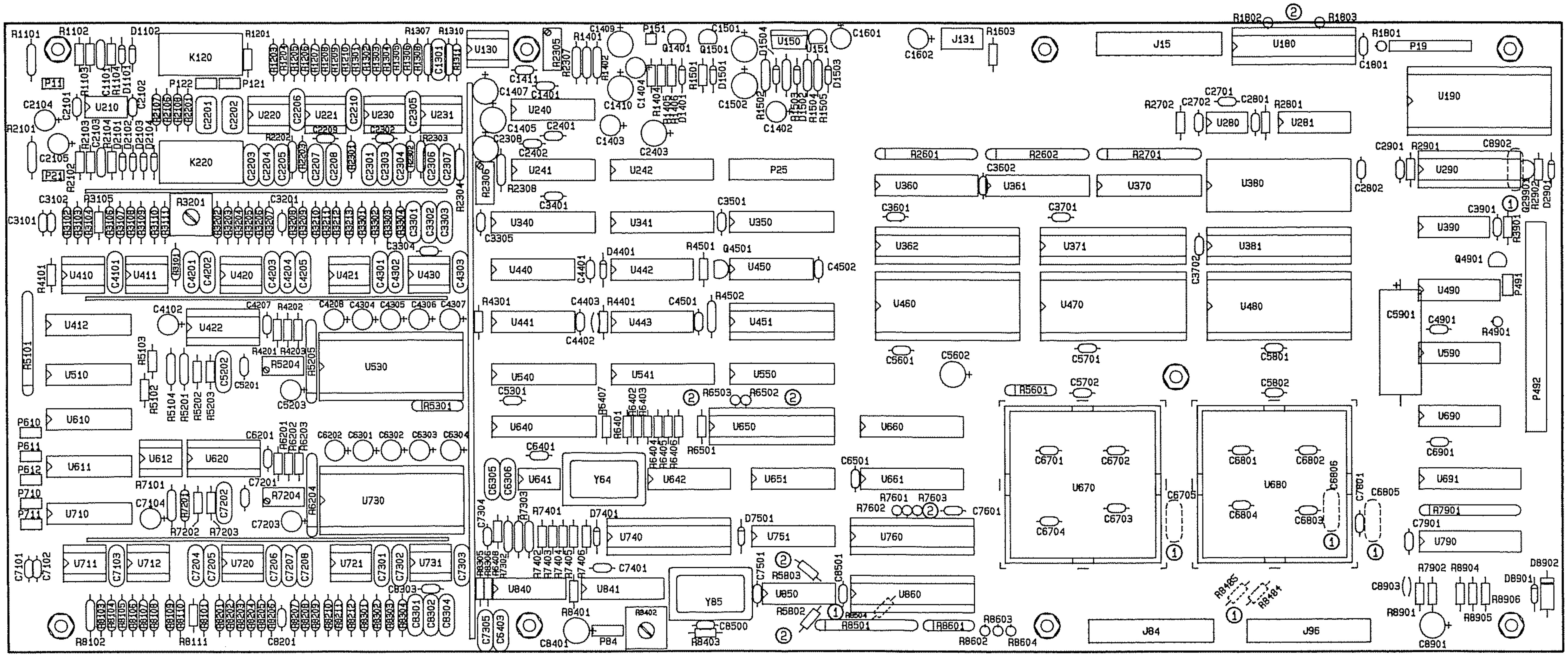
DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

① Parts on solder side.
② Parts on component side.



DRAWN BY: DWM	Audio precision	P.O. BOX 2209 Beaverton, Oregon 97075 PH 503-627-0832 FAX 503-641-8906
ENGINEER BH		
DATE 3/23/92	TITLE ANTI-ALIASING FILTER	9
SCALE	SIZE B	DRAWING NO. 9DSP.1000 · REV 3 · SHEET 9 OF 10

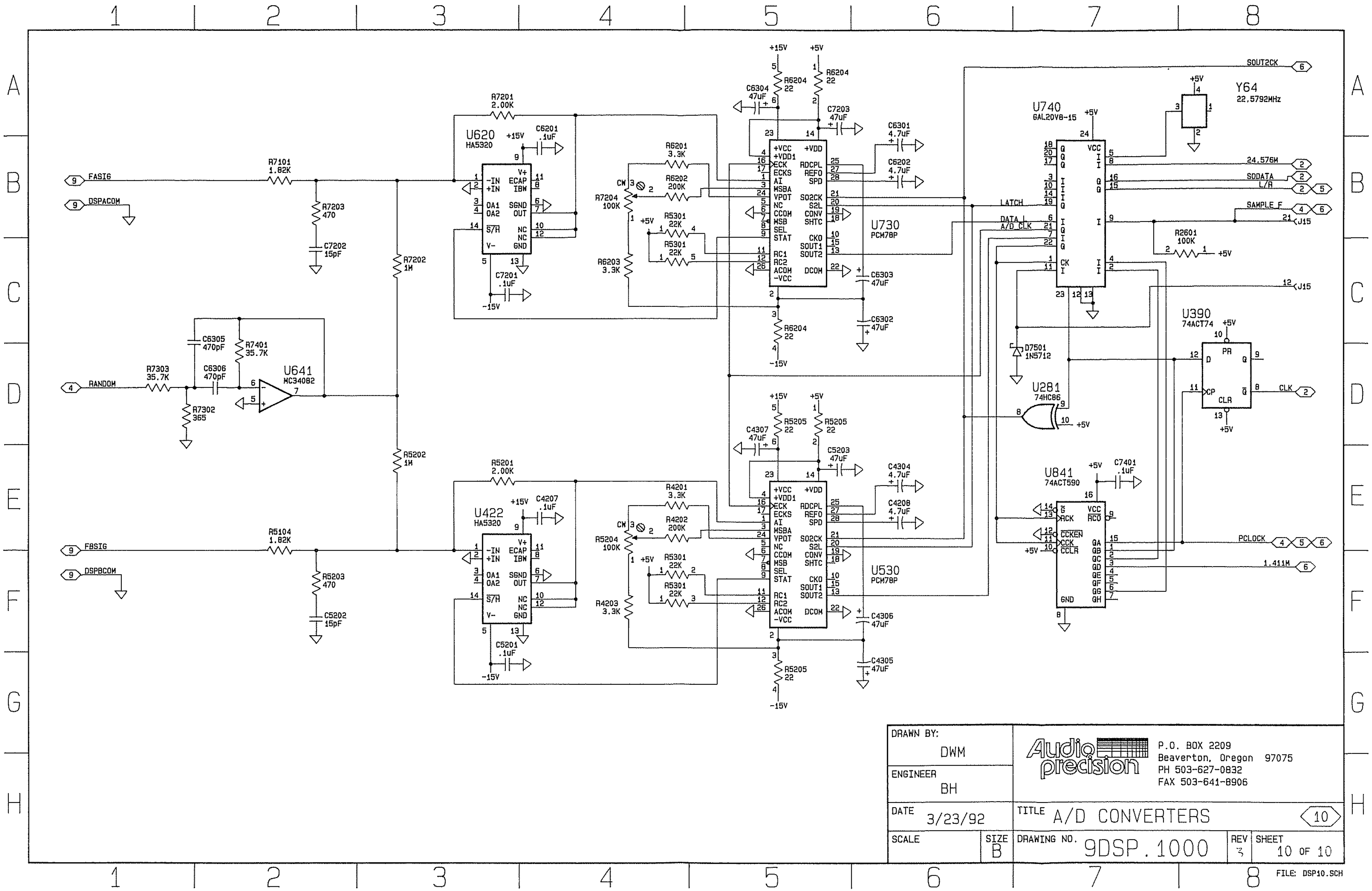
FILE: DSP9.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.1000 (6400.DSP1.3)

① Parts on solder side.

② Parts on component side.



DRAWN BY: DWM

ENGINEER: BH

DATE: 3/23/92

SCALE

SIZE: B

Audio precision

P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

TITLE: A/D CONVERTERS (10)

DRAWING NO. 9DSP.1000

REV 3

SHEET 10 OF 10

FILE: DSP10.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	8G2	2172.0689	CAP CERAM 100V 20%	6.8pF
C1301	7B1	2276.0102	CAP MICA 100V 1%	.001uF
C1401	6F7	2172.0104	CAP CERAM 100V 20%	.1uF
C1402	1B6	2932.0476	CAP AL-EL 25V 20%	47uF
C1403	6B5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C1404	6B6	2932.0476	CAP AL-EL 25V 20%	47uF
C1405	6C6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1407	6F6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1409	6E6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1410	1B7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1411	6E7	2172.0104	CAP CERAM 100V 20%	.1uF
C1501	1B7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1502	1B4	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1601	1B3	2942.0475	CAP AL-EL 35V 20%	4.7uF
C1602	1B5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C1801	6B4	2172.0104	CAP CERAM 100V 20%	.1uF
C2101	8E2	2172.0104	CAP CERAM 100V 20%	.1uF
C2102	8F2	2172.0104	CAP CERAM 100V 20%	.1uF
C2103	8E2	2172.0689	CAP CERAM 100V 20%	6.8pF
C2104	8E1	2932.0476	CAP AL-EL 25V 20%	47uF
C2105	8E1	2932.0476	CAP AL-EL 25V 20%	47uF
C2201	7D6	2454.0105	CAP POLYE 50V 5%	1uF
C2202	7D6	2454.0105	CAP POLYE 50V 5%	1uF
C2203	7C6	2555.0272	CAP POLYP 50V 2%	.0027uF
C2204	7B7	2555.0272	CAP POLYP 50V 2%	.0027uF
C2205	7B6	2276.0102	CAP MICA 100V 1%	.001uF
C2206	7B5	2276.0102	CAP MICA 100V 1%	.001uF
C2207	7B6	2276.0102	CAP MICA 100V 1%	.001uF
C2208	7C5	2276.0102	CAP MICA 100V 1%	.001uF
C2209	7D5	2172.0104	CAP CERAM 100V 20%	.1uF
C2210	7C3	2294.0100	CAP MICA 500V 5%	10pF
C2301	7D3	2276.0102	CAP MICA 100V 1%	.001uF
C2302	7C4	2172.0104	CAP CERAM 100V 20%	.1uF
C2303	7D3	2276.0102	CAP MICA 100V 1%	.001uF
C2304	7D3	2276.0102	CAP MICA 100V 1%	.001uF
C2305	7C2	2276.0102	CAP MICA 100V 1%	.001uF
C2306	7B4	2276.0102	CAP MICA 100V 1%	.001uF
C2307	7B2	2276.0102	CAP MICA 100V 1%	.001uF
C2308	6D6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2401	6E6	2172.0104	CAP CERAM 100V 20%	.1uF
C2402	6D7	2172.0104	CAP CERAM 100V 20%	.1uF
C2403	1B1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2701	1F4	2172.0104	CAP CERAM 100V 20%	.1uF
C2702	1G4	2172.0104	CAP CERAM 100V 20%	.1uF
C2801	1G3	2172.0104	CAP CERAM 100V 20%	.1uF
C2802	3E2	2172.0104	CAP CERAM 100V 20%	.1uF
C2901	1F2	2172.0104	CAP CERAM 100V 20%	.1uF
C3101	8H4	2172.0104	CAP CERAM 100V 20%	.1uF
C3102	9E8	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	9F3	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	9E7	2296.0271	CAP MICA 500V 1%	270pF
C3302	9F6	2276.0102	CAP MICA 100V 1%	.001uF

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C3303	9F7	2454.0103	CAP POLYE 50V 5%	.01uF
C3304	9D7	2172.0104	CAP CERAM 100V 20%	.1uF
C3305	4A6	2172.0104	CAP CERAM 100V 20%	.1uF
C3401	6C6	2172.0104	CAP CERAM 100V 20%	.1uF
C3501	4A4	2172.0104	CAP CERAM 100V 20%	.1uF
C3601	3A4	2172.0104	CAP CERAM 100V 20%	.1uF
C3602	2C7	2172.0104	CAP CERAM 100V 20%	.1uF
C3701	3A3	2172.0104	CAP CERAM 100V 20%	.1uF
C3702	3A2	2172.0104	CAP CERAM 100V 20%	.1uF
C3901	1F3	2172.0104	CAP CERAM 100V 20%	.1uF
C4101	9E2	2276.0102	CAP MICA 100V 1%	.001uF
C4102	8D7	2932.0476	CAP AL-EL 25V 20%	47uF
C4201	9E3	2276.0102	CAP MICA 100V 1%	.001uF
C4202	9F2	2276.0102	CAP MICA 100V 1%	.001uF
C4203	9F4	2294.0100	CAP MICA 500V 5%	10pF
C4204	9E4	2276.0102	CAP MICA 100V 1%	.001uF
C4205	9F4	2276.0102	CAP MICA 100V 1%	.001uF
C4207	10E4	2172.0104	CAP CERAM 100V 20%	.1uF
C4208	10E6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4301	9E6	2276.0102	CAP MICA 100V 1%	.001uF
C4302	9F5	2276.0102	CAP MICA 100V 1%	.001uF
C4303	9E7	2454.0334	CAP POLYE 50V 5%	.33uF
C4304	10E6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4305	10G6	2932.0476	CAP AL-EL 25V 20%	47uF
C4306	10F6	2932.0476	CAP AL-EL 25V 20%	47uF
C4307	10D5	2932.0476	CAP AL-EL 25V 20%	47uF
C4401	4A2	2172.0104	CAP CERAM 100V 20%	.1uF
C4402	5F2	2172.0104	CAP CERAM 100V 20%	.1uF
C4403	5C3	2172.0470	CAP CERAM 100V 20%	47pF
C4501	5C2	2172.0104	CAP CERAM 100V 20%	.1uF
C4502	4D2	2172.0104	CAP CERAM 100V 20%	.1uF
C4901	1B5	2172.0104	CAP CERAM 100V 20%	.1uF
C5201	10G3	2172.0104	CAP CERAM 100V 20%	.1uF
C5202	10F2	2294.0150	CAP MICA 500V 5%	15pF
C5203	10E5	2932.0476	CAP AL-EL 25V 20%	47uF
C5301	4F4	2172.0104	CAP CERAM 100V 20%	.1uF
C5601	3A5	2172.0104	CAP CERAM 100V 20%	.1uF
C5602	1B1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5701	3A6	2172.0104	CAP CERAM 100V 20%	.1uF
C5702	2E3	2172.0104	CAP CERAM 100V 20%	.1uF
C5801	3A7	2172.0104	CAP CERAM 100V 20%	.1uF
C5802	2E5	2172.0104	CAP CERAM 100V 20%	.1uF
C5901	1B2	2911.0108	CAP AL-EL 10V +80/-20%	1000uF
C6201	10B4	2172.0104	CAP CERAM 100V 20%	.1uF
C6202	10B6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6301	10B6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6302	10C6	2932.0476	CAP AL-EL 25V 20%	47uF
C6303	10C6	2932.0476	CAP AL-EL 25V 20%	47uF
C6304	10A5	2932.0476	CAP AL-EL 25V 20%	47uF
C6305	10C1	2296.0471	CAP MICA 500V 1%	470pF
C6306	10D2	2296.0471	CAP MICA 500V 1%	470pF
C6401	8A5	2172.0104	CAP CERAM 100V 20%	.1uF

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C6403	5F4	2276.0102	CAP MICA 100V 1%	.001uF
C6501	3D5	2172.0104	CAP CERAM 100V 20%	.1uF
C6701	2D1	2172.0104	CAP CERAM 100V 20%	.1uF
C6702	2C3	2172.0104	CAP CERAM 100V 20%	.1uF
C6703	2D3	2172.0104	CAP CERAM 100V 20%	.1uF
C6704	2B1	2172.0104	CAP CERAM 100V 20%	.1uF
C6705	2B1	2296.0101	CAP MICA 500V 1%	100pF
C6801	2D7	2172.0104	CAP CERAM 100V 20%	.1uF
C6802	2C5	2172.0104	CAP CERAM 100V 20%	.1uF
C6803	2C5	2172.0104	CAP CERAM 100V 20%	.1uF
C6804	2B7	2172.0104	CAP CERAM 100V 20%	.1uF
C6805	2B7	2296.0101	CAP MICA 500V 1%	100pF
C6806	2B7	2296.0101	CAP MICA 500V 1%	100pF
C6901	1D5	2172.0104	CAP CERAM 100V 20%	.1uF
C7101	8C6	2172.0104	CAP CERAM 100V 20%	.1uF
C7102	8A7	2172.0104	CAP CERAM 100V 20%	.1uF
C7103	9A2	2276.0102	CAP MICA 100V 1%	.001uF
C7104	8D7	2932.0476	CAP AL-EL 25V 20%	47uF
C7201	10C3	2172.0104	CAP CERAM 100V 20%	.1uF
C7202	10C2	2294.0150	CAP MICA 500V 5%	15pF
C7203	10A5	2932.0476	CAP AL-EL 25V 20%	47uF
C7204	9B3	2276.0102	CAP MICA 100V 1%	.001uF
C7205	9C2	2276.0102	CAP MICA 100V 1%	.001uF
C7206	9C4	2294.0100	CAP MICA 500V 5%	10pF
C7207	9B4	2276.0102	CAP MICA 100V 1%	.001uF
C7208	9C4	2276.0102	CAP MICA 100V 1%	.001uF
C7301	9B6	2276.0102	CAP MICA 100V 1%	.001uF
C7302	9C5	2276.0102	CAP MICA 100V 1%	.001uF
C7303	9B7	2454.0334	CAP POLYE 50V 5%	.33uF
C7304	5F5	2172.0104	CAP CERAM 100V 20%	.1uF
C7305	5F6	2276.0102	CAP MICA 100V 1%	.001uF
C7401	10E7	2172.0104	CAP CERAM 100V 20%	.1uF
C7501	5A6	2172.0104	CAP CERAM 100V 20%	.1uF
C7601	3D5	2172.0104	CAP CERAM 100V 20%	.1uF
C7801	2B5	2172.0104	CAP CERAM 100V 20%	.1uF
C7901	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C8201	9B4	2172.0104	CAP CERAM 100V 20%	.1uF
C8301	9B7	2296.0271	CAP MICA 500V 1%	270pF
C8302	9B6	2276.0102	CAP MICA 100V 1%	.001uF
C8303	9C6	2172.0104	CAP CERAM 100V 20%	.1uF
C8304	9C7	2454.0103	CAP POLYE 50V 5%	.01uF
C8401	1B3	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C8500	5A5	2172.0104	CAP CERAM 100V 20%	.1uF
C8501	2E4	2172.0104	CAP CERAM 100V 20%	.1uF
C8901	1B2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C8902	1E1	2276.0102	CAP MICA 100V 1%	.001uF
C8903	1D2	2296.0471	CAP MICA 500V 1%	470pF
D1101	8H3	3110.4152	DIODE SIGNAL	4152
D1102	8G3	3110.4152	DIODE SIGNAL	4152
D1401	7G7	3110.4152	DIODE SIGNAL	4152
D1501	7E2	3110.4152	DIODE SIGNAL	4152

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION		
D1502	1A6	3110.4152	DIODE SIGNAL		4152
D1503	1A3	3110.4152	DIODE SIGNAL		4152
D1504	1A6	3110.4152	DIODE SIGNAL		4152
D2101	8E3	3110.4152	DIODE SIGNAL		4152
D2102	8F3	3110.4152	DIODE SIGNAL		4152
D2103	7A7	3110.4152	DIODE SIGNAL		4152
D2104	7B7	3110.4152	DIODE SIGNAL		4152
D2901	1E1	3120.0000	DIODE SCHOTTKY		1SS97
D4401	5F3	3120.0000	DIODE SCHOTTKY		1SS97
D7401	5G5	3120.0000	DIODE SCHOTTKY		1SS97
D7501	10D7	3120.0000	DIODE SCHOTTKY		1SS97
D8901	1F4	3120.0000	DIODE SCHOTTKY		1SS97
D8902	1B3	3111.4001	DIODE POWER 1A 50V		4001
J131	1A8,1B8	4221.1008	JACK PC 2 X .1		8 PIN
J15	1E8,3F8,5B1,5B8	4221.1024	JACK PC 2 X .1		24 PIN
J84	2E-G1	4221.1024	JACK PC 2 X .1		24 PIN
J96	2B-C1	4221.1024	JACK PC 2 X .1		24 PIN
K120	7E7,7F7	4530.0002.1	RELAY		DPDT
K220	7E2,7E5	4530.0002.1	RELAY		DPDT
P11	8G1	4221.0036	PLUG PC	.1 X.43	36 PIN
P121	7B8	4221.0036	PLUG PC	.1 X.43	36 PIN
P122	7E8	4221.0036	PLUG PC	.1 X.43	36 PIN
P151	7G8	4221.0036	PLUG PC	.1 X.43	36 PIN
P19	2A1,6B1	4221.0036	PLUG PC	.1 X.43	36 PIN
P21	8F1	4221.0036	PLUG PC	.1 X.43	36 PIN
P25	4D-E5	4221.0072	PLUG PC	2X.1 X.43	72 PIN
P491	1H2	4221.0036	PLUG PC	.1 X.43	36 PIN
P492	1A-H1	4151.1740	CABLE ASSY .05	RBN 17	40 COND
P610	8B1	4221.0036	PLUG PC	.1 X.43	36 PIN
P611	8C1	4221.0036	PLUG PC	.1 X.43	36 PIN
P612	8D1	4221.0036	PLUG PC	.1 X.43	36 PIN
P710	8C1	4221.0036	PLUG PC	.1 X.43	36 PIN
P711	8C1	4221.0036	PLUG PC	.1 X.43	36 PIN
P84		4221.0036	PLUG PC	.1 X.43	36 PIN
Q1401	7F7	3211.2222	XSTR NPN TO92		PN2222A
Q1501	7E2	3211.2222	XSTR NPN TO92		PN2222A
Q2901	6D2	3211.2222	XSTR NPN TO92		PN2222A
Q4501	4E1	3211.2222	XSTR NPN TO92		PN2222A
Q4901	1G3	3211.2222	XSTR NPN TO92		PN2222A
R1101	8H2	1136.1003	RES 1/8W M FLM 1%		100K
R1102	8G2	1214.0472	RES 1/4W C FLM 5%		4.7K
R1103	8G3	1214.0510	RES 1/4W C FLM 5%		51
R1104	8G3	1214.0512	RES 1/4W C FLM 5%		5.1K
R1201	7B7	1214.0561	RES 1/4W C FLM 5%		560
R1203	7C6	1136.7872	RES 1/8W M FLM 1%		78.7K
R1204	7E6	1136.1052	RES 1/8W M FLM 1%		10.5K
R1205	7C7	1136.1270	RES 1/8W M FLM 1%		127

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R1206	7C6	1136.2261	RES 1/8W M FLM 1%	2.26K
R1207	7B5	1136.7500	RES 1/8W M FLM 1%	750
R1208	7C5	1139.1001	RES 1/8W M FLM .1%	1.00K
R1209	7C4	1136.1911	RES 1/8W M FLM 1%	1.91K
R1210	7C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R1301	7B4	1136.2741	RES 1/8W M FLM 1%	2.74K
R1302	7C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R1303	7C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R1304	7C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R1305	7C2	1136.2491	RES 1/8W M FLM 1%	2.49K
R1306	7C2	1139.1001	RES 1/8W M FLM .1%	1.00K
R1307	7B1	1139.2003	RES 1/8W M FLM .1%	200K
R1308	7B2	1136.1821	RES 1/8W M FLM 1%	1.82K
R1310	7B2	1136.2430	RES 1/8W M FLM 1%	243
R1311	7B1	1139.2003	RES 1/8W M FLM .1%	200K
R1401	6C7	1136.2003	RES 1/8W M FLM 1%	200K
R1402	6E7	1136.2003	RES 1/8W M FLM 1%	200K
R1404	6B5	1214.0229	RES 1/4W C FLM 5%	2.2
R1405	6B6	1214.0229	RES 1/4W C FLM 5%	2.2
R1406	7F6	1214.0103	RES 1/4W C FLM 5%	10K
R1501	7E1	1214.0103	RES 1/4W C FLM 5%	10K
R1502	1B6	1136.9090	RES 1/8W M FLM 1%	909
R1503	1A6	1136.2740	RES 1/8W M FLM 1%	274
R1504	1B4	1136.9090	RES 1/8W M FLM 1%	909
R1505	1A4	1136.2740	RES 1/8W M FLM 1%	274
R1603	4A7	1214.0203	RES 1/4W C FLM 5%	20K
R1801	6D2	1214.0203	RES 1/4W C FLM 5%	20K
R1802	5B7	1114.0470	RES 1/4W C FLM 5%	47
R1803	5B7	1114.0470	RES 1/4W C FLM 5%	47
R2101	8F2	1136.1003	RES 1/8W M FLM 1%	100K
R2102	8F2	1214.0472	RES 1/4W C FLM 5%	4.7K
R2103	8F3	1214.0510	RES 1/4W C FLM 5%	51
R2104	8E2	1214.0512	RES 1/4W C FLM 5%	5.1K
R2106	7E6	1136.1501	RES 1/8W M FLM 1%	1.50K
R2107	7E7	1136.1402	RES 1/8W M FLM 1%	14.0K
R2108	7E7	1139.2001	RES 1/8W M FLM .1%	2.00K
R2201	7D7	1136.2672	RES 1/8W M FLM 1%	18.7K
R2202	7B6	1139.2001	RES 1/8W M FLM .1%	2.00K
R2203	7B5	1136.1401	RES 1/8W M FLM 1%	1.40K
R2301	7C5	1139.2003	RES 1/8W M FLM .1%	200K
R2302	7B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R2303	7B3	1136.3091	RES 1/8W M FLM 1%	3.09K
R2304	7C2	1139.1001	RES 1/8W M FLM .1%	1.00K
R2305	6E7	4413.0104	POT TRIM PC 10 TURN	100K6F7
R2306	6C7	4413.0104	POT TRIM PC 10 TURN	100K
R2307	6E7	1136.4993	RES 1/8W M FLM 1%	499K
R2308	6C6	1136.4993	RES 1/8W M FLM 1%	499K
R2601	2E8,10C8	1984.9104	RES NET SIP 5% B	9 X 100K
R2602	2C8	1984.9104	RES NET SIP 5% B	9 X 100K
R2701	2B8	1984.9104	RES NET SIP 5% B	9 X 100K
R2702	2A3	1214.0103	RES 1/4W C FLM 5%	10K
R2801	3E2	1214.0202	RES 1/4W C FLM 5%	2.0K

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R2901	3F3	1214.0103	RES 1/4W C FLM 5%	10K
R2902	6D2	1214.0203	RES 1/4W C FLM 5%	20K
R3101	9E2	1139.2003	RES 1/8W M FLM .1%	200K
R3102	9E2	1136.1821	RES 1/8W M FLM 1%	1.82K
R3103	9E2	1139.2003	RES 1/8W M FLM .1%	200K
R3104	9E2	1136.2430	RES 1/8W M FLM 1%	243
R3105	9D7	1214.0153	RES 1/4W C FLM 5%	15K
R3106	8E7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3107	8E7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3108	8F7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3109	8F7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3110	9F2	1136.2371	RES 1/8W M FLM 1%	2.37K
R3111	9F2	1139.1001	RES 1/8W M FLM .1%	1.00K
R3201	9F2	4412.0201	POT TRIM PC ENC	200
R3202	9F3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3203	9E3	1136.3091	RES 1/8W M FLM 1%	3.09K
R3204	9E4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3205	9F4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3206	9F3	1139.2001	RES 1/8W M FLM .1%	2.00K
R3207	9F4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3208	9F5	1139.1003	RES 1/8W M FLM .1%	100K
R3209	9F5	1139.2001	RES 1/8W M FLM .1%	2.00K
R3210	9F5	1139.1001	RES 1/8W M FLM .1%	1.00K
R3211	9E5	1136.7500	RES 1/8W M FLM 1%	750
R3212	9E5	1136.2741	RES 1/8W M FLM 1%	2.74K
R3213	9F6	1139.1001	RES 1/8W M FLM .1%	1.00K
R3301	9E7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3302	9F7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3303	9F7	1136.1782	RES 1/8W M FLM 1%	17.8K
R3304	9E6	1136.1401	RES 1/8W M FLM 1%	1.40K
R3901	1G3	1214.0103	RES 1/4W C FLM 5%	10K
R4101	7A7	1214.0510	RES 1/4W C FLM 5%	51
R4201	10E4	1214.0332	RES 1/4W C FLM 5%	3.3K
R4202	10E4	1214.0204	RES 1/4W C FLM 5%	200K
R4203	10F4	1214.0332	RES 1/4W C FLM 5%	3.3K
R4301	8A2	1214.0203	RES 1/4W C FLM 5%	20K
R4401	5F3	1214.0202	RES 1/4W C FLM 5%	2.0K
R4501	4E1	1214.0103	RES 1/4W C FLM 5%	10K
R4502	4F2	1136.4991	RES 1/8W M FLM 1%	4.99K
R4901	2D4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R5101	8F1,8H1	1984.9680	RES NET SIP 5% B	9 X 68
R5102	8A2	1214.0134	RES 1/4W C FLM 5%	130K
R5103	8B3	1214.0102	RES 1/4W C FLM 5%	1K
R5104	10E2	1136.1821	RES 1/8W M FLM 1%	1.82K
R5201	10E3	1139.2001	RES 1/8W M FLM .1%	2.00K
R5202	10F2	1214.0105	RES 1/4W C FLM 5%	1M
R5203	10G2	1214.0471	RES 1/4W C FLM 5%	470
R5204	10E4	4413.0104	POT TRIM PC 10 TURN	100K
R5205	10G5,10D5	1984.4220	RES NET SIP 5% I	4 X 22
R5301	10F4,10C4	1985.4223	RES NET SIP 2% B	4 X 22K
R5601	2F3	1985.4223	RES NET SIP 2% B	4 X 22K
R6201	10B4	1214.0332	RES 1/4W C FLM 5%	3.3K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R6202	10B4	1214.0204	RES 1/4W C FLM 5%	200K
R6203	10C4	1214.0332	RES 1/4W C FLM 5%	3.3K
R6204	10C5,10E5	1984.4220	RES NET SIP 5% I	4 X 22
R6401	5B2	1214.0470	RES 1/4W C FLM 5%	47
R6402	5C7	1214.0470	RES 1/4W C FLM 5%	47
R6403	5C5	1214.0103	RES 1/4W C FLM 5%	10K
R6404	5C6	1214.0103	RES 1/4W C FLM 5%	10K
R6405	5C5	1214.0103	RES 1/4W C FLM 5%	10K
R6406	5C7	1214.0103	RES 1/4W C FLM 5%	10K
R6407	5G6	1214.0201	RES 1/4W C FLM 5%	200
R6408	5F4	1214.0201	RES 1/4W C FLM 5%	200
R6501	2F7	1214.0000	RES 1/4W C FLM 5%	00
R6502	5B7	1114.0470	RES 1/4W C FLM 5%	47
R6503	5B7	1114.0470	RES 1/4W C FLM 5%	47
R7101	10B2	1136.1821	RES 1/8W M FLM 1%	1.82K
R7201	10A3	1139.2001	RES 1/8W M FLM .1%	2.00K
R7202	10C3	1214.0105	RES 1/4W C FLM 5%	1M
R7203	10B2	1214.0471	RES 1/4W C FLM 5%	470
R7204	10B4	4413.0104	POT TRIM PC 10 TURN	100K
R7302	10D1	1136.3650	RES 1/8W M FLM 1%	365
R7303	10D1	1136.3572	RES 1/8W M FLM 1%	35.7K
R7401	10D2	1136.3572	RES 1/8W M FLM 1%	35.7K
R7402	5G4	1214.0200	RES 1/4W C FLM 5%	20
R7403	5F4	1214.0303	RES 1/4W C FLM 5%	30K
R7404	5G4	1214.0103	RES 1/4W C FLM 5%	10K
R7405	5F4	1214.0103	RES 1/4W C FLM 5%	10K
R7406	5F3	1214.0471	RES 1/4W C FLM 5%	470
R7601	5B7	1114.0470	RES 1/4W C FLM 5%	47
R7602	5B7	1114.0470	RES 1/4W C FLM 5%	47
R7603	5B7	1114.0470	RES 1/4W C FLM 5%	47
R7901	1C-E3	1984.9103	RES NET SIP 5% B	9 X 10K
R7902	3F3	1214.0103	RES 1/4W C FLM 5%	10K
R8101	9B2	1139.2003	RES 1/8W M FLM .1%	200K
R8102	9A2	1136.1821	RES 1/8W M FLM 1%	1.82K
R8103	9B2	1139.2003	RES 1/8W M FLM .1%	200K
R8104	9B2	1136.2430	RES 1/8W M FLM 1%	243
R8105	8B7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8106	8B7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8107	8C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8108	8C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8109	9C2	1139.1001	RES 1/8W M FLM .1%	1.00K
R8110	9C2	1136.2491	RES 1/8W M FLM 1%	2.49K
R8111	9A7	1214.0153	RES 1/4W C FLM 5%	15K
R8201	9C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R8202	9A3	1136.3091	RES 1/8W M FLM 1%	3.09K
R8203	9B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R8204	9C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R8205	9C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R8206	9B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R8207	9C5	1136.1003	RES 1/8W M FLM 1%	100K
R8208	9C5	1139.2001	RES 1/8W M FLM .1%	2.00K

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R8209	9C5	1139.1001	RES 1/8W M FLM .1%	1.00K
R8210	9B5	1136.7500	RES 1/8W M FLM 1%	750
R8211	9A5	1136.2741	RES 1/8W M FLM 1%	2.74K
R8212	9B6	1139.1001	RES 1/8W M FLM .1%	1.00K
R8301	9B7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8302	9C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8303	9C7	1136.1782	RES 1/8W M FLM 1%	17.8K
R8304	9A6	1136.1401	RES 1/8W M FLM 1%	1.40K
R8305	5F6	1214.0201	RES 1/4W C FLM 5%	200
R8306	5F6	1214.0104	RES 1/4W/C/FLM 5%	100K
R8401	5F5	1214.0102	RES 1/4W C FLM 5%	1K
R8402	5B6	4412.0202	POT TRIM PC ENC	2K
R8403	5B6	1214.0202	RES 1/4W C FLM 5%	2.0K
R8404	5B7	1114.0470	RES 1/4W C FLM 5%	47
R8405	5B7	1114.0470	RES 1/4W C FLM 5%	47
R8501	2A3,2E4,2E5,2F4	1984.9472	RESNETSIP 5% B	9 X 4.7K
R8502	5A7	1114.0470	RES 1/4W C FLM 5%	47
R8503	5B7	1114.0470	RES 1/4W C FLM 5%	47
R8504	5B7	1114.0101	RES 1/4W C FLM 5%	100
R8601	2G3,2G5	1985.4223	RES NET SIP 2% B	4 X 22K
R8602	2G5	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R8603	2G5	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R8604	2D3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R8901	1F4	1214.0103	RES 1/4W C FLM 5%	10K
R8904	1E6	1214.0102	RES 1/4W C FLM 5%	1K
R8905	1F6	1214.0102	RES 1/4W C FLM 5%	1K
R8906	1F6	1214.0102	RES 1/4W C FLM 5%	1K
U130	6D7	3411.0844	OP AMP SINGLE	AD844
U150	1A6	3431.0337	VOLT REG NEG VAR TO220	LM337
U151	1A3	3430.1317	VOLT REG POS VAR TO92	LM317L
U180	6C4	3342.20V8	GENERIC ARRAY	GAL20V8-15
U190	6C3	3331.5803	DIGITAL FILTER	SM5803APT
U210	8F2,8G2	3412.5532	OP AMP DUAL	5532
U220	7B6,7E7	3412.5532	OP AMP DUAL	5532
U221	7B4,7C5	3412.5532	OP AMP DUAL	5532
U230	7B3,7C4	3412.5532	OP AMP DUAL	5532
U231	7B2,7C2	3412.5532	OP AMP DUAL	5532
U240	6E6	3441.0056	CONVERTER D/A 16-BIT	PCM56
U241	6C6	3441.0056	CONVERTER D/A 16-BIT	PCM56
U242	2F7,2F8,4E5	3326.0244	BUFFER 8X TRI-STATE	74ACT244
U280	1F4	3450.7705	SUPPLY VOLT SENSOR	5V
U281	3G2,5D3,10D7	3323.0086	GATE 4-IN EXCL OR	74HC86
U290	1G2	3342.16V8	GENERIC ARRAY	GAL16V8-15
U340	4B6	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U341	4D4	3325.0240	BUFFER 8X INV TRI-ST	74AC240
U350	4B4	3325.0240	BUFFER 8X INV TRI-ST	74AC240
U360	2E7	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U361	2D7	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U362	3B4	3722.6264	SRAM CMOS 25ns	8K X 8
U370	2B7	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U371	3B3	3722.6264	SRAM CMOS 25ns	8K X 8

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U380	3F2	3724.2864	EEPROM CMOS 350ns	8K X 8
U381	3B2	3722.6264	SRAM CMOS 25ns	8K X 8
U390	1G3,10D8	3326.0074	FLIP-FLOP 2X D	74ACT74
U410	8F7,9E8	3412.0353	OP AMP DUAL	TL072/LF353
U411	8F7,9E2	3412.5532	OP AMP DUAL	5532
U412	8G4	3323.4052	MULTIPLEX 4X DIFF	HC4052
U420	9F3,9E4	3412.5532	OP AMP DUAL	5532
U421	9F4,9E5	3412.5532	OP AMP DUAL	5532
U422	10F3	3441.5320	SAMPLE AND HOLD AMP	HA5320
U430	9F6,9E7	3412.5532	OP AMP DUAL	5532
U440	4B2	3326.0595	SHIFT REG 8BIT W/LAT	74ACT595
U441	5F2	3326.0590	COUNTER 8-BIT TRI-ST	74ACT590
U442	4C2	3326.0595	SHIFT REG 8BIT W/LAT	74ACT595
U443	5D2	3326.0590	COUNTER 8-BIT TRI-ST	74ACT590
U450	4E2	3326.0595	SHIFT REG 8BIT W/LAT	74ACT595
U451	4G2	3342.16V8	GENERIC ARRAY	GAL16V8-15
U460	3B5	3722.5256.1	SRAM CMOS 85ns	32K X 8
U470	3B6	3722.5256.1	SRAM CMOS 85ns	32K X 8
U480	3B7	3722.5256.1	SRAM CMOS 85ns	32K X 8
U490	1C7	3325.0670	REGISTER FILE 4X4	74AC670
U510	8E4	3323.4052	MULTIPLEX 4X DIFF	HC4052
U530	10F5	3441.0078	CONVERTER A/D 16-BIT	PCM78P
U540	4E6	3326.0794	REGISTER 8X W/READBK	74ACT794
U541	4C6	3326.0794	REGISTER 8X W/READBK	74ACT794
U550	5D4	3326.0794	REGISTER 8X W/READBK	74ACT794
U590	1C5	3325.0670	REGISTER FILE 4X4	74AC670
U610	8B4	3323.4051	MULTIPLEX 8X	HC4051
U611	8B6	3323.4052	MULTIPLEX 4X DIFF	HC4052
U612	8C7,9A8	3412.0353	OP AMP DUAL	TL072/LF353
U620	10B3	3441.5320	SAMPLE AND HOLD AMP	HA5320
U640	4G4	3326.0794	REGISTER 8X W/READBK	74ACT794
U641	8B5,10D2	3412.0082	OP AMP DUAL	MC34082
U642	3G5	3326.0138	DECODER 3-LN/8-LN	74ACT138
U650	5D6	3342.20V8	GENERIC ARRAY	GAL20V8-15
U651	3D6	3326.0138	DECODER 3-LN/8-LN	74ACT138
U660	3G4	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U661	3E4	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U670	2D2	3331.5600	uPROCESSOR	DSP56001
U680	2D6	3331.5600	uPROCESSOR	DSP56001
U690	1D5	3325.0670	REGISTER FILE 4X4	74AC670
U691	1F5	3324.0273	FLIP-FLOP 8X D	74HCT273
U710	8D6	3323.4052	MULTIPLEX 4X DIFF	HC4052
U711	8B7,8E7	3412.5532	OP AMP DUAL	5532
U712	8B7,9B2	3412.5532	OP AMP DUAL	5532
U720	9C3,9B4	3412.5532	OP AMP DUAL	5532
U721	9C4,9B5	3412.5532	OP AMP DUAL	5532
U730	10B5	3441.0078	CONVERTER A/D 16-BIT	PCM78P
U731	9C6,9B7	3412.5532	OP AMP DUAL	5532
U740	10B7	3342.20V8	GENERIC ARRAY	GAL20V8-15
U751	3F6	3326.0138	DECODER 3-LN/8-LN	74ACT138
U760	3E5	3341.20L8	PROG ARRAY	PLUSC20L8-7
U790	1D2	3324.0245	TRANSCVR 8X TRI-ST	74HCT245

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U840	5F4,5F5	3422.0319	COMPARATOR	LM319
U841	10F7	3326.0590	COUNTER 8-BIT TRI-ST	74ACT590
U850	5A6,5B6,5D7	3326.0008	GATE 4 X 2-IN AND	74ACT08
U860	2F4	3342.20V8	GENERIC ARRAY	GAL20V8-15
W122		4131.0185.9	CABLE 1 CND SHLD 18.5	2 PN WHT
W151		4123.0180	CABLE 1 COND UNSHLD 18"	1 PIN
W25		4151.3020	CABLE ASSY .05" RBN 30"	20 COND
W610		4131.0185	CABLE 1 CND SHLD 18.5	2 PN BLK
W611		4131.0185.6	CABLE 1 CND SHLD 18.5	2 PN BLU
W612		4131.0250.2	CABLE 1 CND SHLD 25"	2 PN RED
W710		4131.0250.4	CABLE 1 CND SHLD 25"	2 PN YEL
W711		4131.0185.5	CABLE 1 CND SHLD 18.5	2 PN GRN
W84		4132.0180	CABLE 2 COND SHLD 18"	3 PIN
Y64	10A8	3910.2258	OSCILLATOR CMOS	22.5792MHz
Y85	5A5	3910.2458	OSCILLATOR CMOS	24.576MHz

DSP-2 DIGITAL SIGNAL PROCESSING MODULE

DSP-2, DIGITAL SIGNAL PROCESSING MODULE

NOTE: There have been two versions of the DSP module. The version can be determined from the production code number located on the decal attached to the metal shield. The code number will have the format "DSPx-yyyyy-zz" where "x" is the DSP version.

Introduction

The DSP-2 module, diagrammed in Figure DSP2.1, provides a "dsp" (digital signal processor) core with both analog and digital input and output capabilities. The system is built around three digital signal processors, one for the dsp core functions, one for the analog interface and one for the digital interface. The dsp core and the analog input and output circuitry are on one circuit board. It normally occupies the compartment underneath the analog generator module in a System One. The DSP-2 module itself provides analog signal generation and measurement using on board D/A and A/D converters. In SYS-322 and SYS-302 configurations the DIO module adds additional memory and digital input and output functions. In SYS-222 and SYS-202 configurations the MEM option board provides additional memory only.

The Audio Precision System One provides all commonly used analog audio test and measurement functions. The DSP-2 module expands these functions into the digital audio domain, as well as enhancing the operation of the system for analog measurements. The digital signal processing can be used in conjunction with the System One analog notch filter to measure analog signals to a much wider dynamic range. For example the analog hardware can be used to remove the fundamental in a THD measurement and the dsp may then measure the harmonics individually, with a dynamic range far in excess of its A/D converters capabilities.

All dsp chips in the system are Motorola DSP56001 24-bit digital signal processors operating at 24.576 MHz. The manufacturer's block diagram is reproduced in Figure DSP2.2. It uses a 6-bus architecture for internal processing, providing separate address and data busses for program memory, and for two data memories. On chip resources include two 256-word data memories, a 256 point sine table, 512 words of zero wait state program memory, 24-bit serial inputs and outputs, an 8-bit host interface, interrupt controller with two external interrupts, a 24x24 multiplier and an ALU which supports double precision operations. A single external address and data bus are provided for expanding program or data memory size off chip.

The external busses of all three processors are tied together on the same expansion memory. A bus arbitrator controls access to the shared resources and prevents conflicts. Program memory is expanded to 8k words of 0 wait state static RAM and is used by the main dsp only. The other two dsps rely completely on their internal 512 word program memory. The DSP-2 board provides 32k words of additional static data RAM, split equally between X and Y data memory spaces. The DIO board adds another 64k words of static data RAM, again split equally between X and Y memory. The DSP-2 board also contains a hardware random number generator and simple real time clock. The data RAM and peripherals are available for use by all processors. Only the main and decimator dsps can communicate directly with the host personal computer.

A single ROM contains the program code which fills the internal program memory of all three processors. Each processor reads its respective portion of the ROM when released from reset and fills internal program memory. The main dsp can then communicate with the host computer to download larger programs into external program RAM as well as modifying its own internal RAM. This ROM also contains serial number information and calibration constants. The calibration information eliminates the need for offset or gain adjustments in the A/D converters.

The decimator dsp receives signals from two on board A/D converters and decimates the data to lower sampling rates. The A/D's always run at a 192 kilosample rate or a 176.4 kilosample rate. The decimator reduces these rates to 48 kHz, 44.1 kHz or 32 kHz for compatibility with professional audio sampling rates. This allows compatibility with all professional and consumer digital audio sampling rates. The decimator can also provide 8 kHz and 1 kHz sample rates for use when measuring very low frequency signals. Analog signals from the various portions of the System One analog measurement modules or from dedicated front panel inputs are routed to the anti-alias filters by CMOS switch selectors. The filters are designed to remove energy above 80 kHz before feeding the A/D converters. The converters are dithered by an analog output from the same random number generator which supplies the dsps with digital dither. After filtering, the decimator dsp passes its data serially to the main dsp for further processing.

In SYS-322 and SYS-302 configurations the third dsp processor located on the DIO board is used for AES/EBU communications. Data encoding, decoding, synchronization, parity checking, and extracting the serial status bit stream are accomplished by dedicated logic circuits. However, complete implementation of the AES/EBU interface requires the ability to write and read quite a few status bits in real time. These bits provide sample counts, pre-emphasis flags, channel allocation information, source and destination codes, etc. Additionally, it is necessary to send and receive pre-emphasized data.

The DIO board also contains parallel input and output ports for connection to external test circuits and dsp devices. Each port multiplexes two channels of data onto one set of 24 data lines. Each output channel is buffered by a two stage FIFO to prevent jitter in the transmitted data. Each input channel consists of latches which are written by the external device and read by the main dsp. A sample clock generator is provided to strobe the data inputs and outputs or an external clock may be used for either or both functions. The internal sample clock generator may be programmed for a variety of digital audio rates. Appropriate hardware generates interrupts for the processor when data is read from the output or received at the input.

The digital interface circuits, either AES/EBU or parallel, serve the same function as the balancing amplifiers in an analog system. They provide an interface between the format of the device under test and the internal hardware of the test equipment. They also double buffer data to allow for timing differences between the two pieces of equipment.

PC/Host Computer Interface <1>

Power, address and data from the System One mainframe enters on connector P39. The data bus from the System One interface is buffered by tri-state transceiver U791. The same signal which enables U791 is used to drive the wired-OR attention feature of the System One interface through D2901. Resistor network R7901 prevents the host data bus from drifting to intermediate logic levels when it is tri-stated, reducing power consumption.

The DSP-2 module occupies module address 3 on the System One interface. Each System One module address has associated with it 16 individual data addresses. The upper four bits of the eight bit address bus are used to decode the module address. The lower four address bits are used to select one of 16 addresses on the board. These addresses are decoded by U292.

Reset generator U390 provides the power up reset signal to the processors and guards the EEROM memory against writes during power-up and power-down cycles. If the +5 Volt power supply drops below 4.75 Volts the open collector output on pin 5 will go low, clearing octal latch U790. The PROTECT signal on pin 6 is an open collector pnp transistor output which simultaneously goes high. This is used to clamp the write enable pin of EEROM U380, preventing accidental modification of its contents. The mainframe reset signal /RST on connector P39 is combined with the supply voltage sensing to also force reset when it is asserted low.

The host data bus drives dual port register files U490, U491, and U590 and latch U790. Latch U790 is used to reset the dsps and bring them out of reset under control of the host computer. The lower two bits drive the reset lines of the two dsps on the DSP-2 board. The third bit resets the dsp on the DIO board in SYS-322/SYS-302 configurations.

The three register files are used to hold data from the dsps which can be read by the host computer to indicate when new readings are available. U491 and U590 are written to as 4 bit words by the dsp and are read as bytes by the host. To allow dsp read-modify-write instructions to be used on this data, U490 provides a read back function of the data written to either U491 or U590. When one of the processors writes to the register files flip-flop U291 is clocked low, asserting the open collector IRG line. When the host reads one of the register files the flip-flop is set, releasing the IRG line. All remaining communication between the host and the processors is accomplished through their host port interfaces.

The main processor U780 and the decimator processor U770 host ports (shown on schematic <2>) normally occupy 8 addresses each. U292 maps the main processor U780 into the lower 8 board addresses and the decimator processor into the upper 8. Pin 15 of U292 drives the main processor host port enable (/HEN), while pin 19 drives the decimator processor host port enable (/DHEN). Pin 16 provides a read/write signal for both processors (HR/W). The decoder U292 also maps other hardware functions on top of unused addresses in the processor host ports. The address map in TABLE 1 details this board address allocation. A special host port mode, used for dma transfers, is selected by the /HACK inputs of the processors. This is also decoded in U292.

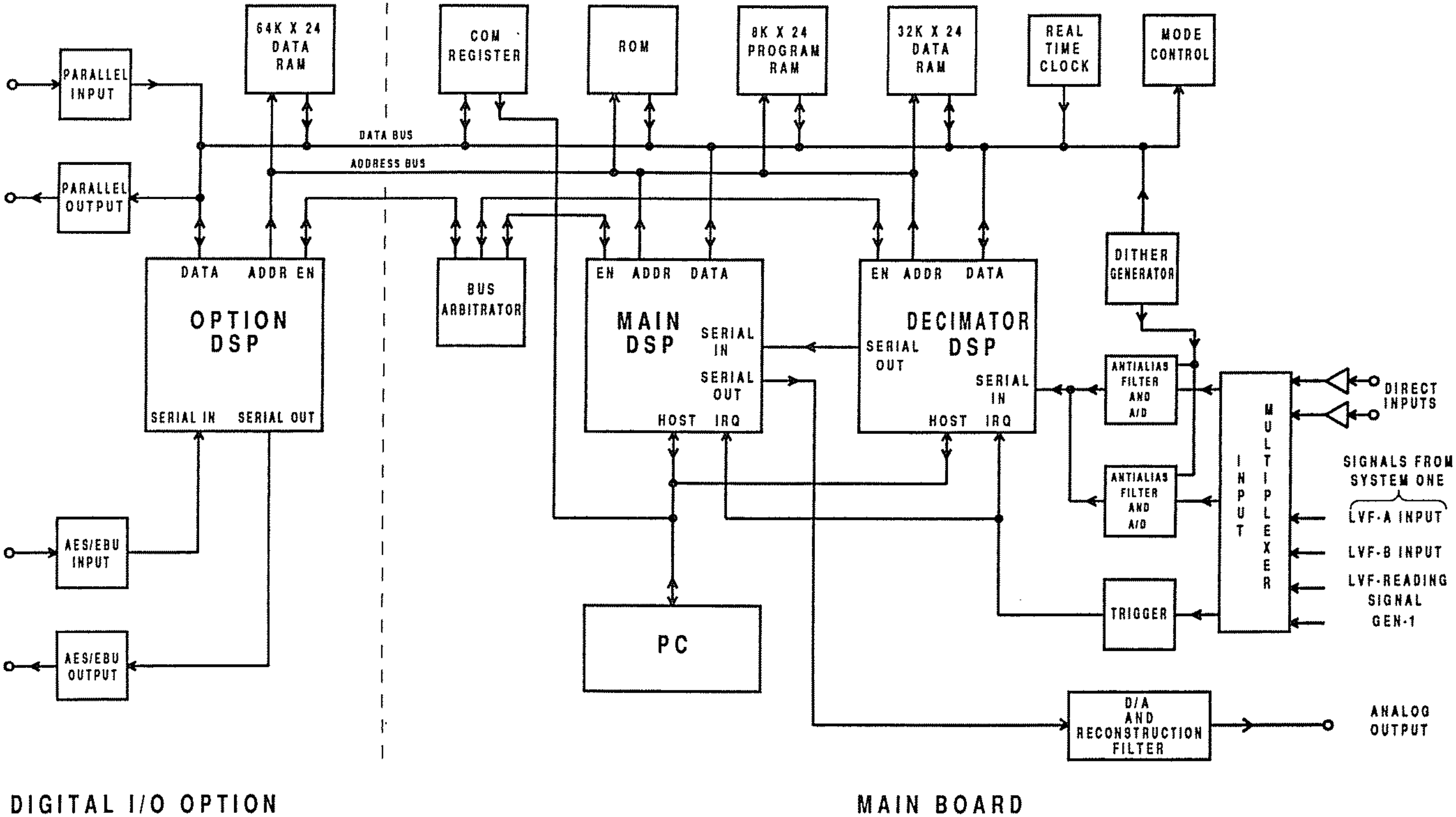


Figure DSP2.1 DSP-2 BLOCK DIAGRAM

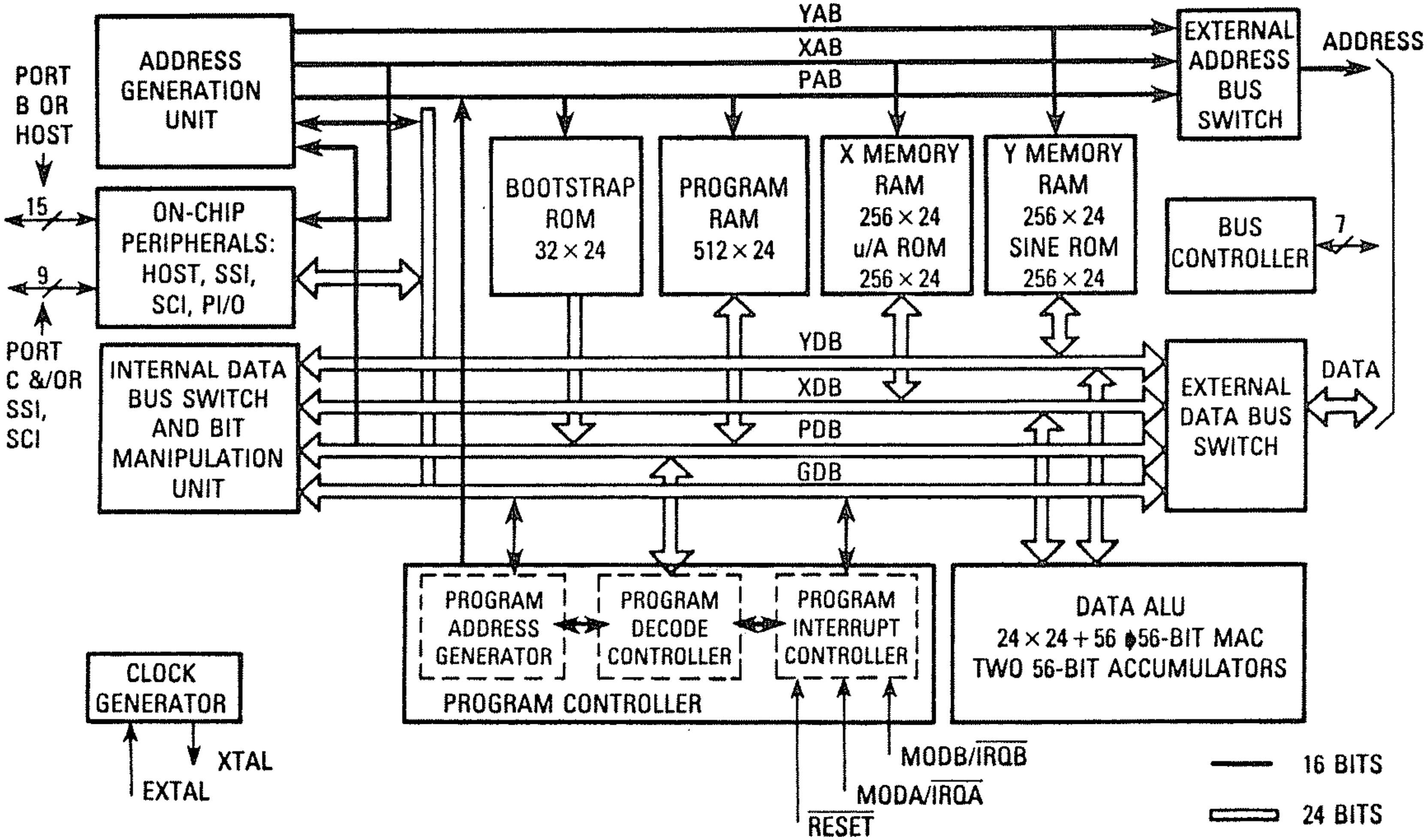


Figure DSP2.2 DSP56001 BLOCK DIAGRAM

Low Voltage Power Supplies <1>

The ±15 Volt supplies are regulated down to ±6 Volts by U141 and U241. Diodes D2402 and D2403 provide reverse voltage protection. Capacitors C1404 and C1405 bypass the 15 Volt supplies and insure low inductance supply inputs. Resistor dividers R2401/R2402 and R2403/R2404 set the output voltages to approximately 5.8 volts. Output bypass capacitors C2402 and C2401 reduce the supply impedances at high frequencies. Capacitor C1402 and C1403 reduce output noise on the negative supply, a critical parameter for the D/A converters. Diode D2401 prevents damage to the regulator during power down.

Processors and Bus Arbitration <2>

The dsp data bus is buffered by tri-state octal transceivers U372, U370 and U361. Programmable logic device U660 arbitrates between the three processors for access to the common address and data bus. Each processor has three pins dedicated to bus arbitration; bus request out (/BUSREQ#), bus enable in (BUSEN#) and bus grant out (/BUSGT#) where # represents the processor number. The bus request output pin is pulled low by the processor to signal the arbitrator that access is needed. The bus enable input is driven high by the arbitrator to allow access to the bus. The bus grant output goes low to signal that bus access is given up. The arbitrator normally examines the state of each bus request and bus grant to determine which processor needs the bus and which currently has the bus. However when the memory select bits MEM1 and MEM0 are asserted during boot from EEROM they force the arbitrator to give access to the appropriate processor regardless of the bus request signal states. During normal operation the bus access priority is set by the three bits PTY2, PTY1, and PTY0 from U281 on schematic <4>. When a processor with higher priority than the one currently using the bus requests bus access the arbitrator takes access away from the current user. After the current user has released the bus, the arbitrator gives the bus to the highest priority requestor. Arbitrator pin 21 is asserted when the bus is idle (no processors currently given access). This state should occur for one clock cycle between any change in bus access. Pin 22 is asserted if any two or three processors claim access at the same time, representing an error condition.

Memory and Address Decode <3>

The address bus is buffered by U561 and U560, shown on schematic <3>. The unbuffered data lines drive the RAMs on the DSP-2 board and are extended through connector J88 to the optional DIO or MEM boards. These RAMs consist of one bank of three 8k-by-8 program memories U460, U470 and U480 and one bank of three 32k-by-8 data memories U570, U571, and U580. The RAM address lines are all driven from the buffered address bus. The lower 13 buffered address lines drive the program RAMs directly, the lower 14 lines are used to drive the data RAMs. The most significant bit of the data RAM address is derived from the X/Y memory select line. Programmable array logic chip U762 acts as a very high speed address decoder. The upper 8 unbuffered address lines and some of the lower address lines are used to decode the various memory enable signals and the buffer enable signals. The enable for the I/O buffers is further decoded by U651 and U750 to create individual enable signals for the I/O devices on the DSP-2 board. U651 decodes read operations while U750 decodes write operations.

EEROM U380 contains the boot code for each of the three processors. It is enabled by address decoder U761. The lower 11 buffered address lines directly drive the lower 11 address inputs of the ROM. The two most significant ROM address lines pass through two sections of exclusive OR U550. The other inputs of the exclusive OR come from latch U790 under control of the host computer. This allows the host to map any one of four pieces of the EEROM to the base address ($C000) used by the dsp processors when they boot. These two memory select lines are also used to drive the bus priority logic, described later, giving control of memory to the processor being brought out of reset. The eight data lines of the EEROM are connected to buffered data lines D0 through D7. The processor automatically reads three consecutive addresses from the ROM, starting at $C000, and uses these bytes to fill one location of internal program RAM. This is repeated at succeeding ROM addresses until internal program memory is filled. The processor then begins executing the code loaded into internal memory. After the processors are operational, the host computer may load additional memory locations as required.

Random Number Generator <4>

Programmable logic device U351 and shift registers U280, U261 and U251 form a maximum length pseudo-random number generator. This is used to generate uniformly distributed random numbers for use in digital dither and to provide analog dither to the A/D converters. U351 contains a 7-bit shift register and a multiple input exclusive NOR gate to provide feedback. Shift registers U280 and U261 are cascaded with the internal shift register to lengthen the sequence to 23 bits. Shift register U251 shadows the data in U351s internal flip flops. The generated data is latched by additional latches in U280, U261 and U251 when /BRD goes high to guarantee that the data does not change during a read operation. The outputs are tri-stated until /RNDRD is asserted low during a read from the generator. A tri-state buffer in U351 copies the most significant bit from U251 and outputs it into the sign bit of the data word. This guarantees that the random values are always between ±0.5. The /RNDRST signal resets the shift registers to guarantee startup on power up or to allow restarting under program control. One of the shift register outputs is gated by transistor Q3401 and filtered by U640 (located on schematic <10>) to produce an analog dither signal for the A/D converters. The /DITHER signal shuts this analog dither down when asserted high.

DIS Signal Monitor <4>

The 16-bit value used to program the tuning DACs on the DIS module is routed through a cable via P25. Also on this cable are four signals from the 6805 microprocessor on the LVF board which indicate when a change in level range occurs. Octal tri-state inverting buffers U262 and U250 buffer the bandpass/notch filter frequency and compensate for the complemented data format in the DIS mdacs. Half of octal buffer U181 buffers the four range-change indication signals. Read enable signal /DISFREQ activates all three buffers when low, placing the data on the bus.

Mode and MUX Control <4>

Octal latch U281 latches bus priority and sample rate control bits. It is strobed by /MEMW when the processor performs a write operation to the appropriate memory location. These latches may be read back by the processor when a read is performed from the same address. This readback is enabled by /MEMR.

Octal latches U270 and U260 latch input and trigger selection control bits. Also included on latch U260 are the data memory page control and the dither enable signals. They are strobed by /MODE when the processor performs a write operation to the appropriate memory location. These latches may be read back by the processor when a read is performed from the same address. This readback is enabled by /MODR.

Read-modify-write instructions are used by the processors to set the latches. Any failure of the readback function may cause bad data to be written into the defective latch.

Status Bits <4>

Octal buffer U371 monitors various status bits on the DSP board. Bits 0 and 1 monitor the bus request activity of the main and decimator processors respectively so that the processor in control of the bus may check to see if other access is requested. A high level on bit 2 indicates that the host computer has routed the D/A converter output through the analog generator. This is used to override the digital output level and resolution if necessary. The trigger signal is available on bit 3 for the processor to use in programs as required.

The YRAM signal on bit 4 is used to determine the presence or absence of an option board. The buffer may be read from either of two addresses, one odd and one even. A resistor from the lowest buffered address line is used to pull the input high or low, depending on the address accessed. If a read from the odd address finds the bit high and a read from the even address finds it low there is no option board present. If a read from either address finds the bit high, the MEM option is present. If a read from either address finds the bit low, the DIO module is present.

Bits 5 and 6 monitor the memory selection bits MEM0 and MEM1 to let the processors know when the boot process is finished and the EEROM is returned to its natural addressing mode. Bit 0 is used to monitor the sync signal from the analog generator.

Clock Generation <5>

Crystal oscillator Y74 provides the master clock for the DSP and DIO modules. It oscillates at 24.576 MHz, driving three sections of U751 through C7502. One section drives the dsp processor master clock inputs, one drives the processor on the DIO board and the third clocks all remaining synchronous logic. Potentiometer R8401 and R8402 adjust the bias at the input of the buffers to obtain a 50% duty cycle at the processor clock inputs.

Interrupt Selection <5>

The processors each have only two hardware interrupt inputs. Programmable logic chip U450 is used to select between the available interrupt sources. Octal latch U360 latches interrupt selection information for both processors on the DSP board. It is strobed by /IRQW when the processor performs a write operation to the appropriate memory location. This latch may be read back by the processor when a read is performed from the same address. This readback is enabled by /IRQR. Read-modify-write instructions are used by the processors to set the latches. Any failure of the readback function may cause bad data to be written into the defective latch.

The lowest two bits of the latch select the main processor (U780) input data interrupt source (IRQA). The next two bits of the latch select the main processor (U780) output data interrupt source (IRQB). The trigger interrupt is also combined with the output data interrupt selection. The next two bits of the latch select the decimator processor (U770) input data interrupt source (IRQA). The top two bits of the latch select the decimator processor (U770) output data interrupt source (IRQB). The trigger interrupt is also combined with the output data interrupt selection.

One section of NAND gate U751 combines the main and decimator reset signals, causing selector U450 to tri-state its outputs when either is asserted low. When this occurs the interrupt inputs are driven through resistors R2702, R2501, R1701, R1602 from the MODE0 and MODE1 bits of U790. The processor latches the levels on its interrupt inputs as it exits reset and uses the two bit value to select the memory map and reset vector. This allows the host computer to control the memory mode of each processor as they exit reset.

Trigger Comparator <5>

The trigger signal is routed to one half of comparator U743. Resistor R7401 and capacitor C8305 eliminate high frequency noise from the signal, preventing false transitions at the output of U743. R7405 and R7402 introduce hysteresis to prevent oscillations at the output of U743 when operating with low frequency inputs. R7404 and R7403 offset the hysteresis when using the opposite signal edge to insure triggering at zero crossings. The trigger invert bit TRIG_INV causes U450 to invert the trigger signal before passing it to the processor interrupt input.

Sync Output Comparator <5>

The second section of U743 is used to create a sync signal when the D/A output is routed through the analog generator. Resistor R7301 and capacitor C8304 eliminate high frequency noise from the signal, preventing false transitions at the output of U743. R7302 and R6401 introduce hysteresis to prevent oscillations at the output of U743 when operating with low frequency inputs. By setting SYNC_EN high the comparator positive input will be held high and the output will be shut down. Since the output is open collector, when this occurs diode D7401 allows the processor to drive the sync output directly. This is used if the sync signal must follow the waveform envelope rather than its zero crossings. The sync signal is sent to the GEN module via P84.

Trigger Time Comparator <5>

8-bit counters U263 and U271 latch the time between a trigger event and the last sample interrupt. C2701, D3701 and R2701 form a one shot which clears the counters at each sample interval. The next input interrupt signal edge is inverted and used to latch the count in the counters. The counter outputs are enabled by /CNTRD going low, placing the count on the lowest 16 bits of the bus.

D/A Converter <6>

The digital audio signal from the main processors serial output port drives the programmable logic chip U652 and digital filter U540. Part of U652 selects between the input and output of the digital filter. When operating at standard digital audio sample rates of 32 kHz, 44.1 kHz, or 48 kHz the data is passed through the digital filter and oversampled by a factor of 8. When operating at a sample rate of 176.4 kHz or 192 kHz, the data is passed directly to the converters and does not pass through the digital filter. The master clock to run the digital filter must be a prescribed multiple of the input sample rate. The clock is applied at pin 6 of U540 and is derived from the PCLOCK signal on U742 pin 15 when the sample rate is derived from the internal crystal oscillators. The PCLOCK signal is 256 times the 44.1 kHz or 48 kHz sample rates. When operating at 32 kHz sample rates the PCLOCK signal is a 384 times clock. Pins 3 and 4 of U540 set the clock ratio for the filter. When pin 3 is high and pin 4 is low the filter will operate with a 384 times clock. When pin 3 is low and pin 4 is high the filter will operate with a 256 times clock. If the D/A signal is derived from the DIO option board the clock will always be 256 times the sample rate. This is sent down from the option board as OPTMCLK (pin 7) and is selected inside U652 when the MAIN/OPT bit (pin 13) goes low.

The digital filter has internal registers which must be programmed to set the operating mode of the chip. This is performed immediately after reset by a serial data word applied to pin 13 of the filter by BDO. This data word is clocked into the filter by /DACM. Buffered address lines BA0 and BA1 select which internal register is to be programmed.

The output of the selector is applied to D/A converters U440 and U340. They each handle one channel of data but their outputs are combined into a single channel by U341 before passing to the analog reconstruction filter.

The converter power supplies are heavily bypassed and decoupled to reduce noise pickup. Potentiometers R2304 and R4301 adjust the MSB scale factor to trim the converters for minimum distortion.

DAC Reconstruction Filter <7>

The DAC reconstruction filter is an analog lowpass filter used to smooth the D/A converter output. It is a "FDNR" (Frequency Dependent Negative Resistance) ladder filter as are the A/D antialias filters. A conventional LC ladder filter consists of series arms which are inductors and shunt arms which are capacitors. As the signal frequency increases, the series inductor impedance increases and the shunt capacitor impedance decreases. Above the corner frequency of the filter the attenuation rises rapidly, reducing out of band signals at the filter output. A FDNR ladder filter may be thought of as an LC lowpass ladder filter in which each inductor has been replaced by a resistor and each capacitor has been replaced by a FDNR element. Using this transformation, resistors in the original filter become capacitors in the transformed filter. Its impedance decreases with frequency twice as fast as a conventional capacitor. This doubly sharp shunt impedance, in combination with the fixed impedance in the series arms of the filter produces the same rolloff as the original LC filter.

The input signal is applied to the filter at C1301 and R1311. R1311 and R1307 provide a dc bias current path for U231, U230, U221, and U220. C1301 and C2207 are the source and load capacitances respectively. They are ratio matched to within 0.1% because their ratio directly determines the passband gain of the filter. R1308, R2302, R1301, and R2203 are the series elements of the ladder. R1310, U231, C2307, R2303, R1306, R1305 and C2305 comprise the first FDNR element, shunting the node between R1308 and R2303 to ground. Similarly, R2301, U230, C2306, R1304, C2210, R1303, R1302 and C2301 form the second FDNR element shunting the next node of the ladder. C2303 and C2304 parallel C2301 in the de-energized state of relay K220, reducing its resonant frequency for use in the 20 kHz lowpass circuit. R1207, U221, C2206, R1210, R1209, R1208, C2208 comprise the third and final FDNR. R2202 and R1206 are the main gain setting resistors for buffer U220, providing a gain of 2 to compensate for the loss in the ladder network. R1203 and C2203 provide mid-band flatness compensation.

Relay K220 is activated in when the 192 kHz or 176.4 kHz sample rates are selected. This sets the filter to an elliptic lowpass response with a corner frequency of 80 kHz. When the relay is de-energized the filter is changed to a 20 kHz lowpass for use with the 48 kHz, 44.1 kHz and 32 kHz sample rates. U220A, R2202, C2204, C2205 and R1205 provide sinX/X compensation for the high sample rates. Clamp diodes D2103 and D2104 prevent damage to the CMOS input and trigger multiplexers. The front panel DAC output bnc is driven with this signal through R1201. The signal to the analog generator module is highpass filtered by U220B, C2201, C2202 and R2201 at approximately 5 Hz. Ground potential differences between the GEN and DSP modules are compensated by the differential amplifier action of U220b R1204, R2107, R2106 and R2108. When DAEN is low relay K120 is de-energized and mutes the signal to the GEN module, thus preventing crosstalk in the analog generator modes.

Analog Signal Switching <8>

The analog input signal for each input channel is selected from one of seven sources. All analog signals entering the DSP-2 module are handled differentially to reduce the effect of ground loops. The signals from the three MONITOR OUTPUTS of the LVF module (CHANNEL A, CHANNEL B and READING) plus the analog MONITOR OUTPUT from the GEN module are routed though shielded cables from the appropriate boards to the DSP-2 board. Dc-coupled fixed range inputs are provided from two bnc connectors (DSP INPUT A and DSP INPUT B) located on the front lower left panel in SYS-2xx configurations and on the lower left back panel in SYS-3xx configurations. A seventh input signal is derived from the D/A converter output which is made available for calibration purposes only. The eighth input of the multiplexers is connected to ground to allow auto-zeroing of input offsets.

The dc coupled inputs are buffered by dual op-amp U210. Resistors R1102 and R2101 limit input current during overload conditions. The op-amp outputs are clamped by diodes D2101, D2102, D1101 and D1102 to prevent damage to the multiplexers if the op-amp outputs attempt to exceed 6 Volts.

The differential 1-of-8 input multiplexer for channel A is created with dual one-of-four CMOS switches U611 and U510. Each CMOS switch is used to select among one of four inputs by the logic levels on pin 9 and pin 10. If none of the four input signals is required the switch output is tri-stated by a high logic level on pin 6. The differential multiplexer outputs are buffered by op-amps U711, U612A and U410A. The differential signals are converted to ground referenced signals compatible with the anti-alias filters by U712A and U411A. The channel B hardware is identical.

Multiplexer U610 selects between the eight available hardware trigger signals. The selected signal is routed to the trigger comparator U743 on schematic <5> through buffer U640. The sync signal from the analog generator arrives via P84 and appears as a status bit as well as a trigger source. To match the threshold of the trigger comparator, the generator sync signal is attenuated by resistors R2502 and R5103 and centered around ground by R5102.

Antialias Filters <9>

The antialiasing filters are analog lowpass filters used to eliminate signals above the Nyquist rate from the A/D converter input. It is a "FDNR" (Frequency Dependent Negative Resistance) ladder filter as is the D/A reconstruction filter. A conventional LC ladder filter consists of series arms which are inductors and shunt arms which are capacitors. As the signal frequency increases, the series inductor impedance increases and the shunt capacitor impedance decreases. Above the corner frequency of the filter the attenuation rises rapidly, reducing out of band signals at the filter output. A FDNR ladder filter may be thought of as an LC lowpass ladder filter in which each inductor has been replaced by a resistor and each capacitor has been replaced by a FDNR element. Using this transformation, resistors in the original filter become capacitors in the transformed filter. Its impedance decreases with frequency twice as fast as a conventional capacitor. This doubly sharp shunt impedance, in combination with the fixed impedance in the series arms of the filter produces the same rolloff as the original LC filter.

Since the two filters are nominally identical, only one will be described here. The input signal is applied to the filter at C7103 and R8103. R8103 and R8101 provide a dc bias current path for U712, U720, U721, and U731. C7103 and C8302 are the source and load capacitances respectively. They are ratio matched to within 0.1% because their ratio directly determines the passband gain of the filter. R8102, R8202, R8211, and R8304 are the series elements of the ladder. R8104, U712B, C7204, U720B, R8109, R8201, R8110 and C7205 comprise the first FDNR element, shunting the node between R8102 and R8202 to ground. Similarly, R8203, U720A, C7207, U721A, R8204, C7208, R8206, R8205 and C7206 form the second FDNR element shunting the next node of the ladder. R8210, U721B, C7301, R8209, R8212, R8208, U731A, C7302, R8207 comprise the third and final FDNR. R8301 and R8302 are the main gain setting resistors for buffer U731B, providing a gain of 2 to compensate for the loss in the ladder network. R8303 and C8304 provide mid-band flatness compensation. C7303 and R8111 provide a dc signal path to exclude dc offsets from the filter.

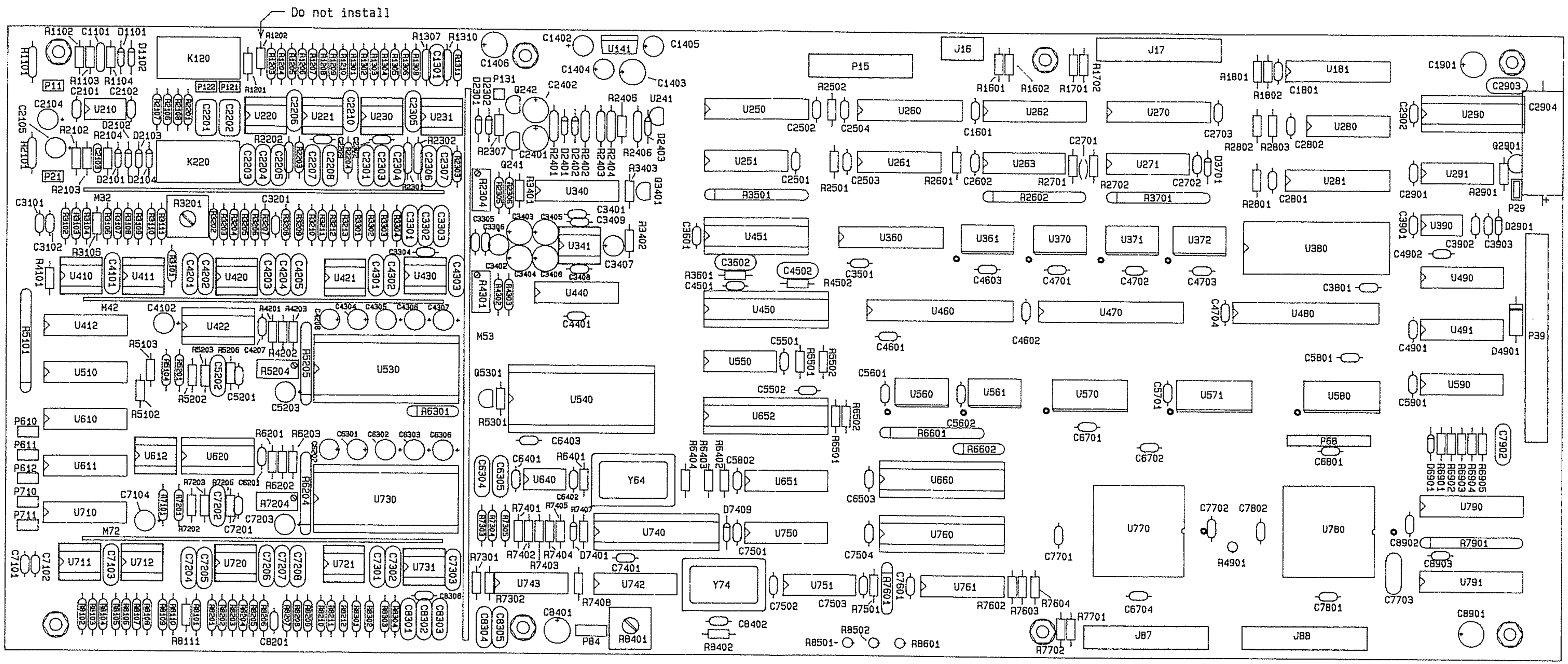
A/D Converters <10>

Analog signals are converted to digital signals for later processing by two 16-bit A/D converters and their associated sample-and-hold amplifiers. There are two nominally identical channels of A/D conversion. Only channel A will be described. The input signals from the antialiasing filters are applied to sample-and-hold amplifier U620. It operates in an inverting configuration with gain set by R7201 and R7101. The R7203-C7202 network peaks the response of the sample and hold U620, reducing the error signal during hold mode with fast slewing signals. Narrowband dither is added from U640 into the summing junction through R7202 to reduce quantization distortion. The sample and hold mode is controlled by the conversion complete signal out of the A/D converter.

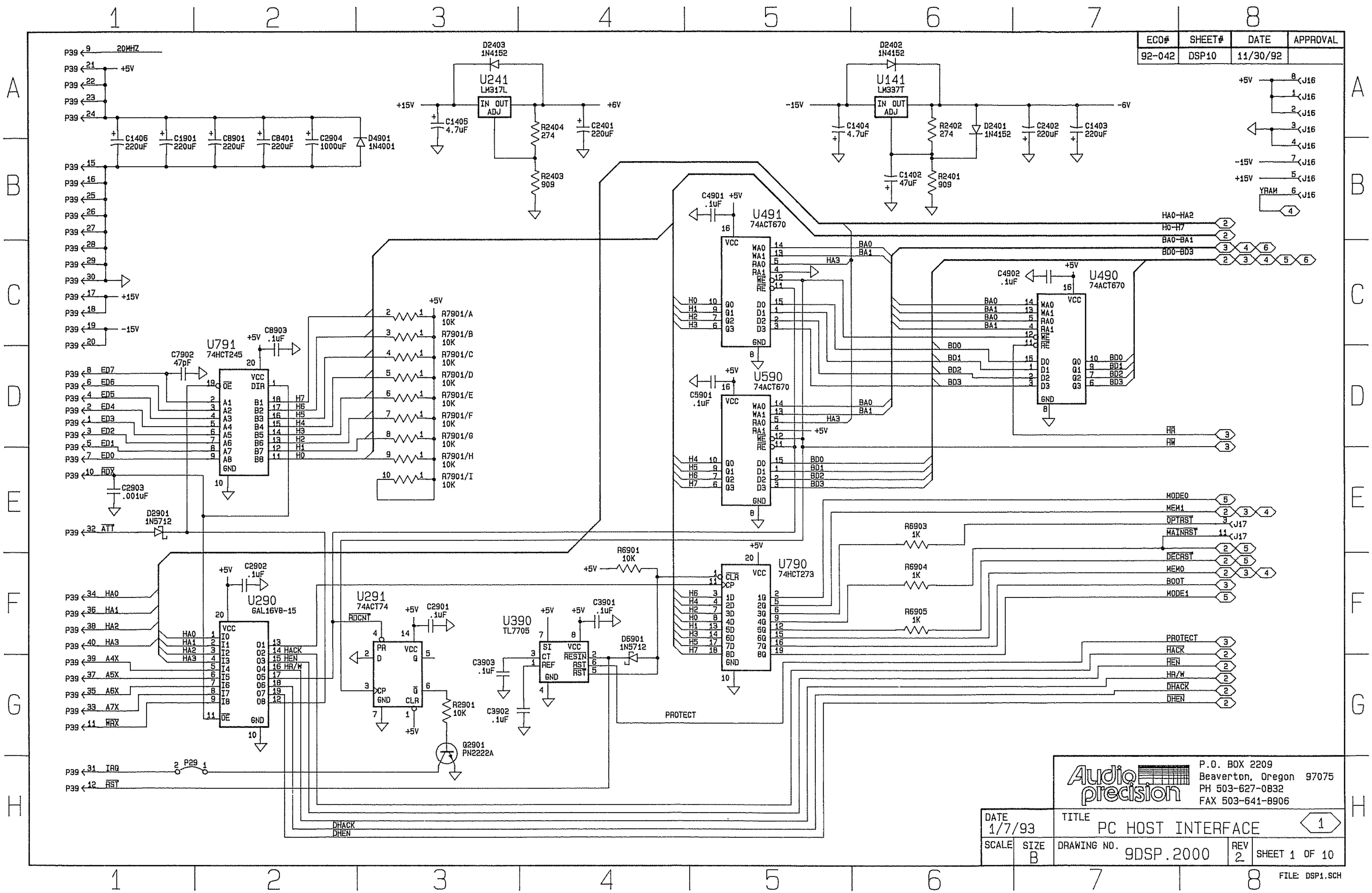
The output of the sample and hold drives the analog input of the A/D converter. The full scale signal at this point is approximately ±3 Volts peak. The conversion clock applied to pin 16 is a divide-by-6 version of the master clock. When operating at the 192 kHz sample rate this is 4.096 MHz, at 176.4 kHz this is 3.7627 MHz. The conversion clock is stopped momentarily by U741 during the start conversion pulse to insure proper operation of the converter. The data is clocked out of the converter by a higher frequency clock applied to pin 21. This is a divide-by-4 signal from the master clock. Data output from the converter on pin 13 is routed through U741 to the serial input of the decimator dsp. Part of U741 acts as a dual input data selector, switching between data from the two A/D converters.

The converter MSB is adjusted by potentiometer R7204. The converter is heavily decoupled from the power supplies by sip network R6204 and capacitors C6306, C7203, C6302, and C6303 to reduce noise pickup. Resistor network R6301 shuts down the internal conversion clock. Capacitors C6301 and C6202 filter the internal reference voltage circuits.

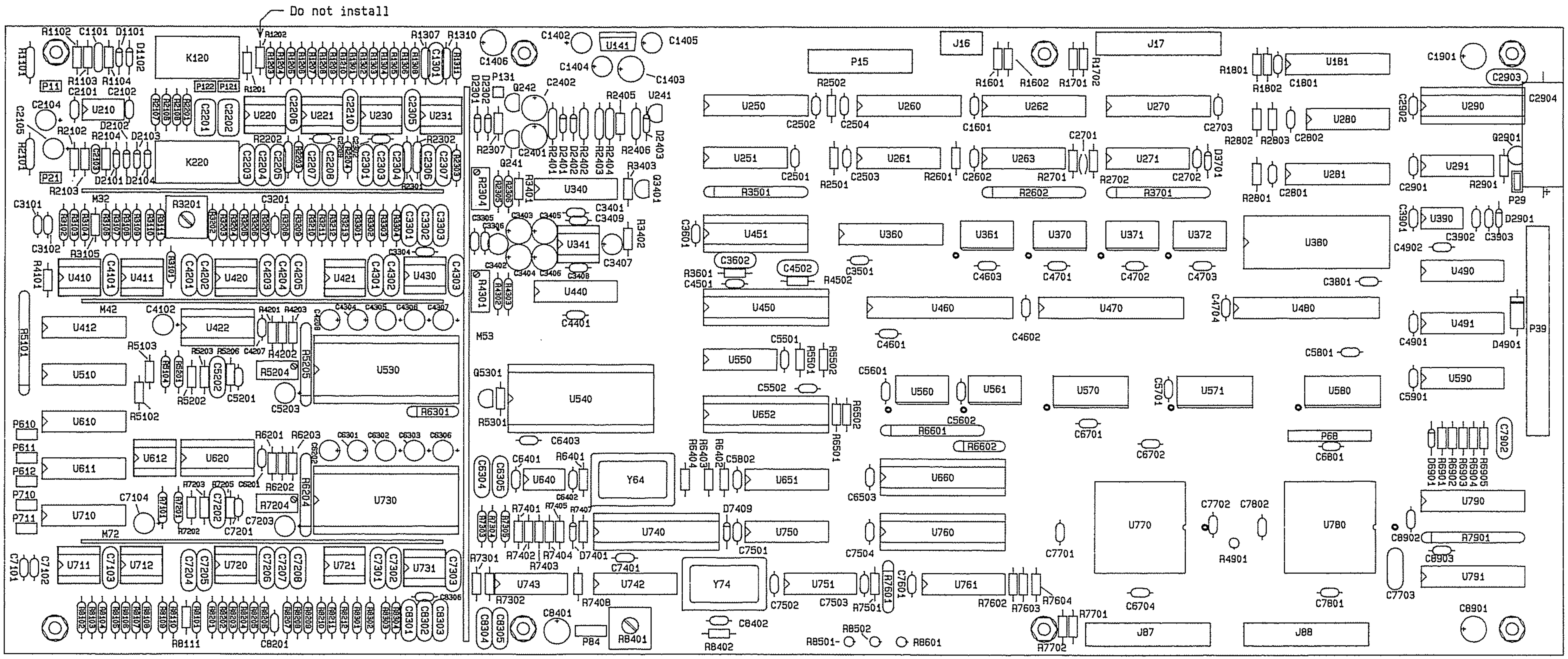
8-bit counter U742 and programmable logic chip U741 generate the A/D converter clock signals. Crystal oscillator Y64 supplies a 22.5792 MHz clock to the pal for use in generating 44.1 kHz and 176.4 kHz sample rate signals. All other sample rates are derived from the 24.576 MHz clock. The SAMPLE_F line from U281 routes the 24.576 MHz clock to U741 pin 22 when high and the 22.5792 MHz clock when low. Counter U742 derives binary sub-multiples of the selected clock which are combined in U741 to obtain the gated clocks required by the A/D converters and by the dsp's serial input port.



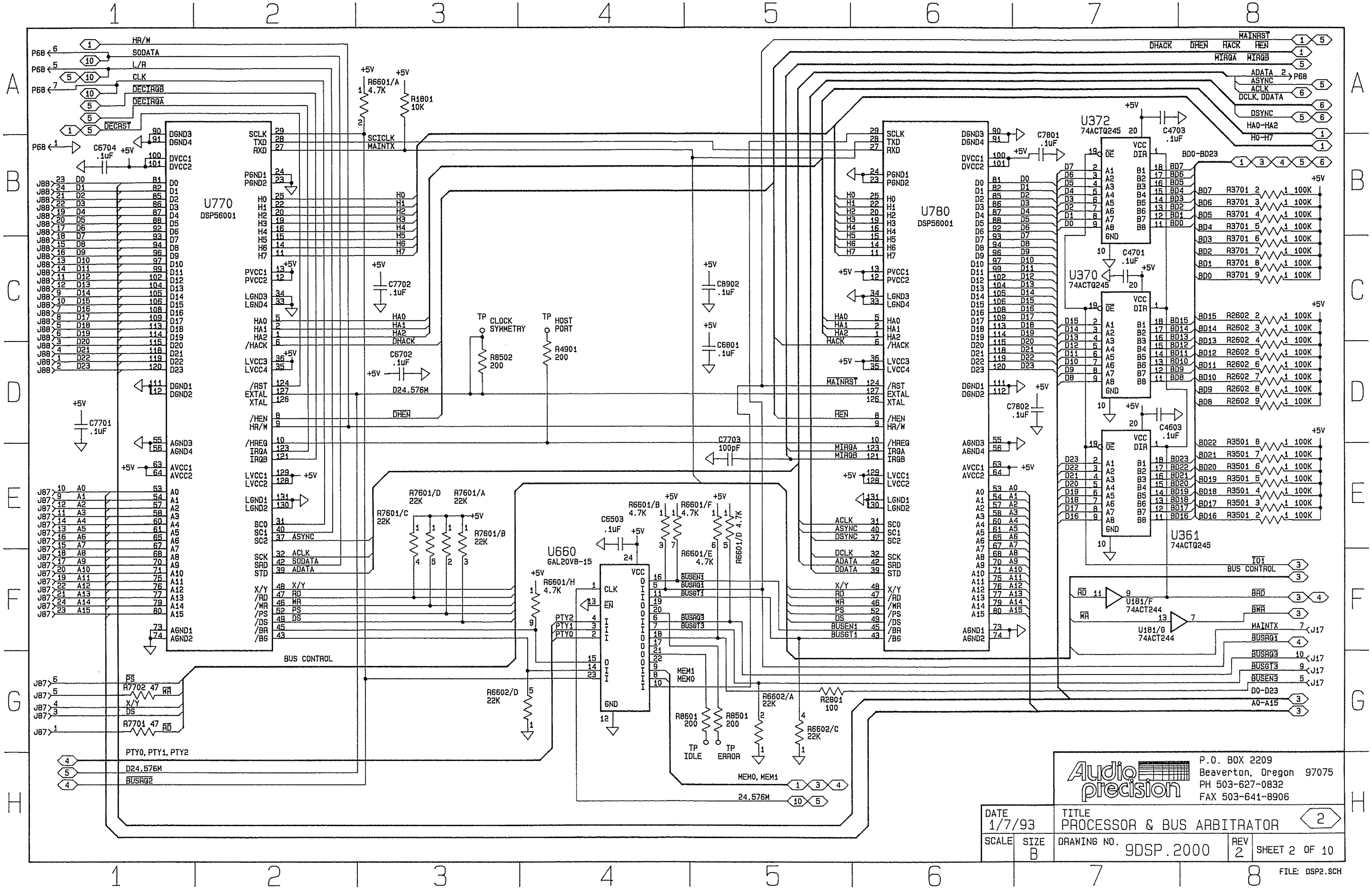
DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)



ECO#
SHEET#
DATE
APPROVAL
92-042
DSP10
11/30/92
U241
LM317L
U141
LM337T
D2403
1N4152
D2402
1N4152
+15V
+6V
-15V
-6V
U491
74ACT670
U590
74ACT670
U490
74ACT670
U791
74HCT245
U290
GAL16V8-15
U291
74ACT74
U390
TL7705
U790
74HCT273
Q2901
PN2222A
HA0-HA2
H0-H7
BA0-BA1
BD0-BD3
MODE0
MEM1
OPTRST
MAINRST
DECRST
MEMO
BOOT
MODE1
PROTECT
HACK
HEN
HR/W
DHACK
DHEN
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
1/7/93
TITLE
PC HOST INTERFACE
SCALE
SIZE
B
DRAWING NO.
9DSP.2000
REV
2
SHEET 1 OF 10
FILE: DSP1.SCH



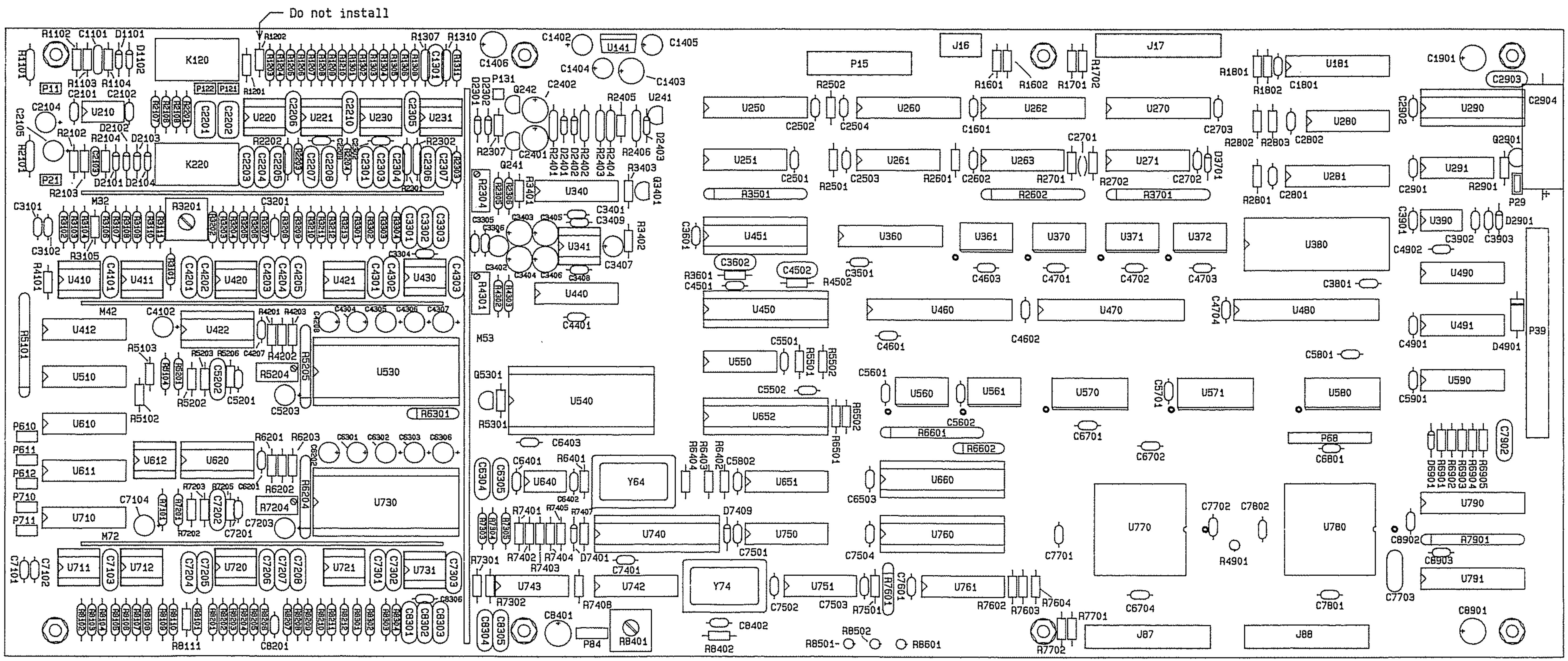
DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)



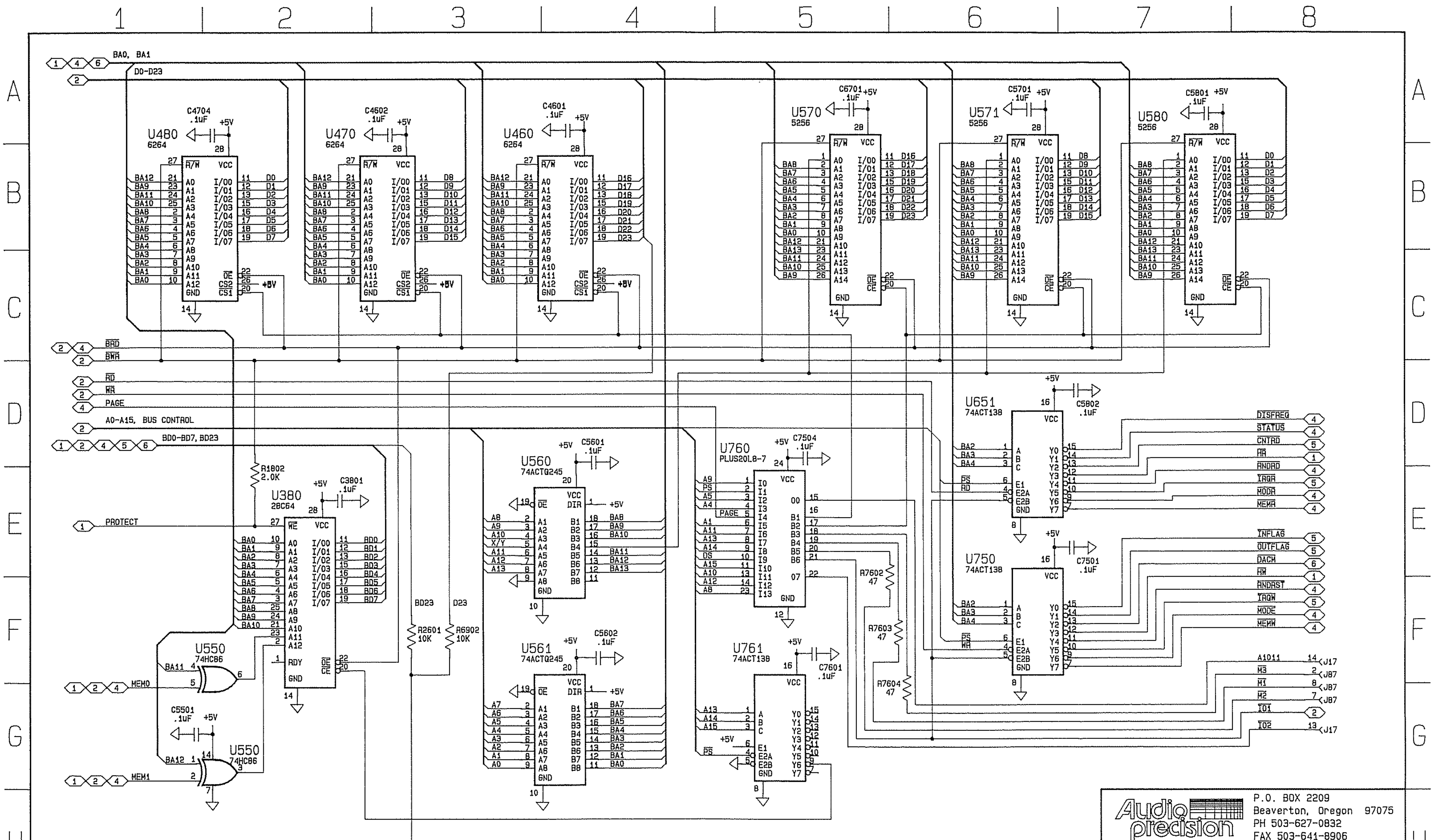
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE		
1/7/93	PROCESSOR & BUS ARBITRATOR		2
SCALE	SIZE B	DRAWING NO. 9DSP.2000	REV 2 SHEET 2 OF 10

FILE: DSP2.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)



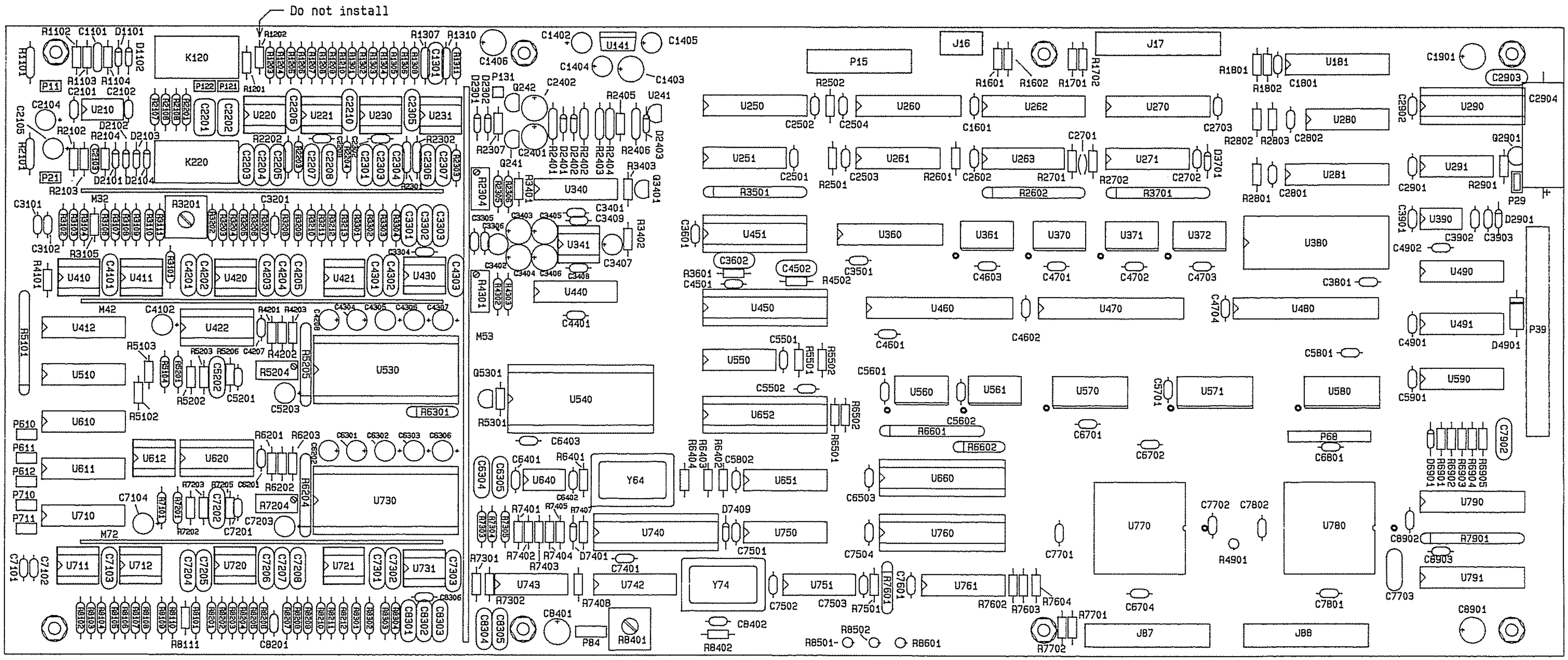
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 1/9/93

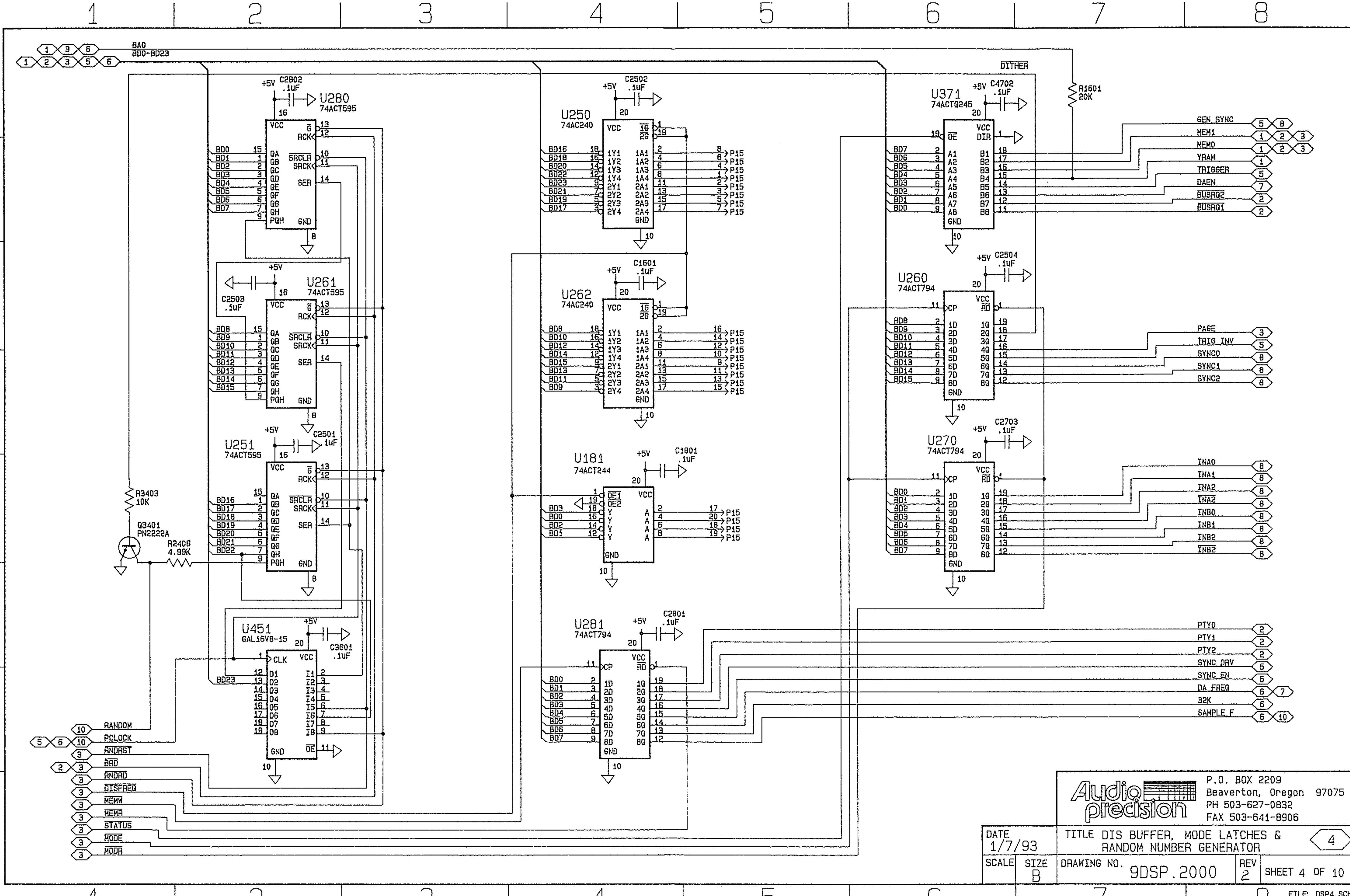
TITLE MEMORY & ADDRESS DECODE 3

SCALE | SIZE B | DRAWING NO. 9DSP.2000 | REV 2 | SHEET 3 OF 10

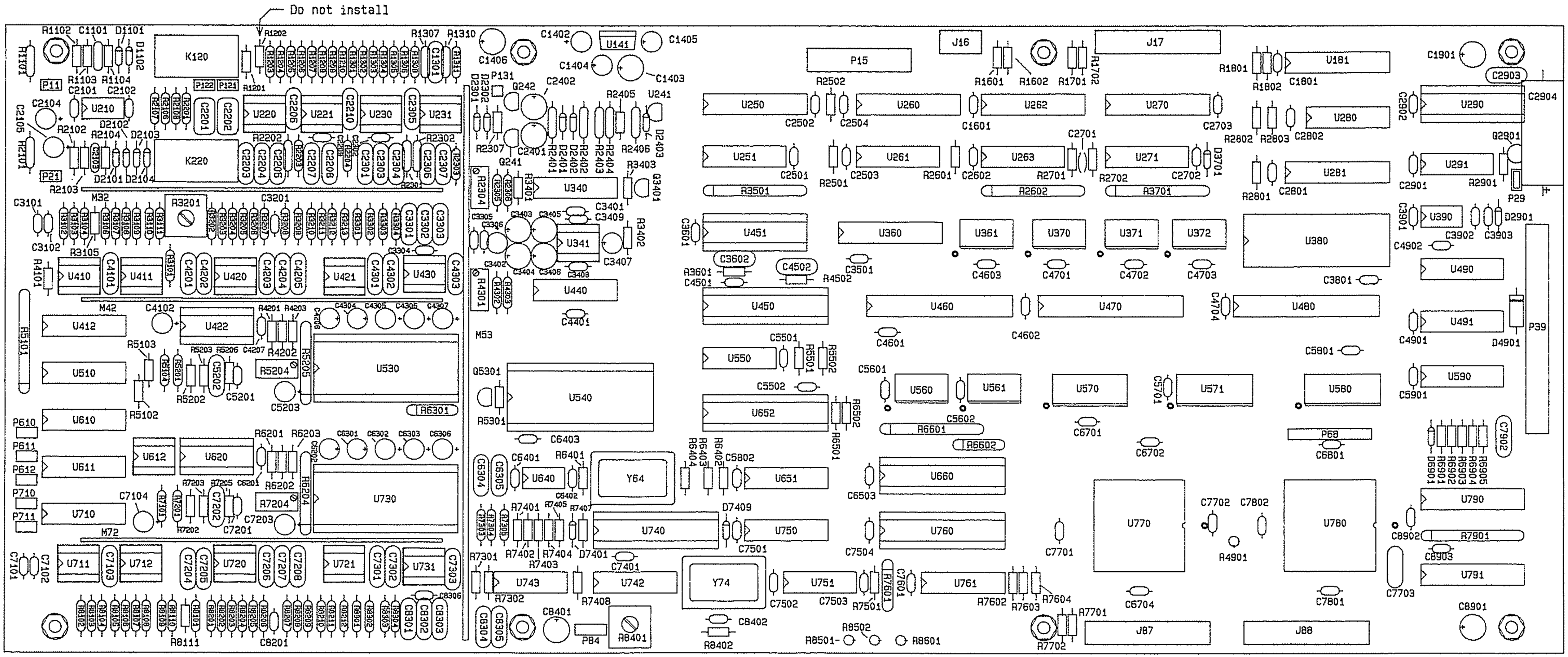
FILE: DSP3.SCH



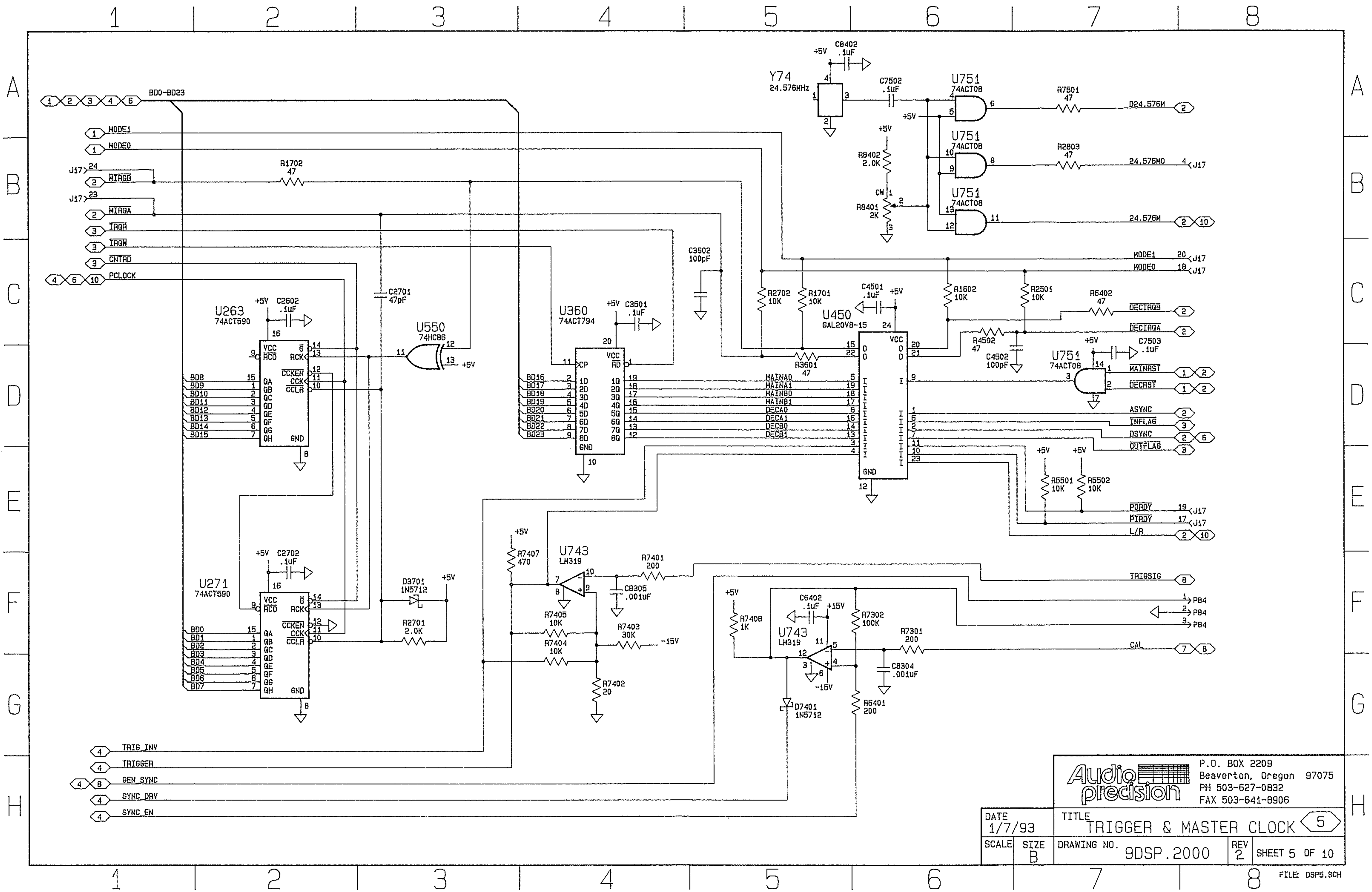
DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)

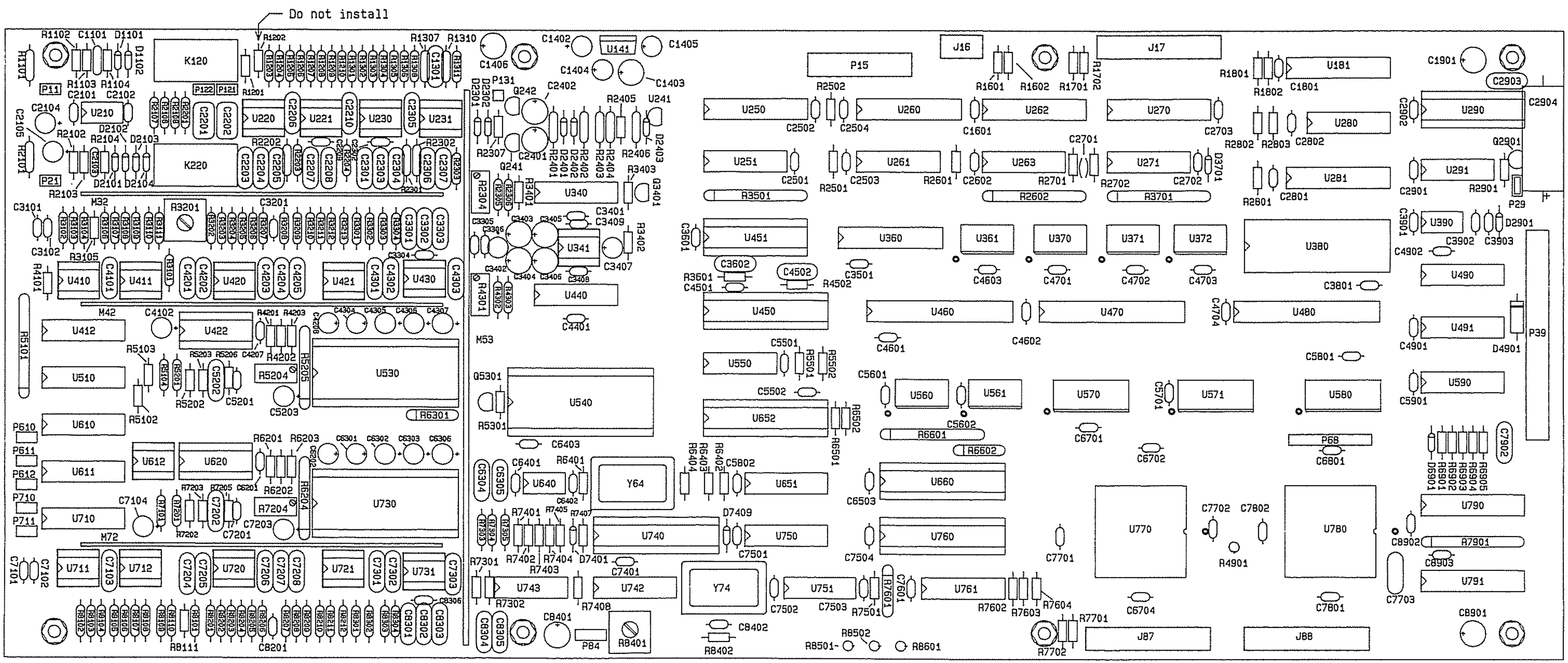


U280 74ACT595
U261 74ACT595
U251 74ACT595
U451 GAL16V8-15
U250 74AC240
U262 74AC240
U181 74ACT244
U281 74ACT794
U371 74ACTQ245
U260 74ACT794
U270 74ACT794
BA0
BD0-BD23
DITHER
R1601 20K
R3403 10K
Q3401 PN2222A
R2406 4.99K
GEN_SYNC
MEM1
MEM0
YRAM
TRIGGER
DAEN
BUSRQ2
BUSRQ1
PAGE
TRIG_INV
SYNC0
SYNC1
SYNC2
INA0
INA1
INA2
INA2
INB0
INB1
INB2
INB2
PTY0
PTY1
PTY2
SYNC_DRV
SYNC_EN
DA_FREQ
32K
SAMPLE_F
RANDOM
PCLOCK
RNDRST
BRD
RNDRD
DISFREQ
MEMW
MEMR
STATUS
MODE
MODR
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 1/7/93
TITLE DIS BUFFER, MODE LATCHES & RANDOM NUMBER GENERATOR
4
SCALE
SIZE B
DRAWING NO. 9DSP.2000
REV 2
SHEET 4 OF 10
FILE: DSP4.SCH

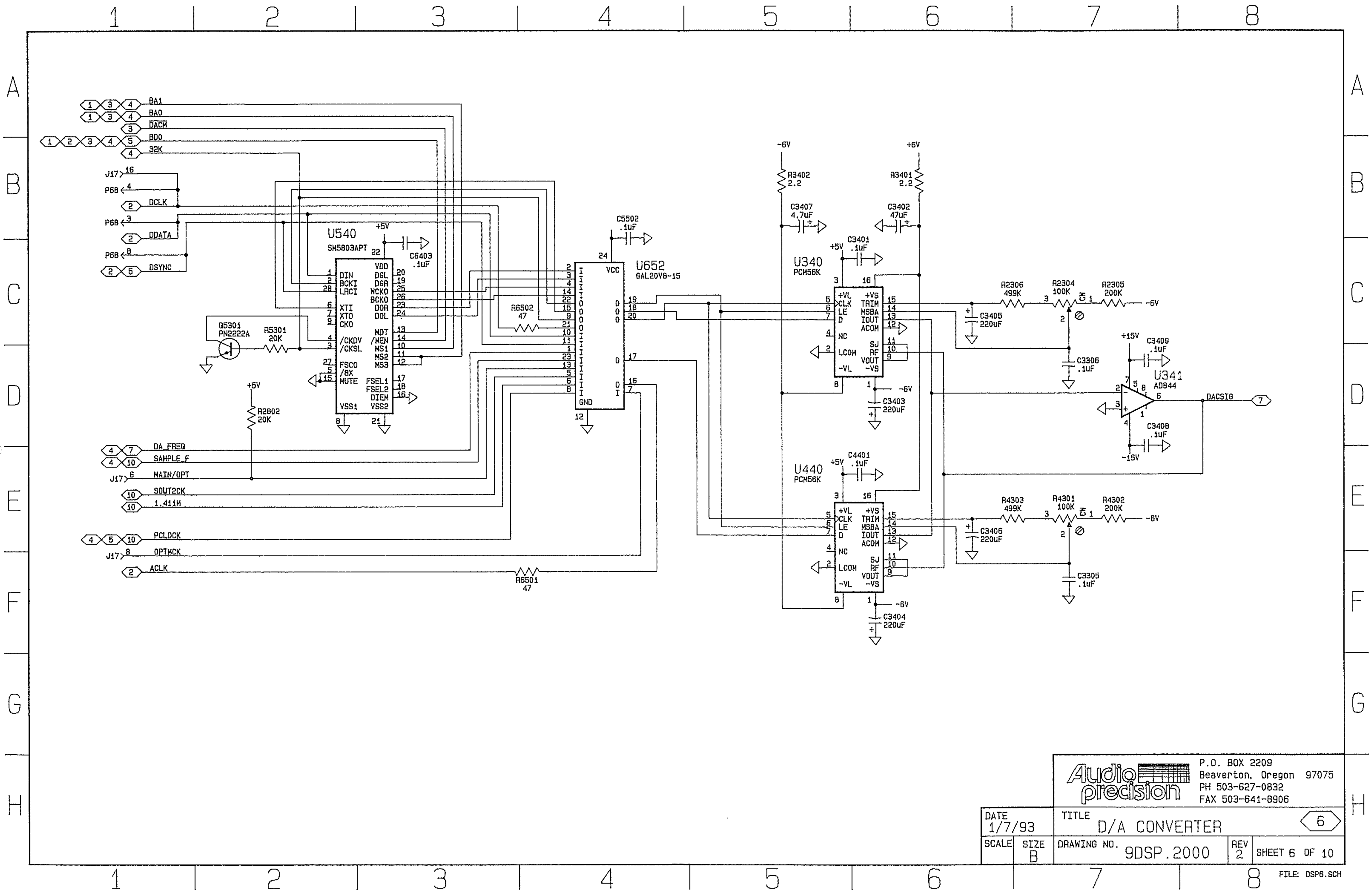


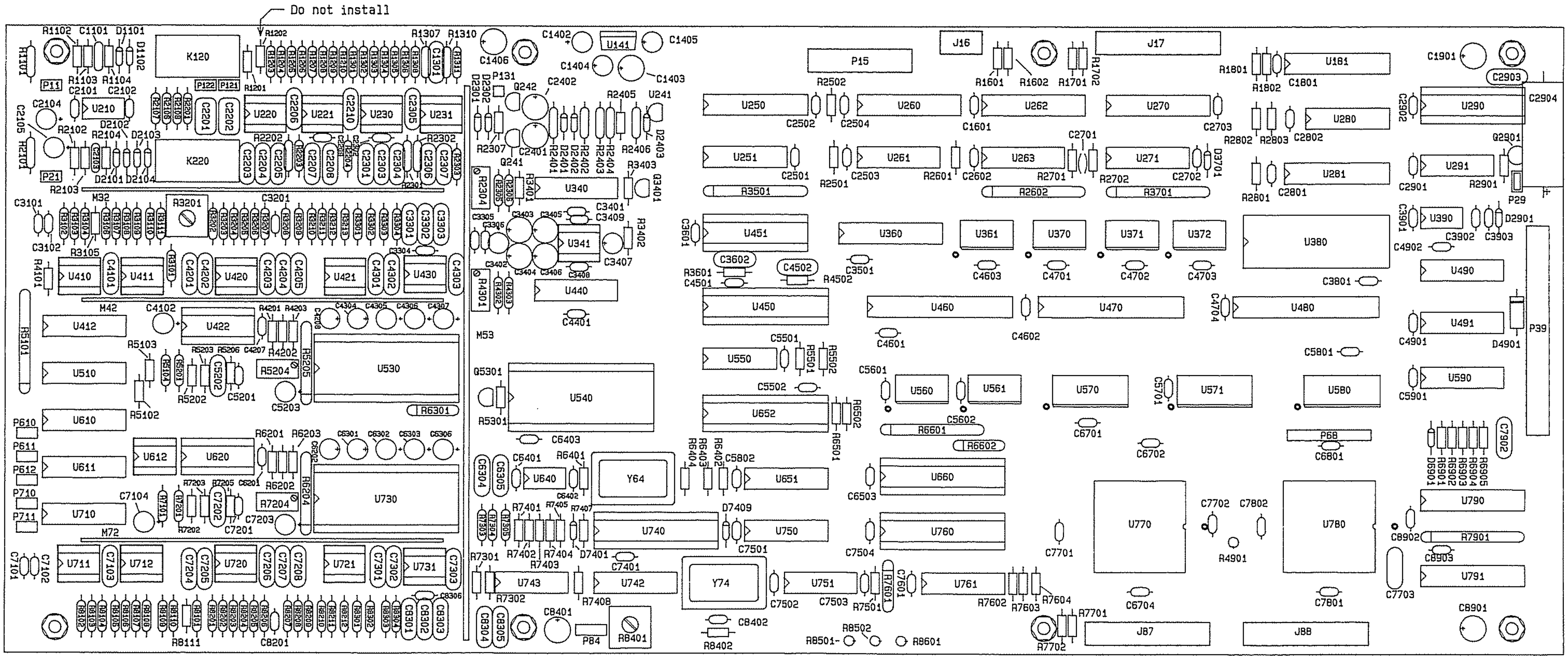
DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)


BD0-BD23
MODE1
MODE0
MIRQB
MIRQA
IRQR
IRQW
CNTRD
PCLOCK
U263
74ACT590
U271
74ACT590
U550
74HC86
U360
74ACT794
U450
GAL20V8-15
Y74
24.576MHz
U751
74ACT08
U743
LM319
D24.576M
24.576M0
24.576M
DECIRQB
DECIRQA
MAINRST
DECRST
ASYNC
INFLAG
DSYNC
OUTFLAG
PORDY
PIRDY
L/R
TRIGSIG
CAL
TRIG_INV
TRIGGER
GEN_SYNC
SYNC_DRV
SYNC_EN
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 1/7/93
TITLE TRIGGER & MASTER CLOCK
SCALE
SIZE B
DRAWING NO. 9DSP.2000
REV 2
SHEET 5 OF 10
FILE: DSP5.SCH

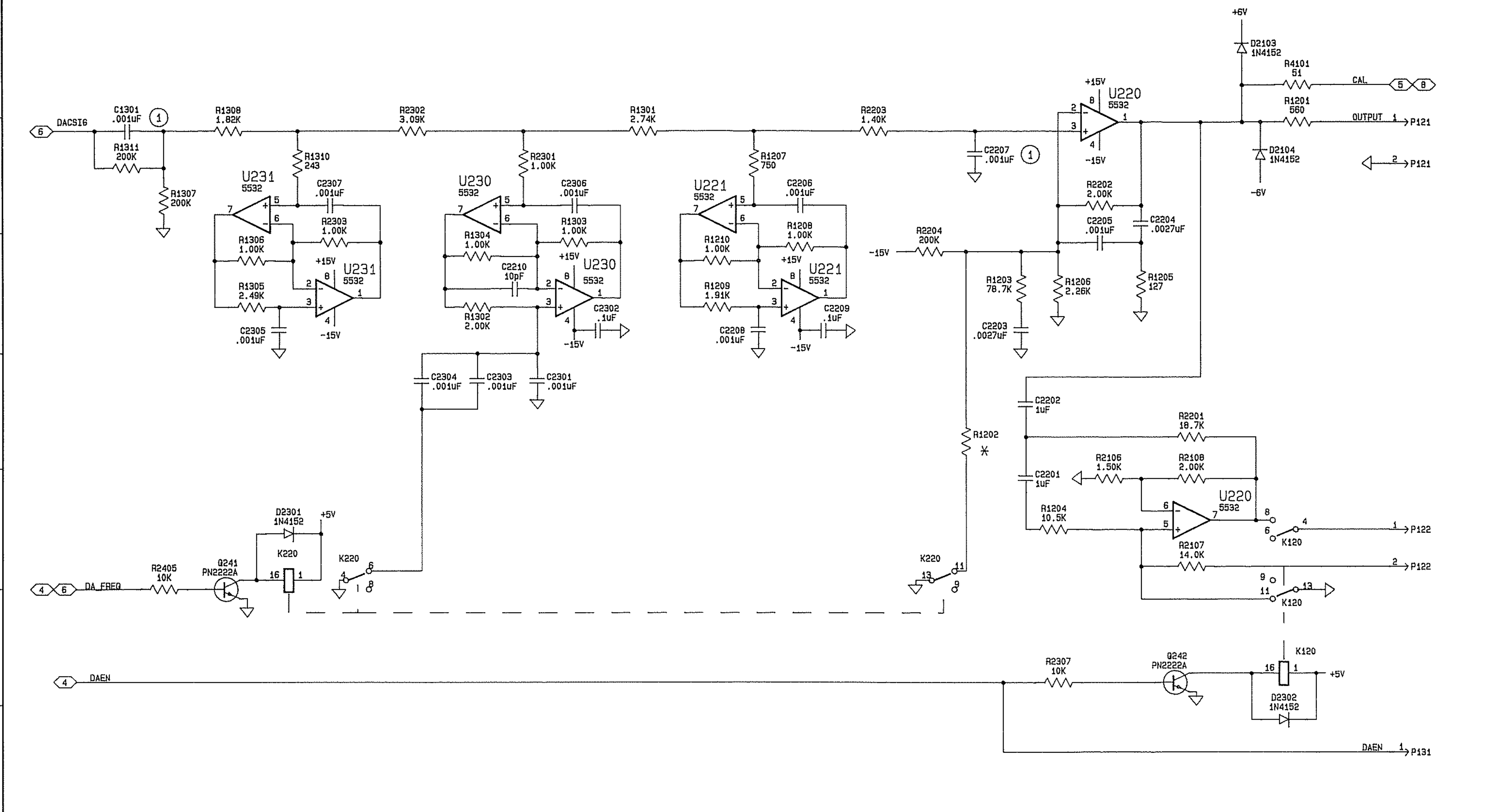


DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)


BA1
BA0
DACM
BD0
32K
J17
P6B
DCLK
DDATA
DSYNC
U540
SM5803APT
+5V
C6403
.1uF
DIN
BCKI
LRCI
XTI
XTO
CKO
/CKDV
/CKSL
FSCO
/8X
MUTE
VSS1
VDD
DGL
DGR
WCKO
BCKO
DOR
DOL
MDT
/MEN
MS1
MS2
MS3
FSEL1
FSEL2
DIEM
VSS2
Q5301
PN2222A
R5301
20K
R2802
20K
R6502
47
C5502
.1uF
U652
GAL20V8-15
VCC
GND
DA_FREQ
SAMPLE_F
MAIN/OPT
SOUT2CK
1.411M
PCLOCK
OPTMCK
ACLK
R6501
47
-6V
+6V
R3402
2.2
R3401
2.2
C3407
4.7uF
C3402
47uF
C3401
.1uF
U340
PCM56K
+VL
CLK
LE
D
NC
LCOM
-VL
+VS
TRIM
MSBA
IOUT
ACOM
SJ
RF
VOUT
-VS
C3403
220uF
C3405
220uF
R2306
499K
R2304
100K
R2305
200K
C3306
.1uF
+15V
-15V
C3409
.1uF
C3408
.1uF
U341
AD844
DACSIG
U440
PCM56K
C4401
.1uF
C3404
220uF
C3406
220uF
R4303
499K
R4301
100K
R4302
200K
C3305
.1uF
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
1/7/93
TITLE
D/A CONVERTER
6
SCALE
SIZE
B
DRAWING NO.
9DSP.2000
REV
2
SHEET 6 OF 10
FILE: DSP6.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)



NOTES:

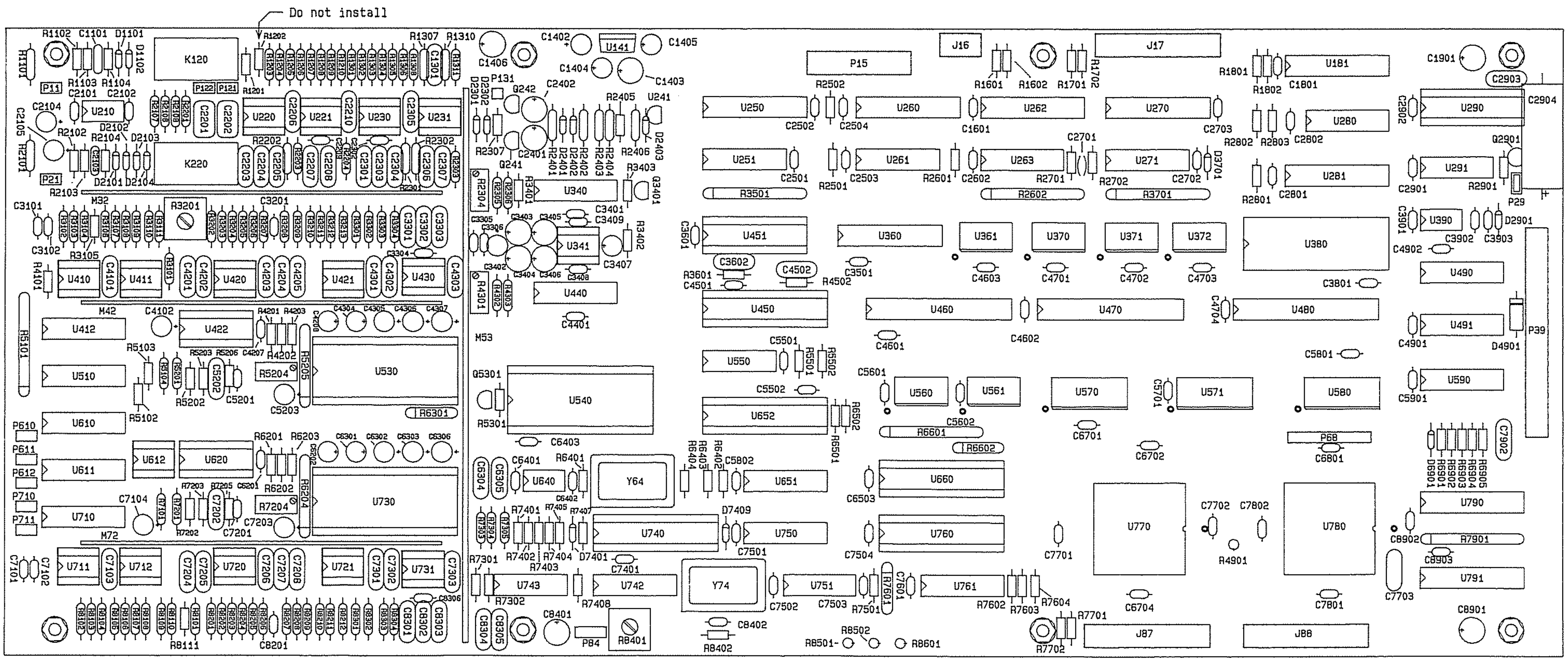
✳ NOT INSTALLED

(1) RATIO MATCHED PAIR WITHIN 1/2%.

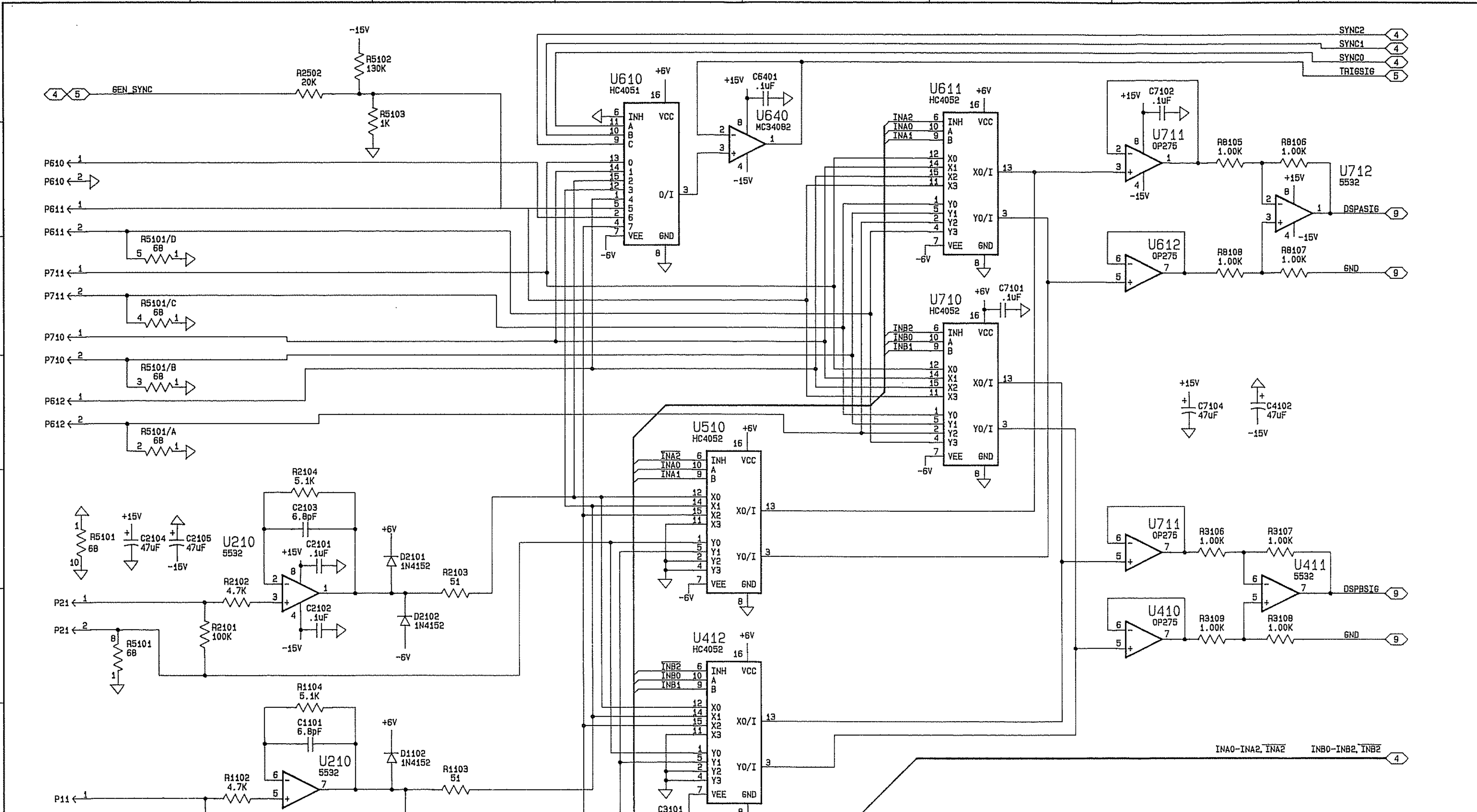
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 7/10/92	TITLE DAC RECONSTRUCTION FILTER		7
SCALE / SIZE B	DRAWING NO. 9DSP.2000	REV 2	SHEET 7 OF 10

FILE: DSP7.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)

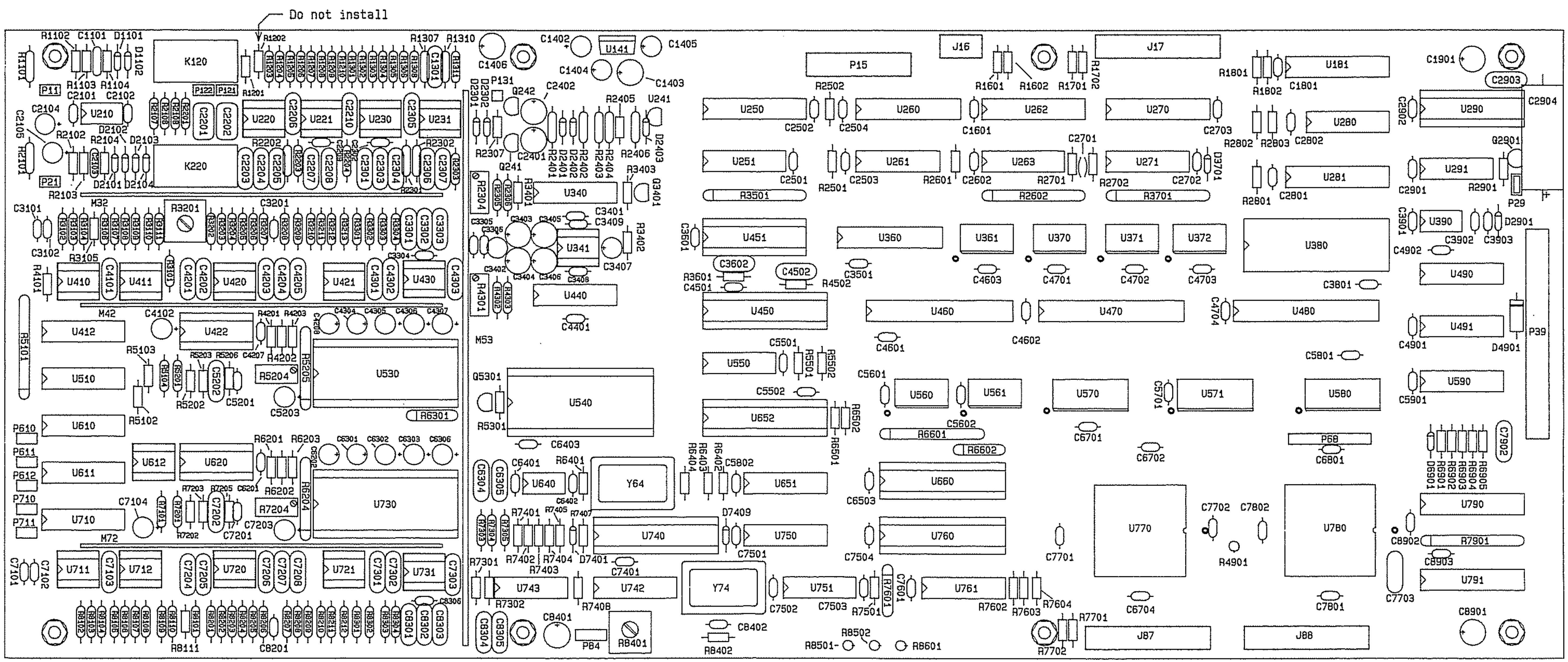


Audio precision

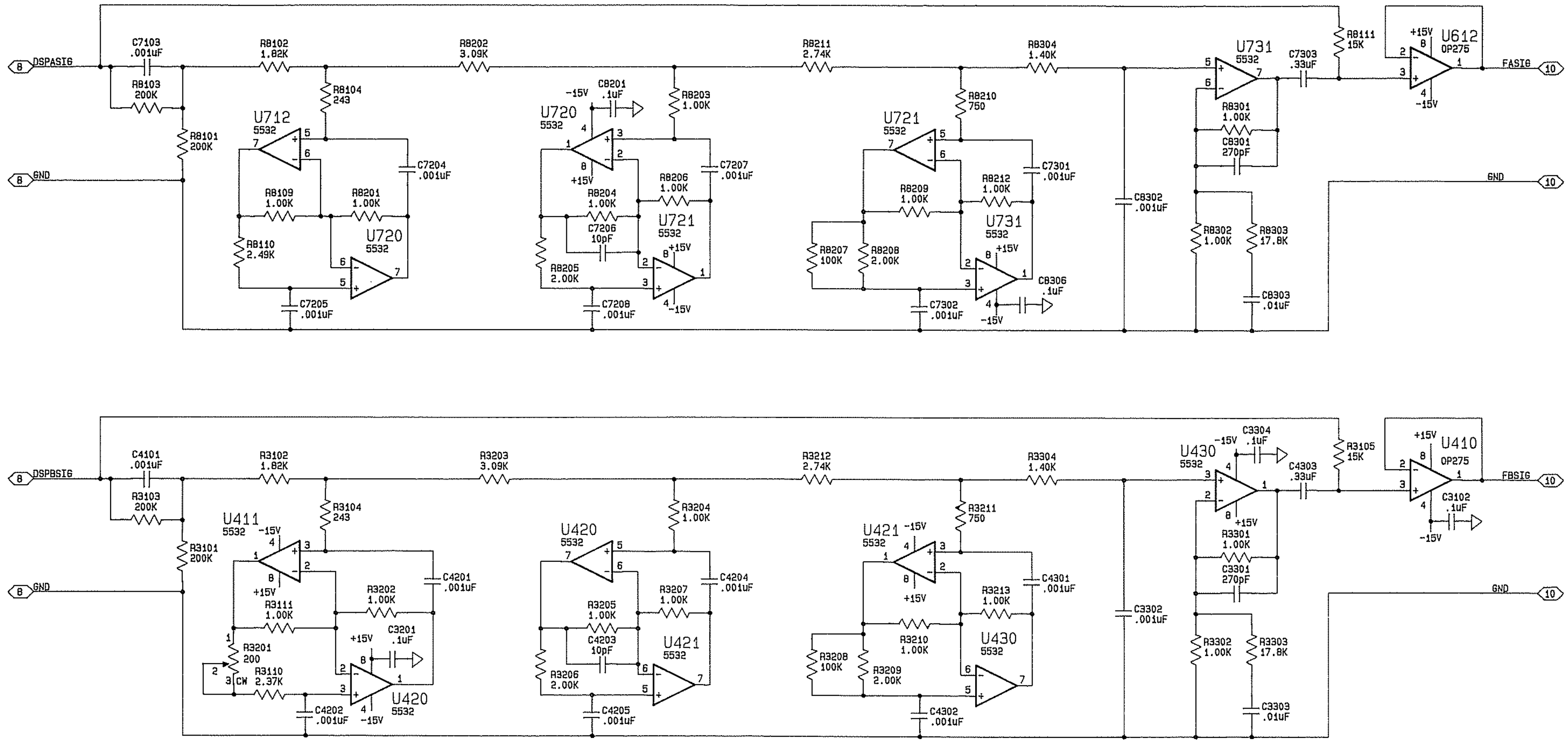
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 1/7/93	TITLE DSP ANALOG SWITCHING		8
SCALE	SIZE B	DRAWING NO. 9DSP.2000	REV 2	SHEET 8 OF 10

FILE: DSP8.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)

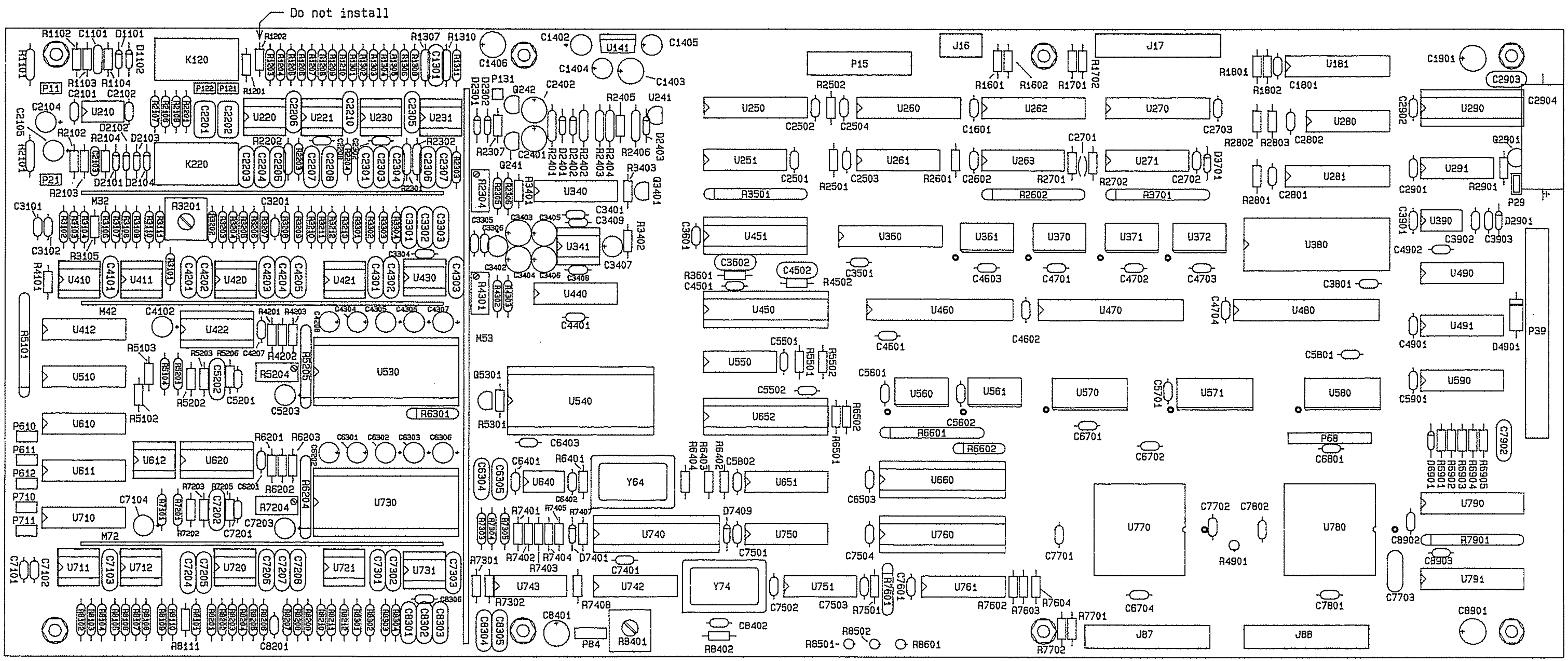


Audio precision

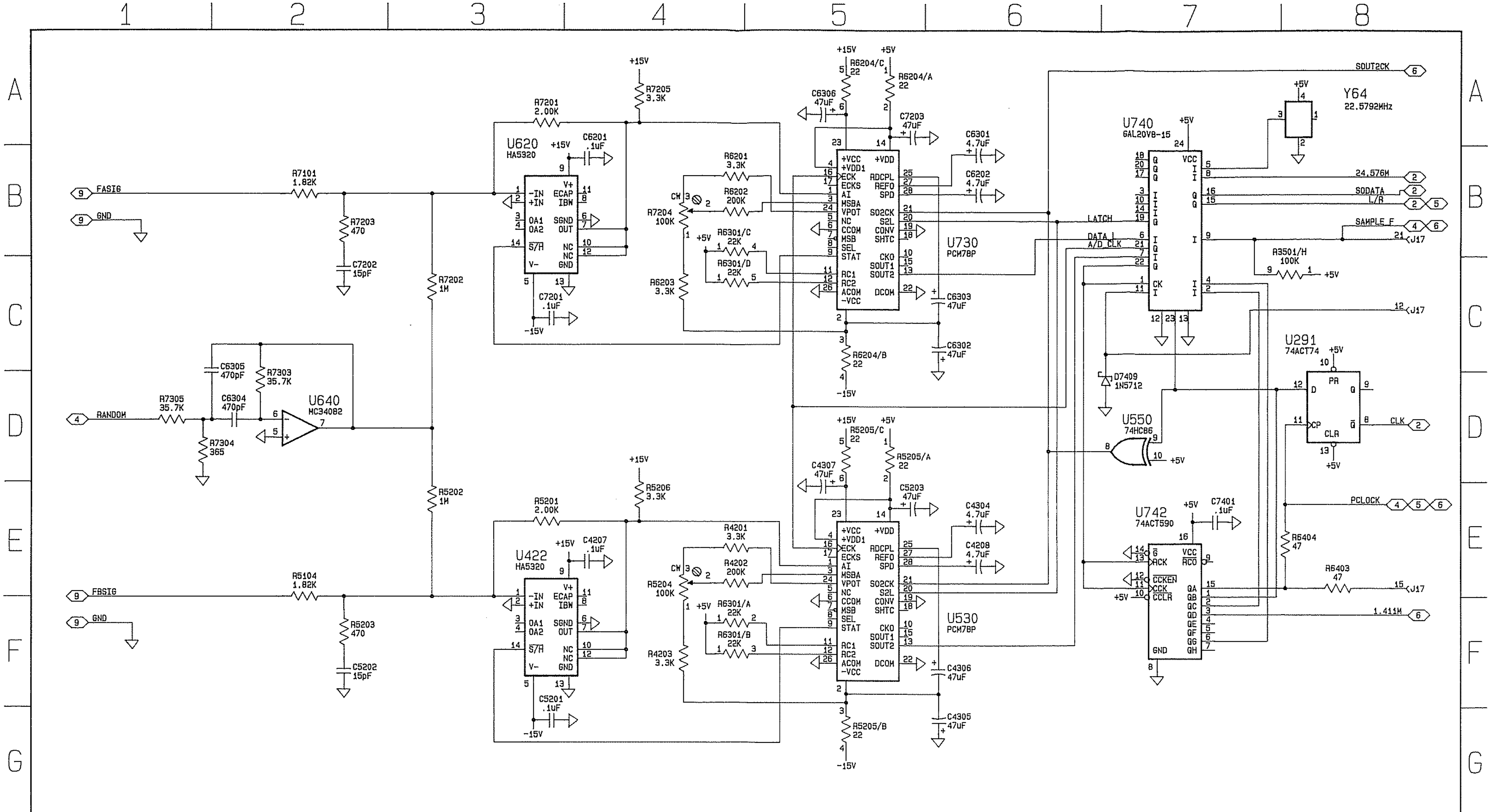
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE		
1/7/93	ANTI-ALIASING FILTER		9
SCALE / SIZE B	DRAWING NO. 9DSP.2000	REV 2	SHEET 9 OF 10

FILE: DSP9.SCH



DIGITAL SIGNAL PROCESSING MODULE 9DSP.2000 (6400.DSP2.2)



P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE			
1/7/93	A/D CONVERTERS			10
SCALE	SIZE B	DRAWING NO. 9DSP.2000	REV 2	SHEET 10 OF 10

FILE: DSP10.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1101	8G2	2172.0689	CAP CERAM 100V 20%	6.8pF
C1301	7B1	2276.0102	CAP MICA 100V 1%	.001uF
C1402	1B6	2932.0476	CAP AL-EL 25V 20%	47uF
C1403	1A7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1404	1B5	2942.0475	CAP AL-EL 35V 20%	4.7uF
C1405	1A3	2942.0475	CAP AL-EL 35V 20%	4.7uF
C1406	1A1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1601	4C4	2172.0104	CAP CERAM 100V 20%	.1uF
C1801	4E4	2172.0104	CAP CERAM 100V 20%	.1uF
C1901	1A1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2101	8E2	2172.0104	CAP CERAM 100V 20%	.1uF
C2102	8F2	2172.0104	CAP CERAM 100V 20%	.1uF
C2103	8E2	2172.0689	CAP CERAM 100V 20%	6.8pF
C2104	8E2	2932.0476	CAP AL-EL 25V 20%	47uF
C2105	8E2	2932.0476	CAP AL-EL 25V 20%	47uF
C2201	7E6	2454.0105	CAP POLYE 50V 5%	1uF
C2202	7D6	2454.0105	CAP POLYE 50V 5%	1uF
C2203	7D6	2555.0272	CAP POLYP 50V 2%	.0027uF
C2204	7B7	2555.0272	CAP POLYP 50V 2%	.0027uF
C2205	7B6	2276.0102	CAP MICA 100V 1%	.001uF
C2206	7B5	2276.0102	CAP MICA 100V 1%	.001uF
C2207	7B6	2276.0102	CAP MICA 100V 1%	.001uF
C2208	7C4	2276.0102	CAP MICA 100V 1%	.001uF
C2209	7C5	2172.0104	CAP CERAM 100V 20%	.1uF
C2210	7C3	2294.0100	CAP MICA 500V 5%	10pF
C2301	7D3	2276.0102	CAP MICA 100V 1%	.001uF
C2302	7C4	2172.0104	CAP CERAM 100V 20%	.1uF
C2303	7D3	2276.0102	CAP MICA 100V 1%	.001uF
C2304	7D3	2276.0102	CAP MICA 100V 1%	.001uF
C2305	7C2	2276.0102	CAP MICA 100V 1%	.001uF
C2306	7C4	2276.0102	CAP MICA 100V 1%	.001uF
C2307	7B2	2276.0102	CAP MICA 100V 1%	.001uF
C2401	1A4	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2402	1A7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2501	4D2	2172.0104	CAP CERAM 100V 20%	.1uF
C2502	4A4	2172.0104	CAP CERAM 100V 20%	.1uF
C2503	4C2	2172.0104	CAP CERAM 100V 20%	.1uF
C2504	4C6	2172.0104	CAP CERAM 100V 20%	.1uF
C2602	5C2	2172.0104	CAP CERAM 100V 20%	.1uF
C2701	5C3	2172.0470	CAP CERAM 100V 20%	47pF
C2702	5F2	2172.0104	CAP CERAM 100V 20%	.1uF
C2703	4D6	2172.0104	CAP CERAM 100V 20%	.1uF
C2801	4F4	2172.0104	CAP CERAM 100V 20%	.1uF
C2802	4A2	2172.0104	CAP CERAM 100V 20%	.1uF
C2901	1F3	2172.0104	CAP CERAM 100V 20%	.1uF
C2902	1F2	2172.0104	CAP CERAM 100V 20%	.1uF
C2903	1E1	2276.0102	CAP MICA 100V 1%	.001uF
C2904	1A2	2911.0108	CAP AL-EL 10V +80/-20%	1000uF
C3101	8H4	2172.0104	CAP CERAM 100V 20%	.1uF
C3102	9E8	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	9F3	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	9E7	2296.0271	CAP MICA 500V 1%	270pF

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION		
C3302	9F6	2276.0102	CAP MICA 100V 1%		.001uF
C3303	9F7	2454.0103	CAP POLYE 50V 5%		.01uF
C3304	9D7	2172.0104	CAP CERAM 100V 20%		.1uF
C3305	6F7	2172.0104	CAP CERAM 100V 20%		.1uF
C3306	6D7	2172.0104	CAP CERAM 100V 20%		.1uF
C3401	6C6	2172.0104	CAP CERAM 100V 20%		.1uF
C3402	6B6	2932.0476	CAP AL-EL 25V 20%		47uF
C3403	6D6	2911.0227	CAP AL-EL	10V +80/-20%	220uF
C3404	6F6	2911.0227	CAP AL-EL	10V +80/-20%	220uF
C3405	6C6	2911.0227	CAP AL-EL	10V +80/-20%	220uF
C3406	6F6	2911.0227	CAP AL-EL	10V +80/-20%	220uF
C3407	6B5	2942.0475	CAP AL-EL 35V 20%		4.7uF
C3408	6D7	2172.0104	CAP CERAM 100V 20%		.1uF
C3409	6D7	2172.0104	CAP CERAM 100V 20%		.1uF
C3501	5D4	2172.0104	CAP CERAM 100V 20%		.1uF
C3601	4G2	2172.0104	CAP CERAM 100V 20%		.1uF
C3602	5C5	2296.0101	CAP MICA 500V 1%		100pF
C3801	3E2	2172.0104	CAP CERAM 100V 20%		.1uF
C3901	1F4	2172.0104	CAP CERAM 100V 20%		.1uF
C3902	1G3	2172.0104	CAP CERAM 100V 20%		.1uF
C3903	1G3	2172.0104	CAP CERAM 100V 20%		.1uF
C4101	9E2	2276.0102	CAP MICA 100V 1%		.001uF
C4102	8D7	2932.0476	CAP AL-EL 25V 20%		47uF
C4201	9F3	2276.0102	CAP MICA 100V 1%		.001uF
C4202	9G2	2276.0102	CAP MICA 100V 1%		.001uF
C4203	9F4	2294.0100	CAP MICA 500V 5%		10pF
C4204	9F4	2276.0102	CAP MICA 100V 1%		.001uF
C4205	9F4	2276.0102	CAP MICA 100V 1%		.001uF
C4207	10E4	2172.0104	CAP CERAM 100V 20%		.1uF
C4208	10E6	2942.0475	CAP AL-EL 35V 20%		4.7uF
C4301	9F5	2276.0102	CAP MICA 100V 1%		.001uF
C4302	9F5	2276.0102	CAP MICA 100V 1%		.001uF
C4303	9E7	2454.0334	CAP POLYE 50V 5%		.33uF
C4304	10E6	2942.0475	CAP AL-EL 35V 20%		4.7uF
C4305	10G6	2932.0476	CAP AL-EL 25V 20%		47uF
C4306	10F6	2932.0476	CAP AL-EL 25V 20%		47uF
C4307	10E5	2932.0476	CAP AL-EL 25V 20%		47uF
C4401	5E5	2172.0104	CAP CERAM 100V 20%		.1uF
C4501	5C5	2172.0104	CAP CERAM 100V 20%		.1uF
C4502	5D5	2296.0101	CAP MICA 500V 1%		100pF
C4601	3A4	2172.0104	CAP CERAM 100V 20%		.1uF
C4602	3A3	2172.0104	CAP CERAM 100V 20%		.1uF
C4603	2D7	2172.0104	CAP CERAM 100V 20%		.1uF
C4701	2C7	2172.0104	CAP CERAM 100V 20%		.1uF
C4702	4A6	2172.0104	CAP CERAM 100V 20%		.1uF
C4703	2A7	2172.0104	CAP CERAM 100V 20%		.1uF
C4704	3A1	2172.0104	CAP CERAM 100V 20%		.1uF
C4901	1C5	2172.0104	CAP CERAM 100V 20%		.1uF
C4902	1C6	2172.0104	CAP CERAM 100V 20%		.1uF
C5201	10G4	2172.0104	CAP CERAM 100V 20%		.1uF
C5202	10F2	2294.0150	CAP MICA 500V 5%		15pF
C5203	10E5	2932.0476	CAP AL-EL 25V 20%		47uF

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C5501	3G1	2172.0104	CAP CERAM 100V 20%	.1uF
C5502	6C4	2172.0104	CAP CERAM 100V 20%	.1uF
C5601	3E4	2172.0104	CAP CERAM 100V 20%	.1uF
C5602	3F4	2172.0104	CAP CERAM 100V 20%	.1uF
C5701	3A6	2172.0104	CAP CERAM 100V 20%	.1uF
C5801	3A7	2172.0104	CAP CERAM 100V 20%	.1uF
C5802	3D6	2172.0104	CAP CERAM 100V 20%	.1uF
C5901	1D5	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	10B4	2172.0104	CAP CERAM 100V 20%	.1uF
C6202	10B6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6301	10B6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6302	10C6	2932.0476	CAP AL-EL 25V 20%	47uF
C6303	10C6	2932.0476	CAP AL-EL 25V 20%	47uF
C6304	10D2	2296.0471	CAP MICA 500V 1%	470pF
C6305	10D2	2296.0471	CAP MICA 500V 1%	470pF
C6306	10A5	2932.0476	CAP AL-EL 25V 20%	47uF
C6401	8A5	2172.0104	CAP CERAM 100V 20%	.1uF
C6402	5F5	2172.0104	CAP CERAM 100V 20%	.1uF
C6403	6C3	2172.0104	CAP CERAM 100V 20%	.1uF
C6503	2F4	2172.0104	CAP CERAM 100V 20%	.1uF
C6701	3A5	2172.0104	CAP CERAM 100V 20%	.1uF
C6702	2D3	2172.0104	CAP CERAM 100V 20%	.1uF
C6704	2B1	2172.0104	CAP CERAM 100V 20%	.1uF
C6801	2D5	2172.0104	CAP CERAM 100V 20%	.1uF
C7101	8C6	2172.0104	CAP CERAM 100V 20%	.1uF
C7102	8B7	2172.0104	CAP CERAM 100V 20%	.1uF
C7103	9A2	2276.0102	CAP MICA 100V 1%	.001uF
C7104	8D7	2932.0476	CAP AL-EL 25V 20%	47uF
C7201	10C3	2172.0104	CAP CERAM 100V 20%	.1uF
C7202	10C2	2294.0150	CAP MICA 500V 5%	15pF
C7203	10A5	2932.0476	CAP AL-EL 25V 20%	47uF
C7204	9C3	2276.0102	CAP MICA 100V 1%	.001uF
C7205	9C2	2276.0102	CAP MICA 100V 1%	.001uF
C7206	9C4	2294.0100	CAP MICA 500V 5%	10pF
C7207	9C4	2276.0102	CAP MICA 100V 1%	.001uF
C7208	9C4	2276.0102	CAP MICA 100V 1%	.001uF
C7301	9C6	2276.0102	CAP MICA 100V 1%	.001uF
C7302	9C6	2276.0102	CAP MICA 100V 1%	.001uF
C7303	9A7	2454.0334	CAP POLYE 50V 5%	.33uF
C7401	10E7	2172.0104	CAP CERAM 100V 20%	.1uF
C7501	3E6	2172.0104	CAP CERAM 100V 20%	.1uF
C7502	5A6	2172.0104	CAP CERAM 100V 20%	.1uF
C7503	5D7	2172.0104	CAP CERAM 100V 20%	.1uF
C7504	3D5	2172.0104	CAP CERAM 100V 20%	.1uF
C7601	3F4	2172.0104	CAP CERAM 100V 20%	.1uF
C7701	2D1	2172.0104	CAP CERAM 100V 20%	.1uF
C7702	2C3	2172.0104	CAP CERAM 100V 20%	.1uF
C7703	2E5	2296.0101	CAP MICA 500V 1%	100pF
C7801	2B7	2172.0104	CAP CERAM 100V 20%	.1uF
C7802	2D6	2172.0104	CAP CERAM 100V 20%	.1uF
C7902	1D1	2294.0470	CAP MICA 500V 5%	47pF
C8201	9B4	2172.0104	CAP CERAM 100V 20%	.1uF

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION		
C8301	9B7	2296.0271	CAP MICA 500V 1%		270pF
C8302	9C6	2276.0102	CAP MICA 100V 1%		.001uF
C8303	9C7	2454.0103	CAP POLYE 50V 5%		.01uF
C8304	5G6	2276.0102	CAP MICA 100V 1%		.001uF
C8305	5F4	2276.0102	CAP MICA 100V 1%		.001uF
C8306	9C6	2172.0104	CAP CERAM 100V 20%		.1uF
C8401	1A2	2911.0227	CAP AL-EL	10V +80/-20%	220uF
C8402	5A5	2172.0104	CAP CERAM 100V 20%		.1uF
C8901	1A2	2911.0227	CAP AL-EL	10V +80/-20%	220uF
C8902	2C5	2172.0104	CAP CERAM 100V 20%		.1uF
C8903	1D2	2172.0104	CAP CERAM 100V 20%		.1uF
D1101	8H3	3110.4152	DIODE SIGNAL		4152
D1102	8G3	3110.4152	DIODE SIGNAL		4152
D2101	8E3	3110.4152	DIODE SIGNAL		4152
D2102	8F3	3110.4152	DIODE SIGNAL		4152
D2103	7A7	3110.4152	DIODE SIGNAL		4152
D2104	7B7	3110.4152	DIODE SIGNAL		4152
D2301	7E2	3110.4152	DIODE SIGNAL		4152
D2302	7G7	3110.4152	DIODE SIGNAL		4152
D2401	1A6	3110.4152	DIODE SIGNAL		4152
D2402	1A6	3110.4152	DIODE SIGNAL		4152
D2403	1A3	3110.4152	DIODE SIGNAL		4152
D2901	1E1	3120.0000	DIODE SCHOTTKY		1SS97
D3701	5F3	3120.0000	DIODE SCHOTTKY		1SS97
D4901	1A3	3111.4001	DIODE POWER 1A 50V		4001
D6901	1G4	3120.0000	DIODE SCHOTTKY		1SS97
D7401	5G5	3120.0000	DIODE SCHOTTKY		1SS97
D7409	10D7	3120.0000	DIODE SCHOTTKY		1SS97
J16	1A8,1B8	4221.1008	JACK PC 2 X .1		8 PIN
J17	1E8,2F8,2G8,5B1, 5E8-5F8,6B1-6F1,10B8-10E8	4221.1024	JACK PC 2 X .1		24 PIN
J29		4220.1002	JACK MINI-JUMPER		2 PIN
J87	2E1-2G1,3F8	4221.1024	JACK PC 2 X .1		24 PIN
J88	2C1-2D1	4221.1024	JACK PC 2 X .1		24 PIN
K120	7E7,7F7	4530.0002.1	RELAY	PC LOW POWER STABLE DPDT	
K220	7E2,7E5	4530.0002.1	RELAY	PC LOW POWER STABLE DPDT	
P11	8G1	4221.0036	PLUG PC	.1 X.43	36 PIN
P121	7B8	4221.0036	PLUG PC	.1 X.43	36 PIN
P122	7E8	4221.0036	PLUG PC	.1 X.43	36 PIN
P131	7G8	4221.0036	PLUG PC	.1 X.43	36 PIN
P15	4B5-4E5	4221.0072	PLUG PC 2X.1 X.43		72 PIN
P21	8F1	4221.0036	PLUG PC	.1 X.43	36 PIN
P29	1H1	4221.0036	PLUG PC	.1 X.43	36 PIN
P39	1A1-1H1	4151.1740	CABLE ASSY .05	RBN 17"40 COND	
P610	8B1	4221.0036	PLUG PC	.1 X.43	36 PIN
P611	8B1	4221.0036	PLUG PC	.1 X.43	36 PIN
P612	8D1	4221.0036	PLUG PC	.1 X.43	36 PIN
P68	2A1,2A8,2B1,6B1	4221.0036	PLUG PC	.1 X.43	36 PIN
P710	8C1	4221.0036	PLUG PC	.1 X.43	36 PIN
P711	8C1	4221.0036	PLUG PC	.1 X.43	36 PIN
P84	5F8	4221.0036	PLUG PC	.1 X.43	36 PIN
Q241	7E7	3211.2222	XSTR NPN TO92		PN2222A

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
Q242	7F7	3211.2222	XSTR NPN TO92	PN2222A
Q2901	1H3	3211.2222	XSTR NPN TO92	PN2222A
Q3401	4E1	3211.2222	XSTR NPN TO92	PN2222A
Q5301	6C2	3211.2222	XSTR NPN TO92	PN2222A
R1101	8H2	1136.1003	RES 1/8W M FLM 1%	100K
R1102	8G2	1214.0472	RES 1/4W C FLM 5%	4.7K
R1103	8G3	1214.0510	RES 1/4W C FLM 5%	51
R1104	8G2	1214.0512	RES 1/4W C FLM 5%	5.1K
R1201	7A7	1214.0561	RES 1/4W C FLM 5%	560
R1202	7D7	1214.0000	JUMPER .4 X.25	00
R1203	7C6	1136.7872	RES 1/8W M FLM 1%	78.7K
R1204	7E6	1136.1052	RES 1/8W M FLM 1%	10.5K
R1205	7C7	1136.1270	RES 1/8W M FLM 1%	127
R1206	7C6	1136.2261	RES 1/8W M FLM 1%	2.26K
R1207	7B4	1136.7500	RES 1/8W M FLM 1%	750
R1208	7C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R1209	7C4	1136.1911	RES 1/8W M FLM 1%	1.91K
R1210	7C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R1301	7B4	1136.2741	RES 1/8W M FLM 1%	2.74K
R1302	7C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R1303	7C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R1304	7C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R1305	7C2	1136.2491	RES 1/8W M FLM 1%	2.49K
R1306	7C2	1139.1001	RES 1/8W M FLM .1%	1.00K
R1307	7B1	1139.2003	RES 1/8W M FLM .1%	200K
R1308	7B2	1136.1821	RES 1/8W M FLM 1%	1.82K
R1310	7C2	1136.2430	RES 1/8W M FLM 1%	243
R1311	7B1	1139.2003	RES 1/8W M FLM .1%	200K
R1601	4A7	1214.0203	RES 1/4W C FLM 5%	20K
R1602	5C6	1214.0103	RES 1/4W C FLM 5%	10K
R1701	5C5	1214.0103	RES 1/4W C FLM 5%	10K
R1702	5B2	1214.0470	RES 1/4W C FLM 5%	47
R1801	2A3	1214.0103	RES 1/4W C FLM 5%	10K
R1802	3E2	1214.0202	RES 1/4W C FLM 5%	2.0K
R2101	8F2	1136.1003	RES 1/8W M FLM 1%	100K
R2102	8F2	1214.0472	RES 1/4W C FLM 5%	4.7K
R2103	8F3	1214.0510	RES 1/4W C FLM 5%	51
R2104	8E2	1214.0512	RES 1/4W C FLM 5%	5.1K
R2106	7E6	1136.1501	RES 1/8W M FLM 1%	1.50K
R2107	7E7	1136.1402	RES 1/8W M FLM 1%	14.0K
R2108	7E7	1139.2001	RES 1/8W M FLM .1%	2.00K
R2201	7D7	1136.1872	RES 1/8W M FLM 1%	18.7K
R2202	7B6	1139.2001	RES 1/8W M FLM .1%	2.00K
R2203	7B5	1136.1401	RES 1/8W M FLM 1%	1.40K
R2204	7C5	1136.2003	RES 1/8W M FLM 1%	200K
R2301	7B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R2302	7B3	1136.3091	RES 1/8W M FLM 1%	3.09K
R2303	7C2	1139.1001	RES 1/8W M FLM .1%	1.00K
R2304	6C7	4413.0104	POT TRIM PC 10 TURN	100K
R2305	6C7	1136.2003	RES 1/8W M FLM 1%	200K
R2306	6C6	1136.4993	RES 1/8W M FLM 1%	499K
R2307	7F6	1214.0103	RES 1/4W C FLM 5%	10K

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R2401	1B6	1136.9090	RES 1/8W M FLM 1%	909
R2402	1B6	1136.2740	RES 1/8W M FLM 1%	274
R2403	1B3	1136.9090	RES 1/8W M FLM 1%	909
R2404	1B4	1136.2740	RES 1/8W M FLM 1%	274
R2405	7E1	1214.0103	RES 1/4W C FLM 5%	10K
R2406	4E1	1136.4991	RES 1/8W M FLM 1%	4.99K
R2501	5C7	1214.0103	RES 1/4W C FLM 5%	10K
R2502	8A2	1214.0203	RES 1/4W C FLM 5%	20K
R2601	3F3	1214.0103	RES 1/4W C FLM 5%	10K
R2602	2C8,2D8	1984.9104	RES	NET SIP 5% B 9 X 100K
R2701	5G3	1214.0202	RES 1/4W C FLM 5%	2.0K
R2702	5C5	1214.0103	RES 1/4W C FLM 5%	10K
R2801	2G5	1214.0101	RES 1/4W C FLM 5%	100
R2802	6D2	1214.0203	RES 1/4W C FLM 5%	20K
R2803	5B7	1214.0470	RES 1/4W C FLM 5%	47
R2901	1G3	1214.0103	RES 1/4W C FLM 5%	10K
R3101	9E2	1139.2003	RES 1/8W M FLM .1%	200K
R3102	9E2	1136.1821	RES 1/8W M FLM 1%	1.82K
R3103	9E2	1139.2003	RES 1/8W M FLM .1%	200K
R3104	9E3	1136.2430	RES 1/8W M FLM 1%	243
R3105	9D7	1214.0153	RES 1/4W C FLM 5%	15K
R3106	8E7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3107	8E7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3108	8F7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3109	8F7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3110	9F2	1136.2371	RES 1/8W M FLM 1%	2.37K
R3111	9F2	1139.1001	RES 1/8W M FLM .1%	1.00K
R3201	9F2	4412.0201	POT TRIM PC ENC	200
R3202	9F3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3203	9E3	1136.3091	RES 1/8W M FLM 1%	3.09K
R3204	9E4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3205	9F4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3206	9F4	1139.2001	RES 1/8W M FLM .1%	2.00K
R3207	9F4	1139.1001	RES 1/8W M FLM .1%	1.00K
R3208	9F5	1136.1003	RES 1/8W M FLM 1%	100K
R3209	9F5	1139.2001	RES 1/8W M FLM .1%	2.00K
R3210	9F5	1139.1001	RES 1/8W M FLM .1%	1.00K
R3211	9E5	1136.7500	RES 1/8W M FLM 1%	750
R3212	9E5	1136.2741	RES 1/8W M FLM 1%	2.74K
R3213	9F6	1139.1001	RES 1/8W M FLM .1%	1.00K
R3301	9E7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3302	9F7	1139.1001	RES 1/8W M FLM .1%	1.00K
R3303	9F7	1136.1782	RES 1/8W M FLM 1%	17.8K
R3304	9E6	1136.1401	RES 1/8W M FLM 1%	1.40K
R3401	6B5	1214.0229	RES 1/4W C FLM 5%	2.2
R3402	6B6	1214.0229	RES 1/4W C FLM 5%	2.2
R3403	4E1	1214.0103	RES 1/4W C FLM 5%	10K
R3501	2D8,2E8,10C8	1984.9104	RES	NET SIP 5% B 9 X 100K
R3601	5D6	1214.0470	RES 1/4W C FLM 5%	47
R3701	2B8,2C8	1984.9104	RES	NET SIP 5% B 9 X 100K
R4101	7A7	1214.0510	RES 1/4W C FLM 5%	51
R4201	10E4	1214.0332	RES 1/4W C FLM 5%	3.3K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4202	10E4	1214.0204	RES 1/4W C FLM 5%	200K
R4203	10F4	1214.0332	RES 1/4W C FLM 5%	3.3K
R4301	6E7	4413.0104	POT TRIM PC 10 TURN	100K
R4302	6E7	1136.2003	RES 1/8W M FLM 1%	200K
R4303	6E6	1136.4993	RES 1/8W M FLM 1%	499K
R4502	5C6	1214.0470	RES 1/4W C FLM 5%	47
R4901	2D4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R5101	8B1-8H1	1984.9680	RES NET SIP 5% B	9 X 68
R5102	8A2	1214.0134	RES 1/4W C FLM 5%	130K
R5103	8A3	1214.0102	RES 1/4W C FLM 5%	1K
R5104	10E2	1136.1821	RES 1/8W M FLM 1%	1.82K
R5201	10E3	1139.2001	RES 1/8W M FLM .1%	2.00K
R5202	10E3	1214.0105	RES 1/4W C FLM 5%	1M
R5203	10F2	1214.0471	RES 1/4W C FLM 5%	470
R5204	10F4	4413.0104	POT TRIM PC 10 TURN	100K
R5205	10E5,10G5	1984.4220	RES NET SIP 5% I	4 X 22
R5206	10E4	1214.0332	RES 1/4W C FLM 5%	3.3K
R5301	6D2	1214.0203	RES 1/4W C FLM 5%	20K
R5501	5E7	1214.0103	RES 1/4W C FLM 5%	10K
R5502	5E7	1214.0103	RES 1/4W C FLM 5%	10K
R6201	10B4	1214.0332	RES 1/4W C FLM 5%	3.3K
R6202	10B4	1214.0204	RES 1/4W C FLM 5%	200K
R6203	10C4	1214.0332	RES 1/4W C FLM 5%	3.3K
R6204	10A5,10D5	1984.4220	RES NET SIP 5% I	4 X 22
R6301	10C4,10F4	1985.4223	RES NET SIP 2% B	4 X 22K
R6401	5G5	1214.0201	RES 1/4W C FLM 5%	200
R6402	5C7	1214.0470	RES 1/4W C FLM 5%	47
R6403	10E8	1214.0470	RES 1/4W C FLM 5%	47
R6404	10E8	1214.0470	RES 1/4W C FLM 5%	47
R6501	6F4	1214.0470	RES 1/4W C FLM 5%	47
R6502	6C4	1214.0470	RES 1/4W C FLM 5%	47
R6601	2A3,2F3,2E4,2E5	1984.9472	RES NET SIP 5% B	9 X 4.7K
R6602	2H5	1985.4223	RES NET SIP 2% B	4 X 22K
R6901	1F4	1214.0103	RES 1/4W C FLM 5%	10K
R6902	3F3	1214.0103	RES 1/4W C FLM 5%	10K
R6903	1E6	1214.0102	RES 1/4W C FLM 5%	1K
R6904	1F6	1214.0102	RES 1/4W C FLM 5%	1K
R6905	1F6	1214.0102	RES 1/4W C FLM 5%	1K
R7101	10B2	1136.1821	RES 1/8W M FLM 1%	1.82K
R7201	10A3	1139.2001	RES 1/8W M FLM .1%	2.00K
R7202	10C3	1214.0105	RES 1/4W C FLM 5%	1M
R7203	10B2	1214.0471	RES 1/4W C FLM 5%	470
R7204	10B4	4413.0104	POT TRIM PC 10 TURN	100K
R7205	10A4	1214.0332	RES 1/4W C FLM 5%	3.3K
R7301	5F6	1214.0201	RES 1/4W C FLM 5%	200
R7302	5F5	1214.0104	RES 1/4W/C/FLM 5%	100K
R7303	10D2	1136.3572	RES 1/8W M FLM 1%	35.7K
R7304	10D1	1136.3650	RES 1/8W M FLM 1%	365
R7305	10D1	1136.3572	RES 1/8W M FLM 1%	35.7K
R7401	5F4	1214.0201	RES 1/4W C FLM 5%	200
R7402	5G4	1214.0200	RES 1/4W C FLM 5%	20
R7403	5G4	1214.0303	RES 1/4W C FLM 5%	30K

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R7404	5G4	1214.0103	RES 1/4W C FLM 5%	10K
R7405	5F4	1214.0103	RES 1/4W C FLM 5%	10K
R7407	5F3	1214.0471	RES 1/4W C FLM 5%	470
R7408	5G5	1214.0102	RES 1/4W C FLM 5%	1K
R7501	5A7	1214.0470	RES 1/4W C FLM 5%	47
R7601	2F3	1985.4223	RES NET SIP 2% B	4 X 22K
R7602	3E5	1214.0470	RES 1/4W C FLM 5%	47
R7603	3F5	1214.0470	RES 1/4W C FLM 5%	47
R7604	3G5	1214.0470	RES 1/4W C FLM 5%	47
R7701	2G1	1214.0470	RES 1/4W C FLM 5%	47
R7702	2G1	1214.0470	RES 1/4W C FLM 5%	47
R7901	1C3-1E3	1984.9103	RES NET SIP 5% B	9 X 10K
R8101	9B2	1139.2003	RES 1/8W M FLM .1%	200K
R8102	9A2	1136.1821	RES 1/8W M FLM 1%	1.82K
R8103	9B2	1139.2003	RES 1/8W M FLM .1%	200K
R8104	9B2	1136.2430	RES 1/8W M FLM 1%	243
R8105	8B7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8106	8B7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8107	8C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8108	8C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8109	9C2	1139.1001	RES 1/8W M FLM .1%	1.00K
R8110	9C2	1136.2491	RES 1/8W M FLM 1%	2.49K
R8111	9A7	1214.0153	RES 1/4W C FLM 5%	15K
R8201	9C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R8202	9A3	1136.3091	RES 1/8W M FLM 1%	3.09K
R8203	9B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R8204	9C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R8205	9C4	1139.2001	RES 1/8W M FLM .1%	2.00K
R8206	9C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R8207	9C5	1136.1003	RES 1/8W M FLM 1%	100K
R8208	9C5	1139.2001	RES 1/8W M FLM .1%	2.00K
R8209	9C5	1139.1001	RES 1/8W M FLM .1%	1.00K
R8210	9B5	1136.7500	RES 1/8W M FLM 1%	750
R8211	9A5	1136.2741	RES 1/8W M FLM 1%	2.74K
R8212	9C5	1139.1001	RES 1/8W M FLM .1%	1.00K
R8301	9B7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8302	9C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R8303	9C7	1136.1782	RES 1/8W M FLM 1%	17.8K
R8304	9A6	1136.1401	RES 1/8W M FLM 1%	1.40K
R8401	5B6	4412.0202	POT TRIM PC ENC	2K
R8402	5B6	1214.0202	RES 1/4W C FLM 5%	2.0K
R8501	1G5	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R8502	2D3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R8601	2G5	1214.0201.1	RES 1/4W C FLM 5% VERT	200
U141	1A6	3431.0337	VOLT REG NEG VAR TO220	LM337
U181	2F7,4E4	3326.0244	BUFFER 8X TRI-STATE	74ACT244
U210	8E2,8G2	3412.5532	OP AMP DUAL	5532
U220	7B6,7E7	3412.5532	OP AMP DUAL	5532
U221	7B4,7C4	3412.5532	OP AMP DUAL	5532
U230	7B3,7C3	3412.5532	OP AMP DUAL	5532
U231	7B2,7C2	3412.5532	OP AMP DUAL	5532
U241	1A3	3430.1317	VOLT REG POS VAR TO92	LM317L

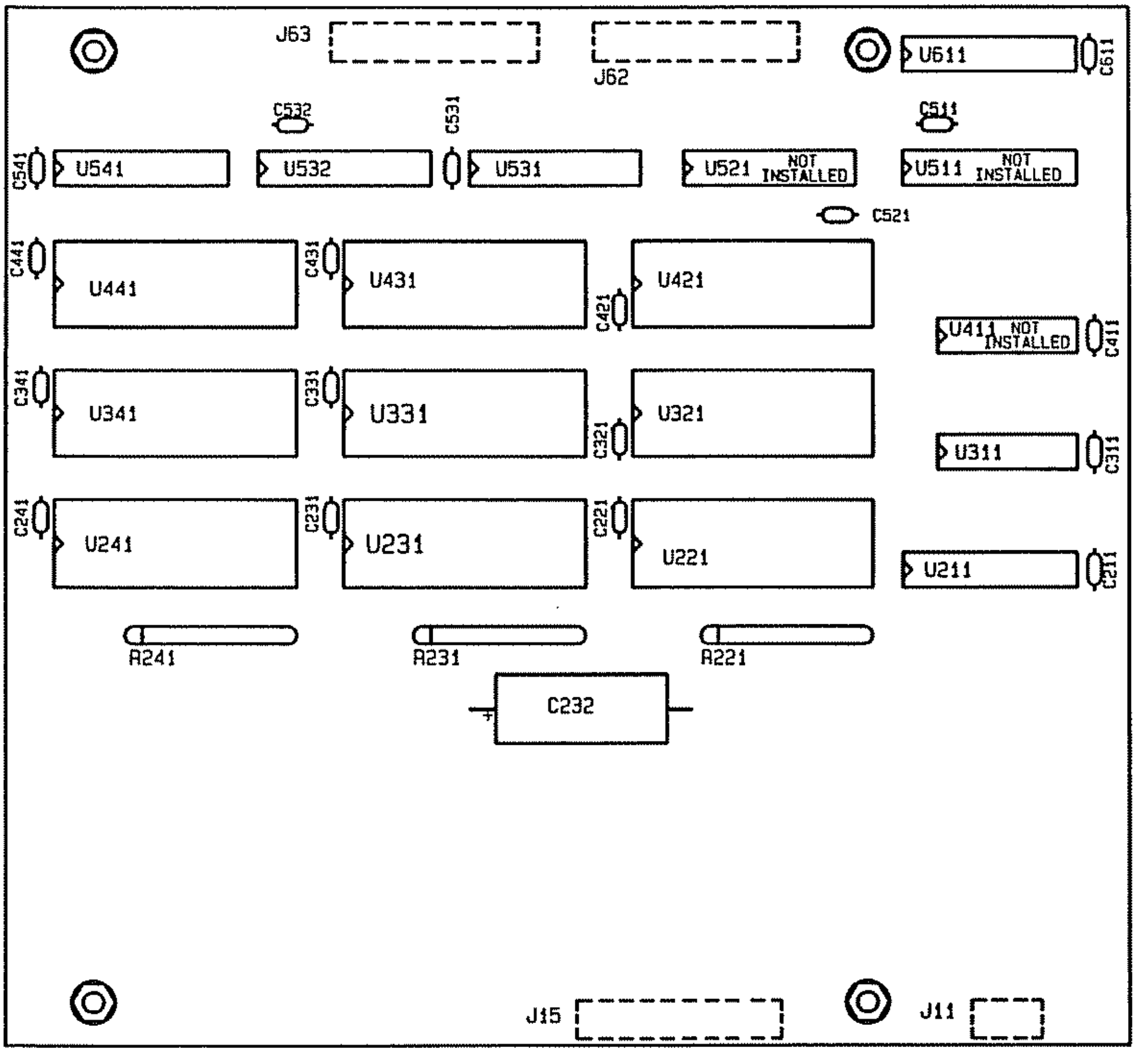
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U250	4A4	3325.0240	BUFFER 8X INV TRI-ST	74AC240
U251	4C2	3326.0595	SHIFT REG 8BIT W/LAT	74ACT595
U260	4C6	3326.0794	REGISTER 8X W/READBK	74ACT794
U261	4C2	3326.0595	SHIFT REG 8BIT W/LAT	74ACT595
U262	4C4	3325.0240	BUFFER 8X INV TRI-ST	74AC240
U263	5C2	3326.0590	COUNTER 8-BIT TRI-ST	74ACT590
U270	4E6	3326.0794	REGISTER 8X W/READBK	74ACT794
U271	5F2	3326.0590	COUNTER 8-BIT TRI-ST	74ACT590
U280	4A2	3326.0595	SHIFT REG 8BIT W/LAT	74ACT595
U281	4G4	3326.0794	REGISTER 8X W/READBK	74ACT794
U290	1G2	3342.16V8.S2	GEN.	ARRAY GAL16V8-15 DSP U290
U291	1F3,10C8	3326.0074	FLIP-FLOP 2X D	74ACT74
U340	6D5	3441.0056	CONVERTER D/A 16-BIT	PCM56
U341	6D7	3411.0844	OP AMP SINGLE	AD844
U360	5D4	3326.0794	REGISTER 8X W/READBK	74ACT794
U361	2E7	3326.0245.1	TRANSCVR	8X 3-ST SMD 74ACTQ245
U370	2C7	3326.0245.1	TRANSCVR	8X 3-ST SMD 74ACTQ245
U371	4B6	3326.0245.1	TRANSCVR	8X 3-ST SMD 74ACTQ245
U372	2B7	3326.0245.1	TRANSCVR	8X 3-ST SMD 74ACTQ245
U380	3E2	3724.2864	EEPROM CMOS 350ns	8K X 8
U390	1F3	3450.7705	SUPPLY VOLT SENSOR	5V
U410	8F7,9D8	3412.0275	OP AMP DUAL	OP275
U411	8F7,9E2	3412.5532	OP AMP DUAL	5532
U412	8F4	3323.4052	MULTIPLEX 4X DIFF	HC4052
U420	9F3,9E4	3412.5532	OP AMP DUAL	5532
U421	9E5,9F4	3412.5532	OP AMP DUAL	5532
U422	10E3	3441.5320	SAMPLE AND HOLD AMP	HA5320
U430	9E7,9F6	3412.5532	OP AMP DUAL	5532
U440	6E5	3441.0056	CONVERTER D/A 16-BIT	PCM56
U450	5D5	3342.20V8.S4	GEN.	ARRAY GAL20V8-15 DSP U450
U451	4G2	3342.16V8.S4	GEN.	ARRAY GAL16V8-15 DSP U451
U460	3B3	3722.6264	SRAM CMOS 25ns	8K X 8
U470	3B2	3722.6264	SRAM CMOS 25ns	8K X 8
U480	3B1	3722.6264	SRAM CMOS 25ns	8K X 8
U490	1C7	3326.0670	REGISTER FILE 4X4	74ACT670
U491	1C5	3326.0670	REGISTER FILE 4X4	74ACT670
U510	8E4	3323.4052	MULTIPLEX 4X DIFF	HC4052
U530	10F5	3441.0078	CONVERTER A/D 16-BIT	PCM78P
U540	6C3	3331.5803	DIGITAL FILTER	SM5803APT
U550	3F2,3G2,5D3,10D7	3323.0086	GATE 4-IN EXCL OR	74HC86
U560	3E3	3326.0245.1	TRANSCVR	8X 3-ST SMD 74ACTQ245
U561	3G3	3326.0245.1	TRANSCVR	8X 3-ST SMD 74ACTQ245
U570	3B5	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U571	3B6	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U580	3B7	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U590	1D5	3326.0670	REGISTER FILE 4X4	74ACT670
U610	8A4	3323.4051	MULTIPLEX 8X	HC4051
U611	8B6	3323.4052	MULTIPLEX 4X DIFF	HC4052
U612	8C7,9A8	3412.0275	OP AMP DUAL	OP275
U620	10B3	3441.5320	SAMPLE AND HOLD AMP	HA5320
U640	8B5,10D2	3412.0082	OP AMP DUAL	MC34082
U651	3D6	3326.0138	DECODER 3-LN/8-LN	74ACT138

REPLACEABLE ELECTRICAL PARTS LIST: 9DSP.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U652	6C4	3342.20V8.S6	GEN.	ARRAY GAL20V8-15 DSP U652
U660	2F4	3342.20V8.S6	GEN.	ARRAY GAL20V8-15 DSP U652
U710	8C6	3323.4052	MULTIPLEX 4X DIFF	HC4052
U711	8B7,8E7,9C3,9B4	3412.0275	OP AMP DUAL	OP275
U712	8B7,9B2,9B5	3412.5532	OP AMP DUAL	5532
U720	9C3	3412.5532	OP AMP DUAL	5532
U721	9C4	3412.5532	OP AMP DUAL	5532
U730	10B5	3441.0078	CONVERTER A/D 16-BIT	PCM78P
U731	9C6,9B7	3412.5532	OP AMP DUAL	5532
U740	10B7	3342.20V8.S7	GEN.	ARRAY GAL20V8-15 DSP U740
U742	10E7	3326.0590	COUNTER 8-BIT TRI-ST	74ACT590
U743	5F4,5G5	3422.0319	COMPARATOR	DUAL HI-SPEED LM319
U750	3E6	3326.0138	DECODER 3-LN/8-LN	74ACT138
U751	5D7,5A6,5B6	3326.0008	GATE 4 X 2-IN AND	74ACT08
U760	3E5	3341.20L8.S7	PRG	ARRAY PLUSC20L8-7 DSP U76
U761	3G4	3326.0138	DECODER 3-LN/8-LN	74ACT138
U770	2B2	3331.5600.1	uPROCESSOR SMD	DSP56001
U780	2B5	3331.5600.1	uPROCESSOR SMD	DSP56001
U790	1F5	3324.0273	FLIP-FLOP 8X D	74HCT273
U791	1D2	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
Y64	10A8	3910.2258	OSCILLATOR CMOS	22.5792MHz
Y74	5A5	3910.2458	OSCILLATOR CMOS	24.576MHz

→

MEM-1 MEMORY OPTION



MEMORY EXPANSION OPTION 9MEM.1000 (6200.MEM1.1 or 6400.MEM1.1)

MEM-1, EXPANDED MEMORY OPTION

NOTE: There have been two versions of the MEM option board. The version can be determined from the production code number located on the decal attached to the circuit board. The code number will have the format "MEMx-yyyyy-zz" where "x" is the MEM version.

Buffers and Address Decoding <1>

Schematic <1> shows the data and address bus interface to the DSP module. The 24 unbuffered data lines enter the board through connector J63. The unbuffered data lines are buffered by tri-state octal transceivers U541, U532 and U531. The direction of these buffers is controlled by buffered read strobe /BRD. They are enabled by /OPTBUF which is generated in the DSP module address decoder pal.

The 16 address lines A0 through A15 and several control lines enter the board through connector J62. The address lines are buffered by octal buffers U511 and U611 before driving the RAM array as BA0 through BA13. Address lines A14 and A15 are never used in buffered form.

Resistor networks R221, R231 and R241 pull the data bus high when tri-stated, preventing illegal logic levels and reducing power dissipation.

Mode Control <1>

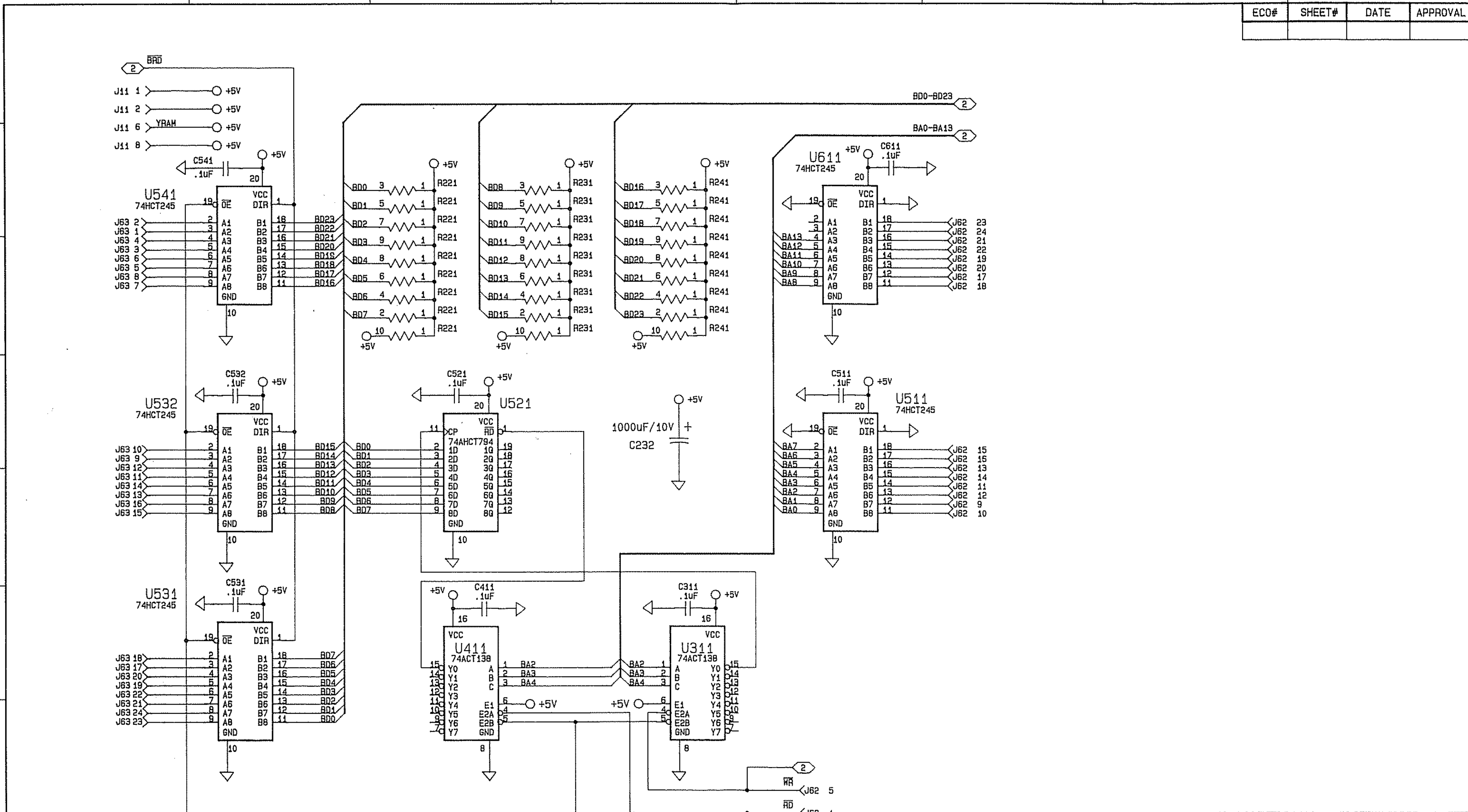
The addresses of I/O devices on board are selected by one-of-eight decoders U411 and U311. These select one of four address ranges, each 4 addresses wide. Decoder U311 decodes writes and U411 handles reads.

Octal latches U521 on schematic <1> latches mode control bits. They are strobed via pin 11 when the processor performs a write operation to the appropriate memory location. This latch may be read back by the processor when a read is performed from the same address. This readback is enabled via pin 1.

The mode control circuitry is not currently used on the MEM-1 option. Consequently the components associated with this function (U311, U411 and U521) are not present on the circuit board.

Expansion Data RAM <2>

The nine 32k-by-8 static RAMs on schematic <2> are organized into two banks of 48k by 24-bit memory. One bank is mapped into X memory space and one into Y memory space. The X/Y select line from the processor is buffered by one section of octal buffer U211 and used to drive the most significant address bit of each RAM. Read and write strobe signals from the processor are buffered in two more sections of U211 and used to drive the output enable and write enable pins respectively of each RAM. The chip enable signals for each set of three RAMs is obtained from the DSP module address decoder pal via J62.



Audio precision

P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 06/25/92

TITLE MEMORY EXPANSION OPTION 1

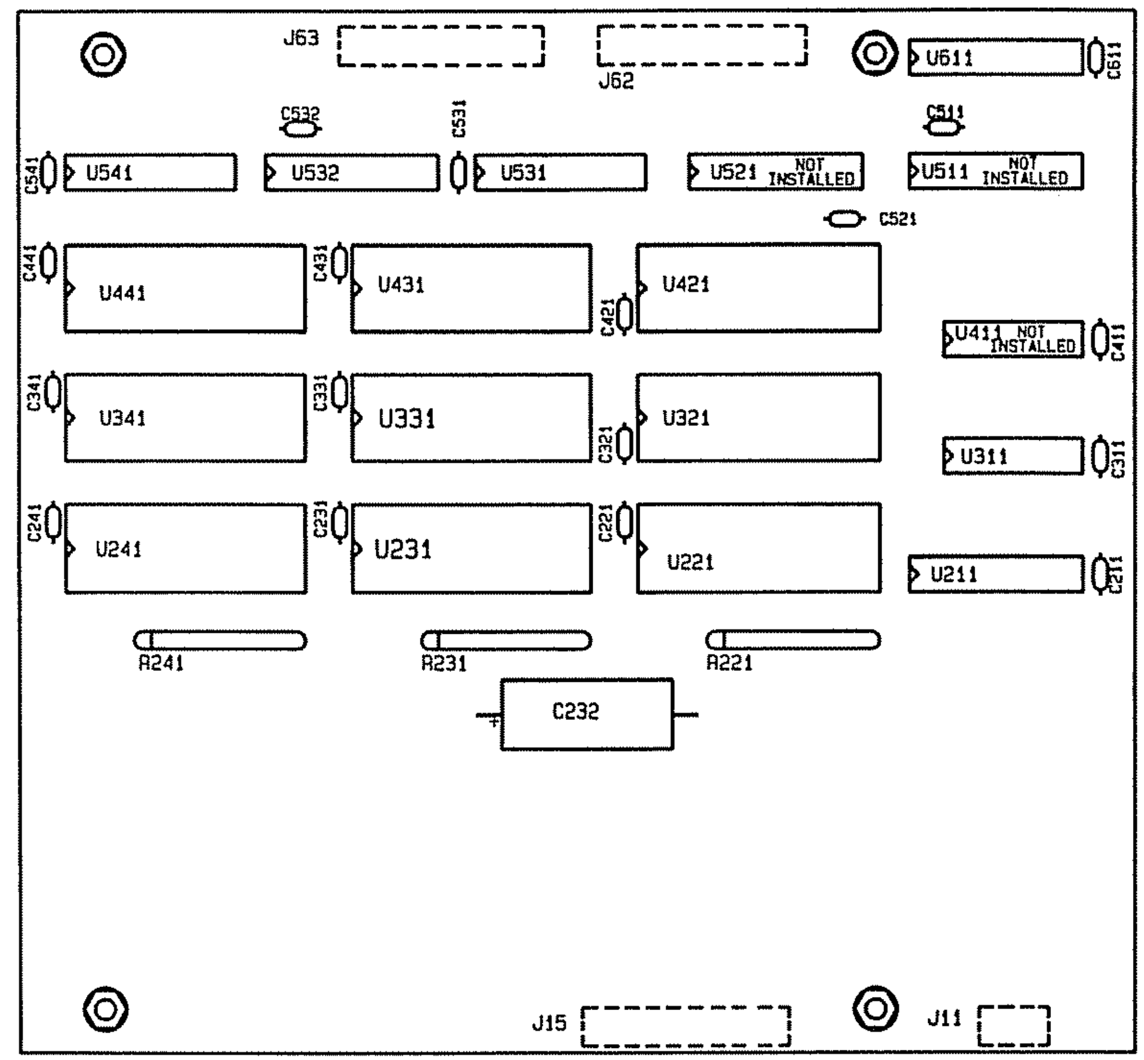
SCALE SIZE B

DRAWING NO. 9MEM.1000

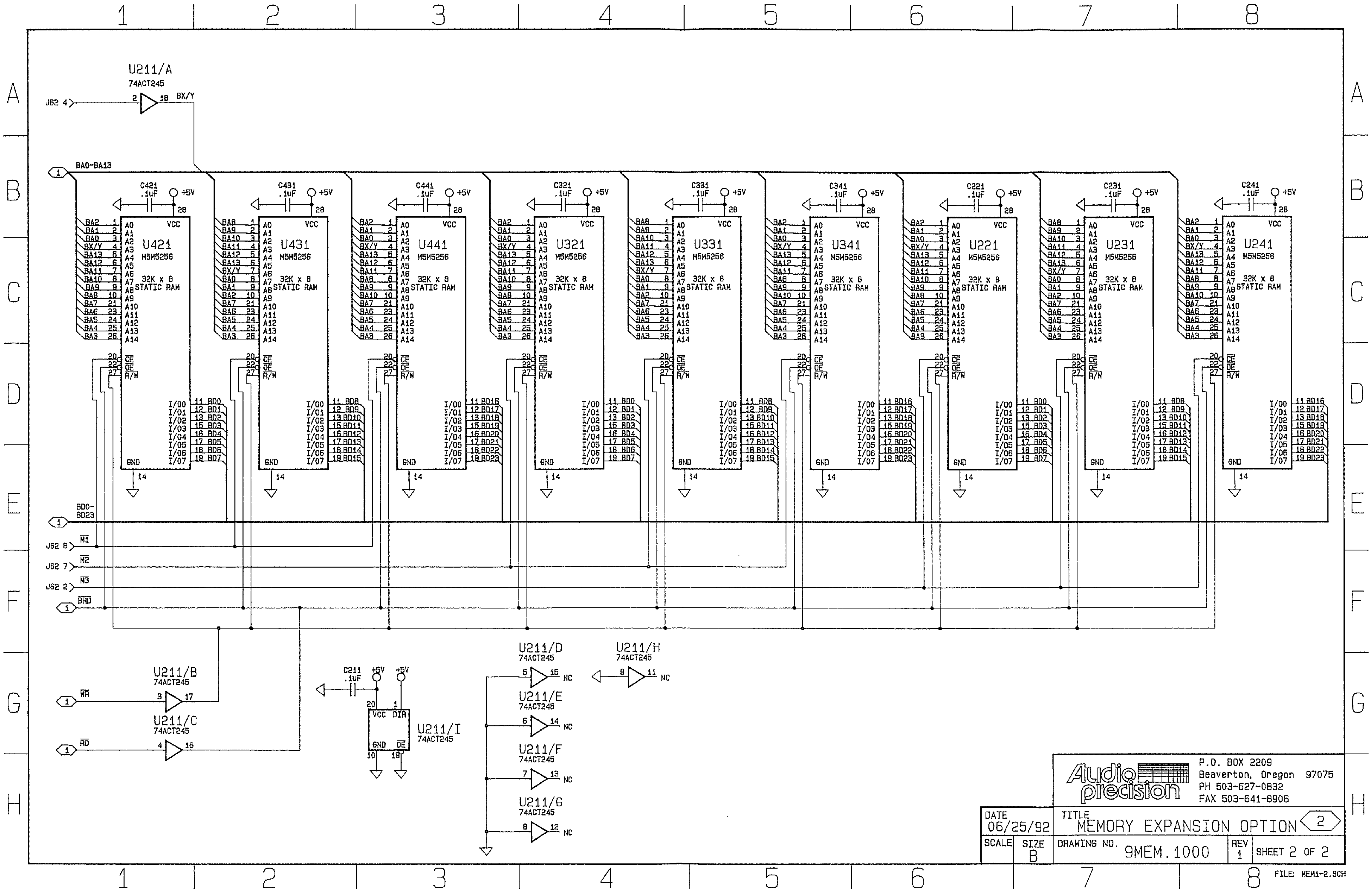
REV 1

SHEET 1 OF 2

FILE: MEM1-1.SCH

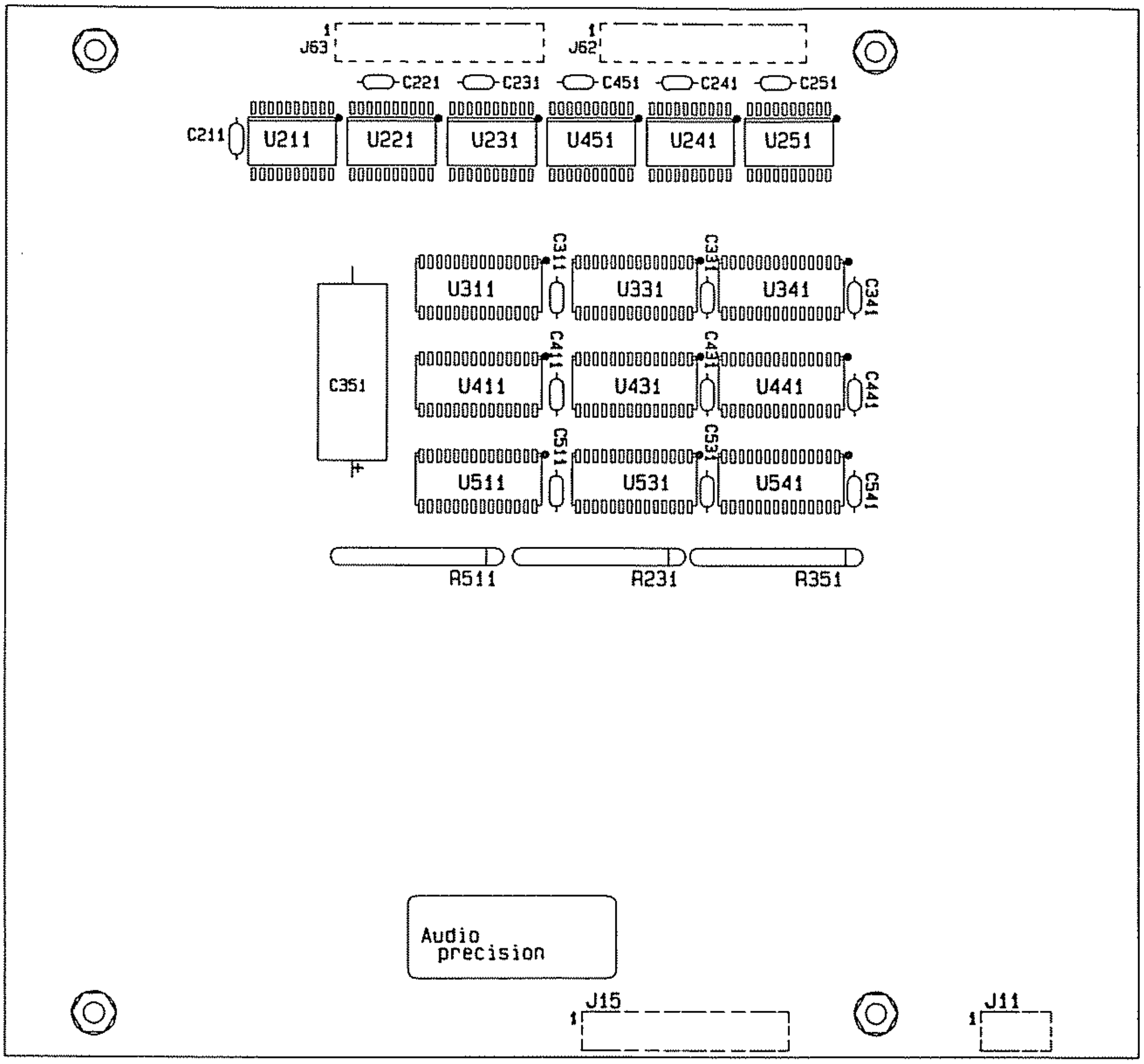


MEMORY EXPANSION OPTION 9MEM.1000 (6200.MEM1.1 or 6400.MEM1.1)


U211/A 74ACT245
J62 4
BX/Y
BA0-BA13
C421 .1uF +5V
C431 .1uF +5V
C441 .1uF +5V
C321 .1uF +5V
C331 .1uF +5V
C341 .1uF +5V
C221 .1uF +5V
C231 .1uF +5V
C241 .1uF +5V
U421 M5M5256 32K x 8 STATIC RAM
U431 M5M5256 32K x 8 STATIC RAM
U441 M5M5256 32K x 8 STATIC RAM
U321 M5M5256 32K x 8 STATIC RAM
U331 M5M5256 32K x 8 STATIC RAM
U341 M5M5256 32K x 8 STATIC RAM
U221 M5M5256 32K x 8 STATIC RAM
U231 M5M5256 32K x 8 STATIC RAM
U241 M5M5256 32K x 8 STATIC RAM
BD0-BD23
J62 8 M1
J62 7 M2
J62 2 M3
BRD
WR
RD
U211/B 74ACT245
U211/C 74ACT245
C211 .1uF +5V +5V
U211/I 74ACT245
U211/D 74ACT245
U211/E 74ACT245
U211/F 74ACT245
U211/G 74ACT245
U211/H 74ACT245
NC
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 06/25/92
TITLE MEMORY EXPANSION OPTION 2
SCALE
SIZE B
DRAWING NO. 9MEM.1000
REV 1
SHEET 2 OF 2
FILE: MEM1-2.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C211	2A4	2172.0104	CAP CERAM 100V 20%	1uF
C221	2D2	2172.0104	CAP CERAM 100V 20%	1uF
C231	2D1	2172.0104	CAP CERAM 100V 20%	.1uF
C232	1C3	2911.0108	CAP AL-EL 10V +80/-20%	1000uF
C241	2D1	2172.0104	CAP CERAM 100V 20%	.1uF
C311	1B3	2172.0104	CAP CERAM 100V 20%	.1uF
C321	2D3	2172.0104	CAP CERAM 100V 20%	.1uF
C331	2D2	2172.0104	CAP CERAM 100V 20%	.1uF
C341	2D2	2172.0104	CAP CERAM 100V 20%	.1uF
C411	1B3	2172.0104	CAP CERAM 100V 20%	.1uF
C421	2D4	2172.0104	CAP CERAM 100V 20%	.1uF
C431	2D4	2172.0104	CAP CERAM 100V 20%	.1uF
C441	2D3	2172.0104	CAP CERAM 100V 20%	.1uF
C511	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C521	1B3	2172.0104	CAP CERAM 100V 20%	.1uF
C531	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C532	1C4	2172.0104	CAP CERAM 100V 20%	.1uF
C541	1D4	2172.0104	CAP CERAM 100V 20%	.1uF
C611	1D2	2172.0104	CAP CERAM 100V 20%	.1uF
E221	2C2	4232.1028	SOCKET IC WIDE	28 PIN
E231	2D1	4232.1028	SOCKET IC WIDE	28 PIN
E241	2C1	4232.1028	SOCKET IC WIDE	28 PIN
E321	2C3	4232.1028	SOCKET IC WIDE	28 PIN
E331	2C2	4232.1028	SOCKET IC WIDE	28 PIN
E341	2C2	4232.1028	SOCKET IC WIDE	28 PIN
E421	2D4	4232.1028	SOCKET IC WIDE	28 PIN
E431	2C4	4232.1028	SOCKET IC WIDE	28 PIN
E441	2C3	4232.1028	SOCKET IC WIDE	28 PIN
J11	1D4,1A4	4221.1008	JACK PC 2 X .1	8 PIN
J15	1A2	4221.1024	JACK PC 2 X .1	24 PIN
J62	1A2,2B4,2D4,1B2,1C2,1D2	4221.1024	JACK PC 2 X .1	24 PIN
J63	1A4,1B4,1C4,1D4	4221.1024	JACK PC 2 X .1	24 PIN
R221	1D3	1984.9104	RES NET SIP 5% B	9 X 100K
R231	1D3	1984.9104	RES NET SIP 5% B	9 X 100K
R241	1D3	1984.9104	RES NET SIP 5% B	9 X 100K
U211	2D4,2A3,2A4	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U221	2C2	3722.5256.1	SRAM CMOS 85ns	32K X 8
U231	2D1	3722.5256.1	SRAM CMOS 85ns	32K X 8
U241	2C1	3722.5256.1	SRAM CMOS 85ns	32K X 8
U321	2C3	3722.5256.1	SRAM CMOS 85ns	32K X 8
U331	2C2	3722.5256.1	SRAM CMOS 85ns	32K X 8
U341	2C2	3722.5256.1	SRAM CMOS 85ns	32K X 8
U421	2D4	3722.5256.1	SRAM CMOS 85ns	32K X 8
U431	2C4	3722.5256.1	SRAM CMOS 85ns	32K X 8
U441	2C3	3722.5256.1	SRAM CMOS 85ns	32K X 8
U511	1C2	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U531	1B4	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U532	1C4	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U541	1D4	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U611	1D2	3326.0245	TRANSCVR 8X TRI-ST	74ACT245

MEM-2 MEMORY OPTION



MEMORY EXPANSION OPTION 9MEM.2000 (6400.MEM2.1)

MEM-2, EXPANDED MEMORY OPTION

NOTE: There have been two versions of the MEM option board. The version can be determined from the production code number located on the decal attached to the circuit board. The code number will have the format "MEMx-yyyyy-zz" where "x" is the MEM version.

Buffers and Address Decoding <1>

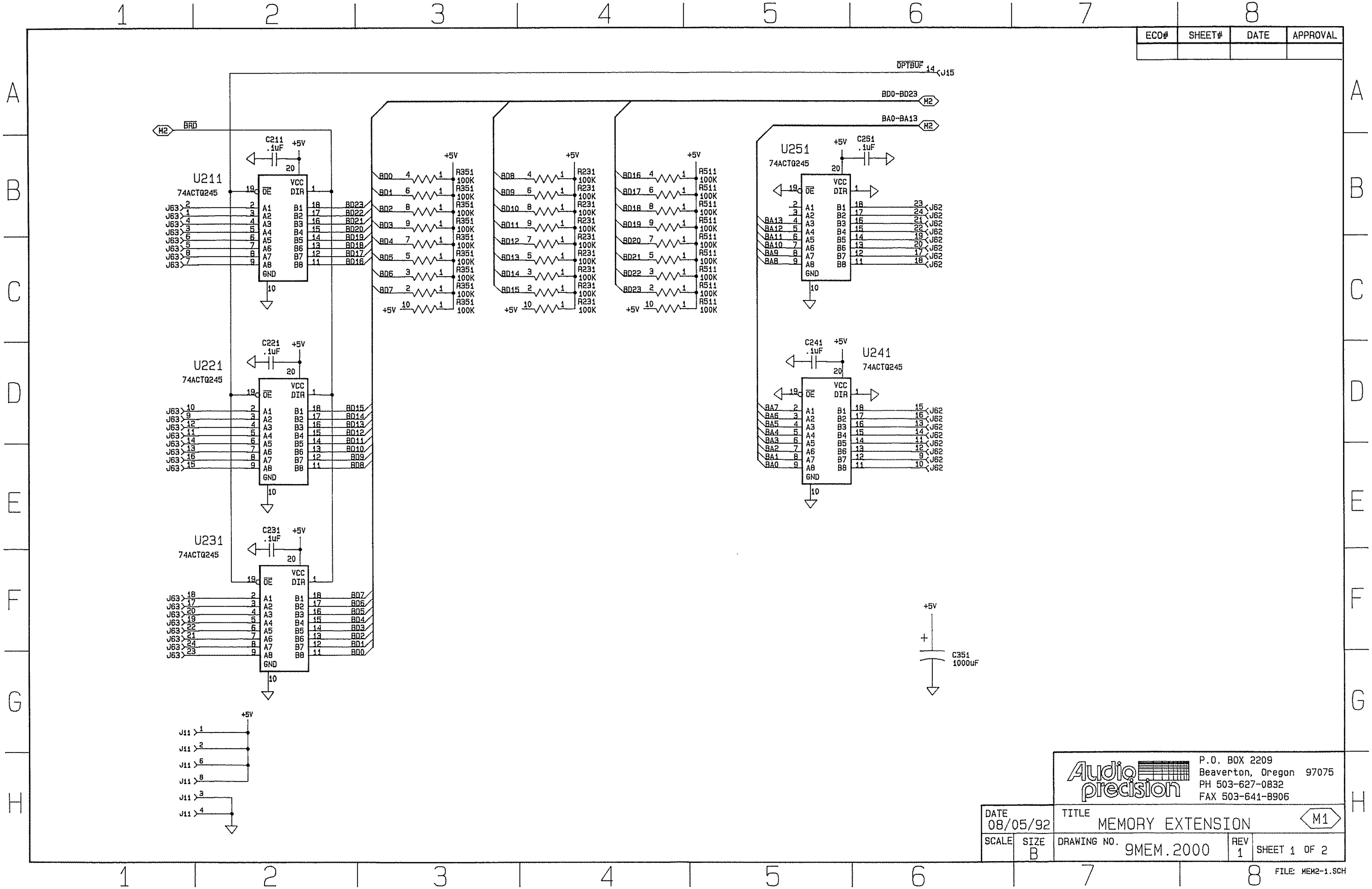
Schematic <1> shows the data and address bus interface to the DSP module. The 24 unbuffered data lines enter the board through connector J63. The unbuffered data lines are buffered by tri-state octal transceivers U211, U221 and U231. The direction of these buffers is controlled by buffered read strobe /BRD. They are enabled by /OPTBUF which is generated in the DSP address decoder pal.

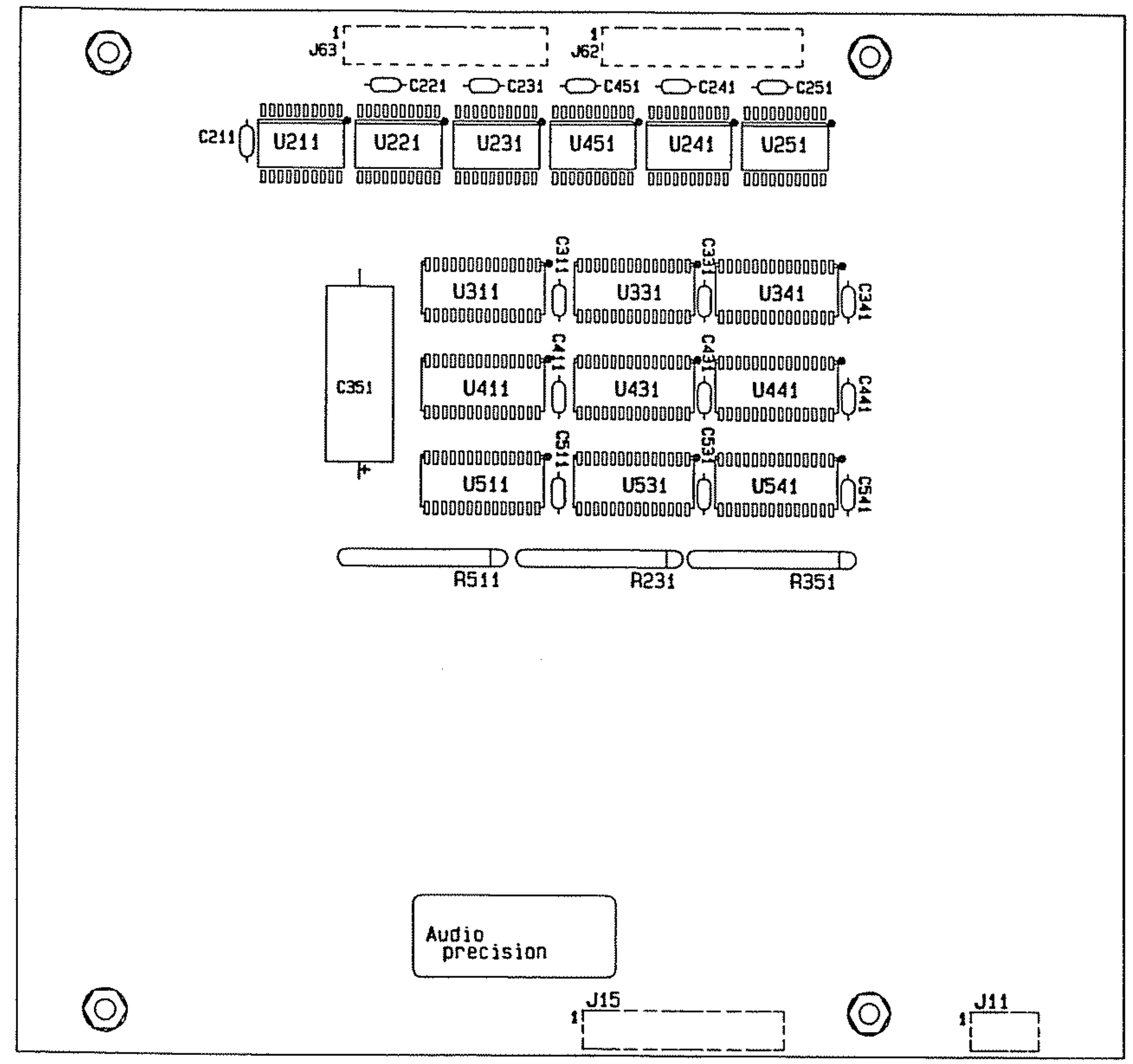
The 16 address lines A0 through A15 and several control lines enter the board through connector J62. The address lines are buffered by octal buffers U241 and U251 before driving the RAM array as BA0 through BA13. Address lines A14 and A15 are never used in buffered form.

Resistor networks R351, R231 and R511 pull the data bus high when tri-stated, preventing illegal logic levels and reducing power dissipation.

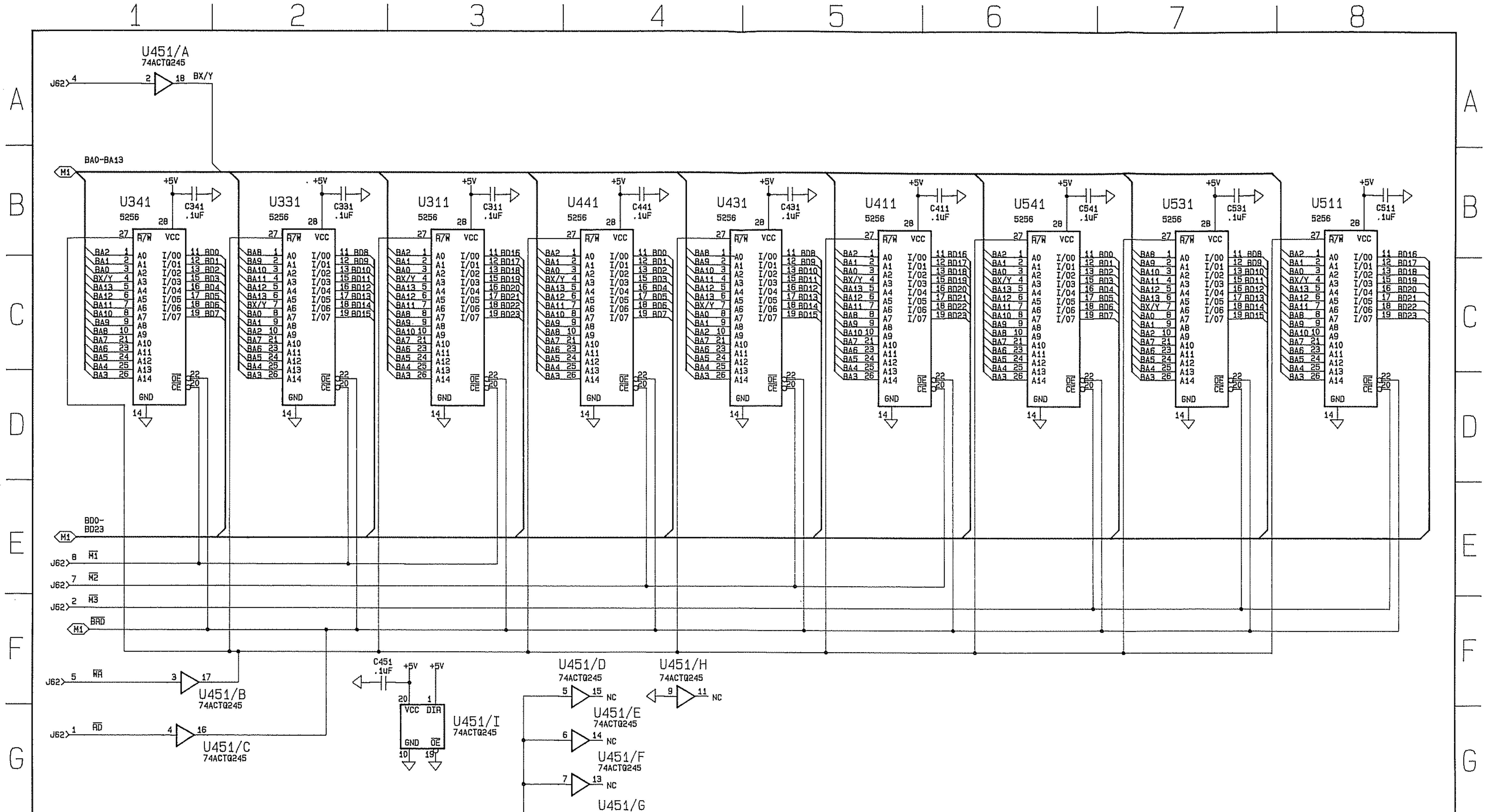
Expansion Data RAM <2>

The nine 32k-by-8 static RAMs on schematic <2> are organized into two banks of 48k by 24-bit memory. One bank is mapped into X memory space and one into Y memory space. The X/Y select line from the processor is buffered by one section of octal buffer U451 and used to drive the most significant address bit of each RAM. Read and write strobe signals from the processor are buffered in two more sections of U451 and used to drive the output enable and write enable pins respectively of each RAM. The chip enable signals for each set of three RAMs is obtained from the DSP address decoder pal via J62.


ECO#
SHEET#
DATE
APPROVAL
U211
74ACTQ245
U221
74ACTQ245
U231
74ACTQ245
U251
74ACTQ245
U241
74ACTQ245
OPTBUF
J15
BD0-BD23
BA0-BA13
BRD
C351
1000uF
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
08/05/92
TITLE
MEMORY EXTENSION
M1
SCALE
SIZE
B
DRAWING NO.
9MEM.2000
REV
1
SHEET 1 OF 2
FILE: MEM2-1.SCH



MEMORY EXPANSION OPTION 9MEM.2000 (6400.MEM2.1)



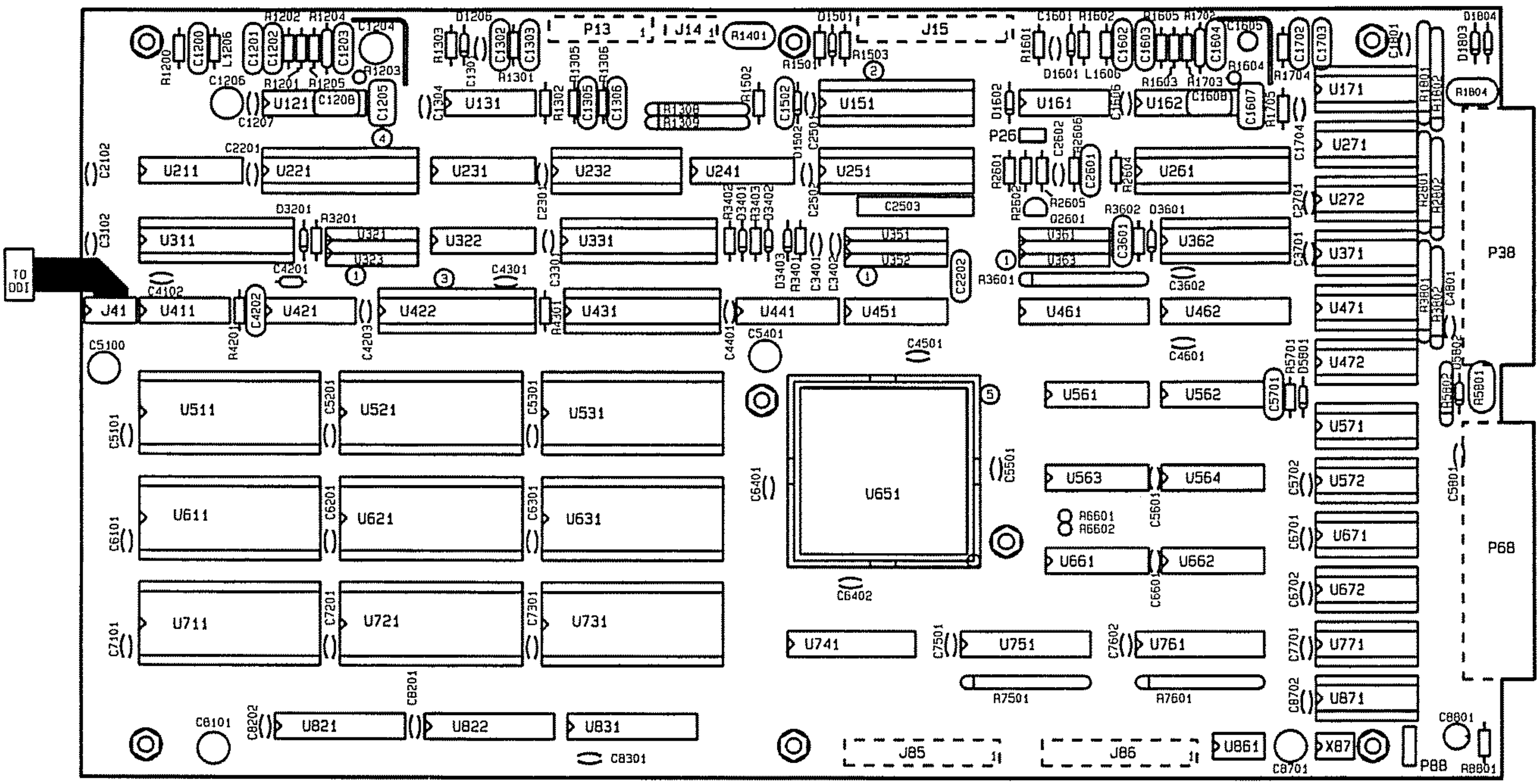
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE		
08/05/92	MEMORY EXTENSION		M2
SCALE / SIZE B	DRAWING NO. 9MEM.2000	REV 1	SHEET 2 OF 2

FILE: MEM2-2.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C211	1B2	2172.0104	CAP CERAM 100V 20%	.1uF
C221	1D2	2172.0104	CAP CERAM 100V 20%	.1uF
C231	1E2	2172.0104	CAP CERAM 100V 20%	.1uF
C241	1D5	2172.0104	CAP CERAM 100V 20%	.1uF
C251	1B6	2172.0104	CAP CERAM 100V 20%	.1uF
C311	2B3	2172.0104	CAP CERAM 100V 20%	.1uF
C331	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C341	2B1	2172.0104	CAP CERAM 100V 20%	.1uF
C351	1F6	2911.0108	CAP AL-EL 10V +80/-20%	1000uF
C411	2B6	2172.0104	CAP CERAM 100V 20%	.1uF
C431	2B5	2172.0104	CAP CERAM 100V 20%	.1uF
C441	2B4	2172.0104	CAP CERAM 100V 20%	.1uF
C451	2F3	2172.0104	CAP CERAM 100V 20%	.1uF
C511	2B8	2172.0104	CAP CERAM 100V 20%	.1uF
C531	2B7	2172.0104	CAP CERAM 100V 20%	.1uF
C541	2B6	2172.0104	CAP CERAM 100V 20%	.1uF
J11	1G1, 1H1	4221.1008	JACK PC 2 X .1	8 PIN
J15	1A6	4221.1024	JACK PC 2 X .1	24 PIN
J62	2A1,2E1-2G1,1B6-1E6	4221.1024	JACK PC 2 X .1	24 PIN
J63	1A1-1G1	4221.1024	JACK PC 2 X .1	24 PIN
R231	1B4, 1C4	1984.9104	RES NET SIP 5% B	9 X 100K
R351	1B3, 1C4	1984.9104	RES NET SIP 5% B	9 X 100K
R511	1B5, 1C5	1984.9104	RES NET SIP 5% B	9 X 100K
U211	1B2	3326.0245.1	TRANSCVR 8X 3-ST SMD74ACTQ245	
U221	1D2	3326.0245.1	TRANSCVR 8X 3-ST SMD74ACTQ245	
U231	1F2	3326.0245.1	TRANSCVR 8X 3-ST SMD74ACTQ245	
U241	1D5	3326.0245.1	TRANSCVR 8X 3-ST SMD74ACTQ245	
U251	1B5	3326.0245.1	TRANSCVR 8X 3-ST SMD74ACTQ245	
U311	2C3	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U331	2C2	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U341	2C1	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U411	2C5	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U431	2C4	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U441	2C4	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U451	1A1, 2G1-2G4	3326.0245.1	TRANSCVR 8X 3-ST SMD74ACTQ245	
U511	2C8	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U531	2C7	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U541	2C6	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8

DIO-1 DIGITAL I/O MODULE



NOTES:

1. U323, U352, U363 are mounted on top of U321, U351, U361.
2. R1504, R1505 are mounted under U151 on solderside.
3. R4202, R4203 are mounted under U422 on solderside.
4. R2202 is mounted under U221 on solderside.
5. R6501 R6502 are mounted under U651 on solderside.

DIGITAL INPUT/OUTPUT OPTION 9DIO.1000 (6400.DIO1.2)

DIO-1, DIGITAL AUDIO INPUT/OUTPUT MODULE

NOTE: There have been two versions of the DIO module. The version can be determined from the production code number located on the decal attached to the circuit board. The code number will have the format "DIOx-yyyyy-zz" where "x" is the DIO version.

Buffers and Address Decoding <1>

Schematic <1> shows the data and address bus interface to the DSP module. The 24 unbuffered data lines enter the board through connector J86. The unbuffered data lines are buffered by tri-state octal transceivers U741, U751 and U761. The direction of these buffers is controlled by buffered read strobe /BRD. They are enabled by AIOII which is generated in the DSP module address decoder pal.

The 16 address lines A0 through A15 and several control lines enter the board through connector J85. The address lines are buffered by octal buffers U822 and U831 before driving the RAM array as BA0 through BA14. Address line A15 is never used in buffered form. The lowest two address lines (A0 and A1) also drive I/O devices and are therefore buffered separately for this by two sections of U821. A0 and A1 become BA30 and BA31 after buffering.

The addresses of I/O devices on board are selected by one-of-eight decoders U351 and U451. These select one of four address ranges, each 4 addresses wide. Decoder U351 decodes writes and U451 handles reads.

Word Reversal Latches <1>

Register files U561, U562, U563, U564, U661 and U662 form a 4 deep by 24-bit wide set of word reversal latches. Their input bits are wired in opposite order to their output bits. Any data written to the buffers will be read back in bit reverse order. This means that the LSB will be swapped with the MSB. Bit 1 will be swapped with bit 22, etc. Since the registers are four deep, four separate data words may be written to this array for later readback.

Mode Control <1>

Octal latches U461 and U462 on schematic <1> latch mode and sample rate control bits. They are strobed via pin 11 when the processor performs a write operation to the appropriate memory location. These latches may be read back by the processor when a read is performed from the same address. This readback is enabled via pin 1.

The most significant bit of U462 is clamped by zener diode D3601 and routed to a rear panel bnc connector via R2605. Bit 22 is latched in U462, clamped by zener diode D3402 and routed to the 15-pin rear panel connector via R3403.

Status Buffer <1>

Half of octal tri-state buffer U362 is used to read the state of four status bits on the DIO-1 board. These are the AES/EBU receiver phase lock loop lock indicator (RLOCK), house sync phase lock loop lock indicator (TLOCK), the option dsp bus request output (OPTBUSREQ) and an auxiliary data input from the 15-pin rear panel serial connector (AUX1).

Expansion Data RAM <2>

The nine 32k-by-8 static RAMs on schematic <2> are organized into two banks of 48k by 24-bit memory. One bank is mapped into X memory space and one into Y memory space. The X/Y select line from the processor is buffered by one section of octal buffer U831 and used to drive the most significant address bit of each RAM. Read and write strobe signals from the processor are buffered in two more sections of U821 and used to drive the output enable and write enable pins respectively of each RAM. The chip enable signals for each set of three RAMs is obtained from the DSP address decoder pal via J85.

Data Bus Termination <3>

Resistor networks R3601, R7501 and R7601 pull the data bus high when tri-stated, preventing illegal logic levels and reducing power dissipation.

Parallel Digital Input <3>

The parallel input accepts two channels of 24-bit data on a rear panel 34-pin connector and latches it when the strobe line is low. The data is latched into the channel A input when the channel select line is held low and the strobe is asserted. The data is latched into the channel B input when the channel select line is held high and the strobe is asserted. Latching channel B data also generates an interrupt for the System One, causing it to read both channels of data just written to the latches. The channel select line must be held either high or low during the entire time the strobe line is low. A transition on the channel select line while the strobe line is low will cause an incorrect latch operation. Note that data must always be supplied to Channel B since its latch operation triggers the dsp to read the data. If a single channel interface is desired it must therefore be configured as Channel B and the channel select line connected to +5V.

The parallel input consists of 4 x 4 register files U571, U572, U671, U672, U771 and U871. Only two sections of each is used, forming a dual 24 bit wide latch. One latch is dedicated to each input channel. The channel selection bit is applied to pin 28 of the connector. This is buffered by one section of octal buffer U362 and applied to an address select input of the register files. Clamp diode D5801 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R5701 and capacitor C5701 reduce the effect of external cable crosstalk and noise. The write strobe is active low and is applied to pin 30 of the interface. This is buffered by one section of octal buffer U362. Clamp diode D5802 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R3602 and capacitor C3601 reduce the effect of external cable crosstalk and noise. The channel select and strobe inputs are internally pulled high by R5802. Strobe pulses are gated with the channel select line and coupled to the processors interrupt selection logic by an AND gate in U261. The processor will be interrupted (signalling new input data) only when the channel select line is high (channel B writes).

Parallel Digital Output <3>

The output port provides 24-bit data on the data lines at all times. The channel select line determines which channels data appears on these lines. The read strobe line causes both channels of data to be updated and signals the System One processor that another pair of data words are required. The data is buffered with a two stage FIFO which guarantees that data will be available when needed rather than after the service delay of the processor. As long as the maximum sample rate restriction is obeyed the two stage buffer will never empty. If a single channel output is desired the port may be configured as Channel B or Channel A and the channel select line connected to +5V or ground, respectively.

The parallel output consists of 4 x 4 register files U171, U271, U272, U371, U471 and U472. All four sections of each are used, creating four 24-bit wide latches. Two latches are dedicated to each output channel. The channel selection bit is applied to pin 28 of the connector. This is buffered by one section of octal buffer U362 and applied to an address select input of the register files. Clamp diode D1803 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R1705 and capacitor C1703 reduce the effect of external cable crosstalk and noise. The read strobe is active low and is applied to pin 30 of the interface. This is buffered by one section of octal buffer U362 and applied to the read enable input of the register files. Clamp diode D1804 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R2604 and capacitor C2601 reduce the effect of external cable crosstalk and noise. The channel select and strobe inputs are internally pulled high by resistor network R5802. Strobe pulses are gated with the channel select line and coupled to the processors interrupt selection logic by an AND gate in U261. The processor will be interrupted (signalling new output data) only when the channel select line is high (channel B reads). The gated read strobe also causes flip-flop U361 to change state. The Q and /Q outputs are wired to the second address inputs of the register files. When a read is performed the two data latches are swapped with a alternate set. This creates a two stage FIFO, allowing the processor to update the channels consecutively without the interchannel delay being visible externally.

The 24 data output lines are isolated by resistor networks R3801, R3802, R2801, R2802, R1801 and R1802. These provide some damping when driving long lines and limit the rise time. There are no clamping circuits to prevent damage on either the input or output bits. Since this greatly increases the risk of damage due to misuse, all register files have been mounted in sockets. Both the parallel input and output connectors provide +5V on a connector pin through a series thermistor. These limit the current under short circuit conditions to prevent overloading of the System One power supply.

The parallel inputs and outputs may be operated at any sample rate selectable from the panel of the dsp program being run. The internal sample clock generator can produce a square wave sample clock at 32 kHz, 44.1 kHz or 48 kHz. The dsp program in use may limit the choice of sample rates based on processing time limitations. Many of the dsp programs limit the maximum sample rate to 48 kHz.

AES/EBU Interface Hardware

A block diagram of the AES/EBU interface circuitry contained in the Audio Precision System One Dual Domain test system is shown in Figure DIO1.1. Signal generation timing may be driven from the internal crystal oscillators or may be slaved to the received signal or an external sync signal. The external sync signal drives a phase locked loop to generate the high frequency clock (128 x Fs) necessary for clocking the internal logic. The hardware is timed by a master timing generator which is clocked from the selected source. The preambles are always generated with the same polarity to allow testing of polarity sensitivity in the device under test. The interface dsp then outputs the serial data signal with bit reversed order to the transmit logic at the appropriate time in the transmitted word. After the last bit in the data stream the validity, user and status bits are selected. These are bi-phase mark encoded in hardware, converted to a differential signal and output. An appropriately attenuated version is also output to drive consumer interface devices.

On the receive side, the input signal is taken from its balanced form and converted to an unbalanced form by the transformer and line receiver. This drives a sync detector and phase lock loop clock generator identical to that used for the external sync input. This clock operates the preamble detector and bi-phase decoder and is available to drive the transmit logic. The preamble detector identifies the presence of one of the three valid preambles and outputs a channel select signal indicating which channel is being received. When a block preamble is detected a pulse is generated lasting one frame indicating that the words being received are the first in the block. The bi-phase decoder takes the encoded data and flag bits and recreates a NRZ data stream. The data separator passes the audio data to the dsp serial input and latches the flag bits for later examination. A parity checker also accesses the NRZ data stream to compute parity on the data and flag bits.

AES/EBU and Serial Inputs <4>

In units manufactured before January 1991, the signal from the front panel enters the board via P11A. It is coupled through transformer X310 into differential line receiver U401A. The output of this gate is a ground referenced AES/EBU signal. In units manufactured after January 1991, components C4401, X310, and U401 are deleted and functionally moved to the DDI-3 circuit board mounted directly behind the front panel connectors. In these units the ground referenced AES/EBU input signal enters the DIO-1 board via J41 and is labeled DDI_IN.

Programmable logic device U422 detects the sync preambles in the DDI_IN signal to provide a reference for the phase lock loop. There are two sync detector circuits inside U422, one is used for 32 kHz and the other for 44.1 kHz and 48 kHz sample rates. Pin 21 of U422 goes low whenever the 32 kHz sync detector finds a sync preamble. The combination of R3201, D3201 and C4203 senses this and holds pin 5 of U422 low if syncs are detected. The output on pin 20 will then be the output of the 32 kHz sync detector. If no syncs are detected pin 5 will go high and the 44.1kHz/48kHz detector will be enabled. The output on pin 20 will then be the output of the 44.1kHz/48kHz detector. Since preambles occur at the beginning of each channel of data the signal at the output of U422 will be at twice the audio sample rate.

The DDI_IN signal is also fed to a delay circuit consisting of R1302, C1303, U131, R1301 and C1302. The delayed signal drives shift register U411 and an exclusive-OR edge detector consisting of R4201, C4202 and part of U323. Its output is used to re-clock the sync preamble detection pulse in flip-flop U321. A high frequency clock at 256 times the audio sample rate is generated by a phase lock loop consisting of U121, U211 and the associated components. The phase lock loop U121 contains a phase detector, VCO and lock detect circuit. The re-clocked output of the sync detector from U321 drives the pin 14 input of the phase detector through U261. The reference input (pin 3) of the phase detector normally comes from the divide by 128 output of the counter through U251 (acting as a switch). The VCO center frequency and tuning range is determined by C1203, R1204 and R1205. The phase detector output is filtered by R1201, R1202 and C1202 to produce the loop control voltage into the VCO. The loop will seek a point at which the VCO output frequency is correct to produce equal input frequencies at the two phase detector inputs.

The outputs of the shift register U411 will be 8 consecutive cells in the AES/EBU signal. When U311 detects a preamble at these outputs it indicates whether it is a channel A, channel B or block sync type. This is used to create a channel A/channel B signal (SIA/B at pin 17) and a start of block signal (SIBLK at pin 16). A word sync output is also derived which pulses at the end of each channel A preamble to synchronize the bit counter U231.

The bit counter U231 tracks the current position in the AES/EBU word. This count is decoded by U221 and used to create the bit clock and word clock necessary to drive the dsp serial input port. The first two outputs of shift register U411 are decoded in U221 to create normal binary data from the bi-phase encoded data. This data is gated in U221 before being routed to the dsp serial input. The status, validity and user bits of the serial stream are also decoded and latched in U221 before driving dedicated input pins on the processor. U221 also derives the parity information for the received bits and this is latched in U321A. The parity flag (SIPARITY) is connected to an additional input of the processor.

AES/EBU Transmitter <5>

The clock to drive the AES/EBU transmit circuitry is at 128 times the sample rate and is selected by U251. Either the internal crystal oscillators, the AES/EBU receiver, or the house sync input may be used as the selected clock source. The selected clock source drives a 16 bit counter consisting of U322 and U441. The lower 7 bits of the counter serve as an address for registered ROM U331. The ROM generates control and data signals for the bi-phase encoder U431 and the dsp processor U651. The timing diagram of the transmit circuitry is illustrated in Figure DIO1.2. Signals E0 through E3 (pins 9, 10, 11 and 14) are the state control signals for the encoder. PRE (U331 pin 14) is the preamble to be output over the interface. The dsp serial output bit clock is labeled SO_BCK and comes from U331 pin 15. This is gated on for 24 clock cycles to clock the data out of the processor. The word clock for the processor is labeled SO_SYNC and comes from U331 pin 16. The processor outputs data bits (SO_DATA), the validity bit (SO_VAL), the status bit (SO_STAT) and the user bit (SO_USER). These bits are combined and bi-phase encoded to produce the output signal at pin 19 of U431. In units manufactured before January 1991 this signal is balanced by U401 and coupled through transformer X210 to the output jack via P11B. In units manufactured after January 1991, the signal from pin 19 of U431 is labeled DDI_OUT and coupled to the DDF-3 circuit board through J41 pin 3.

Block sync is generated every 192 pairs of data words by U441 and a registered AND gate in U431. This block sync output appears on U431 pin 16 and shifts the address of U331 to generate the appropriate preamble for the block sync. This signal (SOBLK) also drives an input of the processor to signal that the start of a new status bit block has begun.

AES/EBU Interface Processor <5>

The dsp processor U651 accepts the serial data and bit flags from the AES/EBU receive input. It performs appropriate checking of those bits and sends the result to the main dsp for processing. It also accepts the AES/EBU data from the main processor and supplies the signals needed for the transmitter circuitry.

Part of U261 is used as an interrupt selector for the AES/EBU processor. The external interrupts may come from the parallel ports or from a flag input (/OPTFLAG) created by U351. The choice of interrupt sources is selected by IRQ0 from U461. U261 combines the flag input with the buffered address line BA1 to create two flag inputs, depending on the address written to U351. The /OPTRST signal, causes U261 to tri-state its outputs when asserted low. When this occurs the interrupt inputs are driven through resistors R1601 and R2606 from the MODE0 and MODE1 bits. The processor latches the levels on its interrupt inputs as it exits reset and uses the two bit value to select the memory map and reset vector. This allows the host computer to control the memory mode of the processor as it exits reset.

House Sync Receiver <6>

The signal from the rear panel enters the board via P88. It is coupled through transformer X87 into differential line receiver U861. The output of this gate is a ground referenced AES/EBU signal. Programmable logic device U151 detects the sync preambles on the signal to provide a reference signal for the phase lock loop. There are two sync detector circuits inside U151, one is used for 32 kHz and the other for 44.1 kHz and 48 kHz sample rates. Pin 21 of U151 goes low whenever the 32 kHz sync detector finds a sync preamble. The combination of R3401, D3403 and C3401 senses this and holds pin 5 of U151 low if syncs are detected. The output on pin 20 will then be the output of the 32 kHz sync detector. If no syncs are detected pin 5 will go high and the 44.1kHz/48kHz detector will be enabled. The output on pin 20 will then be the output of the 44.1kHz/48kHz detector. Since preambles occur at the beginning of each channel of data the signal at the output of U151 is twice the audio sample rate.

The AES/EBU signal is also fed to a delay circuit consisting of R1306, C1306, U131, R1305 and C1305. The delayed signal drives an exclusive-OR edge detector consisting of R1704, C1702 and part of U363. Its output is used to re-clock the sync preamble detection pulse in flip-flop U361. A high frequency clock at 256 times the audio sample rate is generated by a phase lock loop consisting of U162, U241 and the associated components. The phase lock loop U162 contains a phase detector, VCO and lock detect circuit. The re-clocked output of the sync detector from U361 drives the pin 14 input of the phase detector. The reference input (pin 3) of the phase detector comes from the divide-by-128 output of the counter. The VCO center frequency and tuning range is determined by C1604, R1702 and R1703. The phase detector output is filtered by R1603, R1605 and C1602 to produce the loop control voltage into the VCO. The loop will seek a point at which the

VCO output frequency is correct to produce equal input frequencies at the two phase detector inputs.

The house sync may also operate with a TTL squarewave instead of an AES/EBU input as a reference signal. In this mode pin 8 of U151 (TTL) is driven high, changing the logic of the sync detector. In the TTL mode the sync detection logic is bypassed and the input signal appears on pin 20 of U151. This is re-clocked by the flip-flop U361 and a delayed replica of the reference input appears at the phase comparator input. The phase lock loop is designed to lock onto a reference signal of twice the desired audio sample rate, requiring a 96 kHz reference input for a 48 kHz sample rate output.

Front Panel I/O without Optical <7a>

Schematic <7a> applies only to those units manufactured before January 1991, which have not been modified with a retrofit kit. U401 converts the unbalanced output signal to a balanced format and receives the balanced input and converts it to an unbalanced form. X310 and X210 provide additional ground loop rejection and isolation. Resistors are used to terminate the AES/EBU input with 240 Ohms and terminate the SPDIF input with 75 Ohms. The voltage of an AES/EBU output is 5 V behind a 120 Ohms output impedance. The SPDIF output is attenuated to provide 0.5 V from 75 Ohms when correctly terminated. The capacitors block dc from appearing across the transformers or attenuator resistors.

Front Panel I/O with Optical <7b>

The Digital I/O connector front panel assembly includes a small circuit board called the DDI-3. Circuits on the DDI3 board buffer the AES/EBU, SPDIF and optical EIAJ signals individually.

The AES/EBU input enters on connector J151, through dc blocking capacitor C151 to transformer X141. The input impedance is switchable by S151 between 120 Ohms and 10k Ohms to allow bridging operation. The transformer output is converted to unbalanced operation and buffered by U141A. The SPDIF input enters on J131 and is terminated by R131. U131A acts as a buffer amplifier to boost the incoming 0.5 V signal. U131B and U131C create a Schmitt trigger buffer which squares the input into a proper logic signal. U101 converts the optical input to an electrical signal.

The three input signals drive multiplexer U111 and edge detectors formed by U121B, U121C and U121D. The edge detectors sense the presence of signal and store this information in peak detectors. The multiplexer uses these three signal present indications to decide which input signal to pass to the output. If multiple inputs are present simultaneously the AES/EBU signal has the highest priority, followed by optical input. U131F overrides the input selection and forces the AES/EBU output signal (U111 pin 12) to be looped back for self test applications.

The AES/EBU output is balanced by U141 and isolated by transformer X143. Resistors R153 and R152 build out the impedance to approximately 110 Ohms. U121 drives the SPDIF output through X142. The attenuator formed by R122 and R121 drops the signal level to 0.5V at a source impedance of 75 Ohms. The optical conversion is provided by U102.

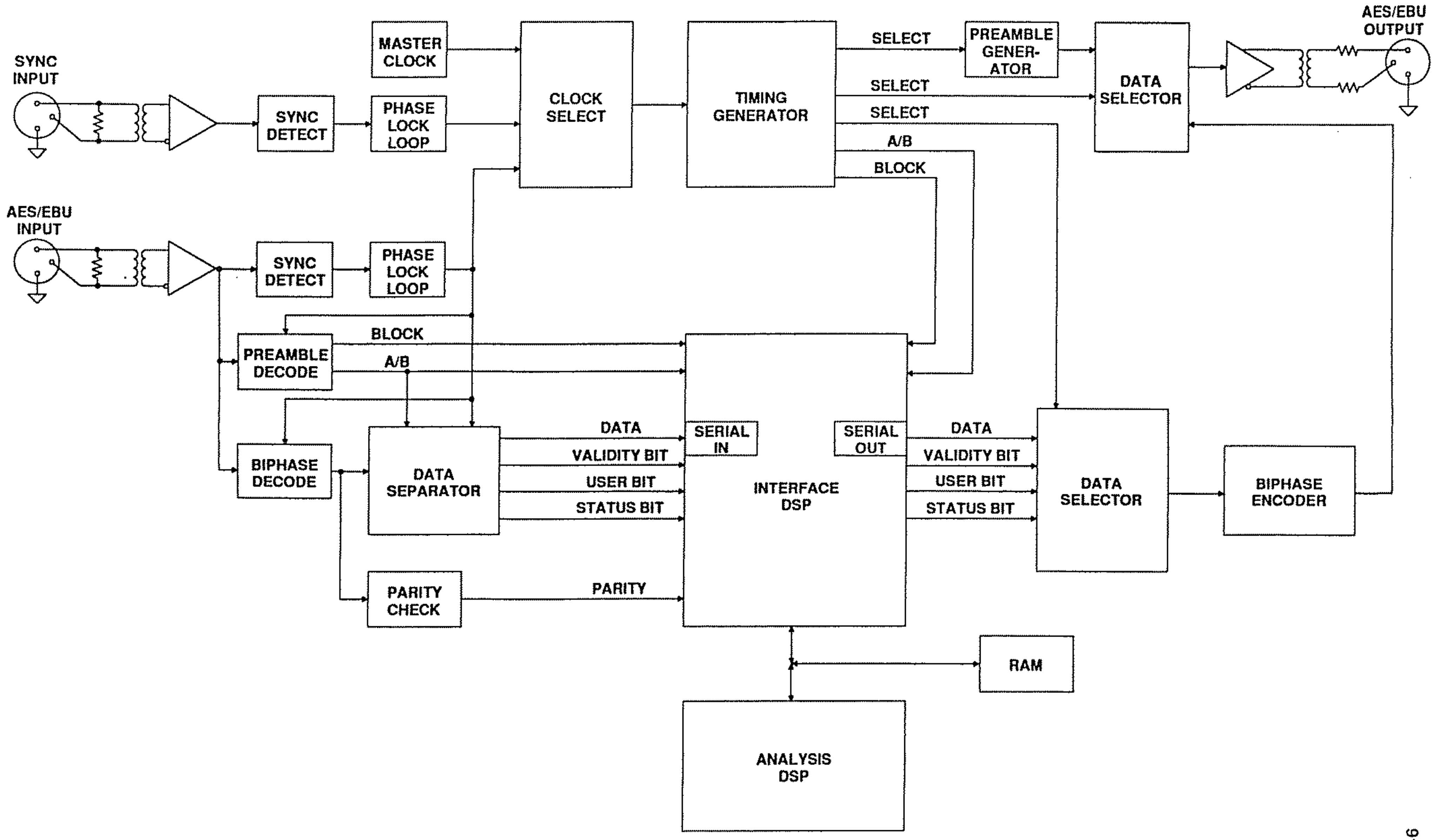


Figure DIO1.1 AES-EBU INTERFACE BLOCK DIAGRAM

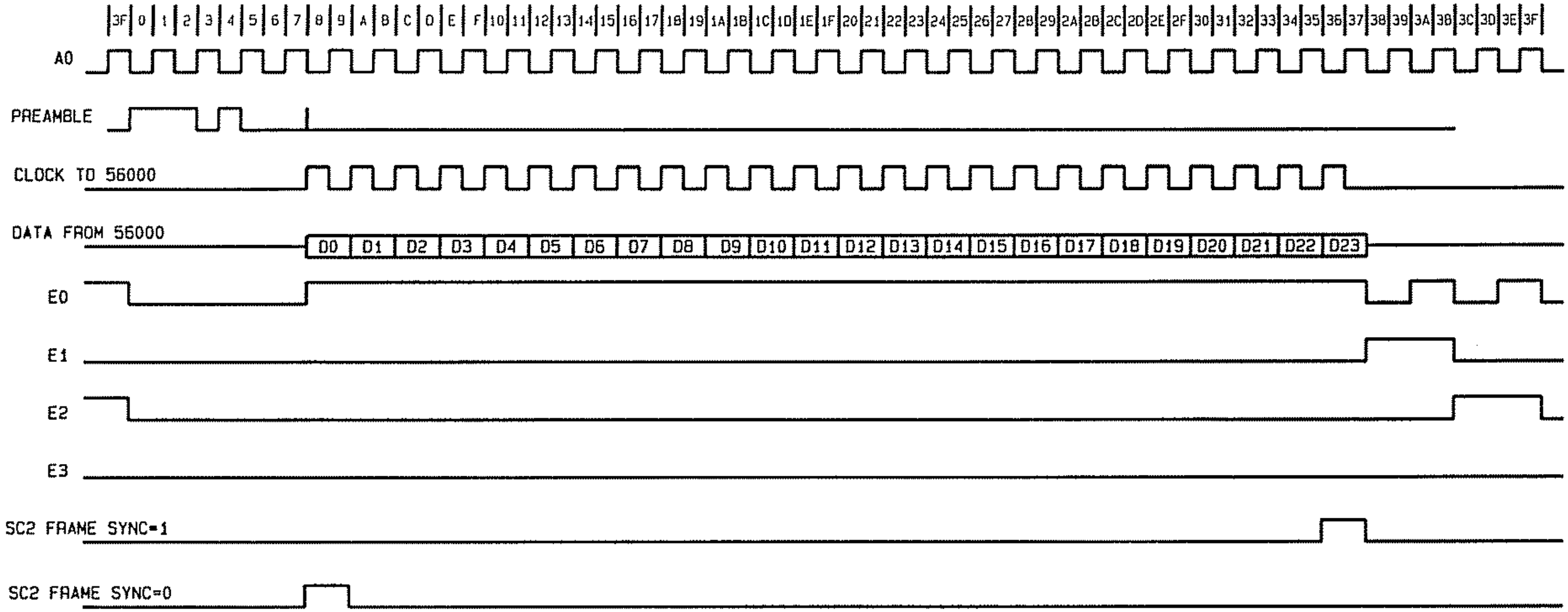


Figure DIO1.2 AES-EBU TRANSMITTER TIMING

AES/EBU INTERFACE SPECIFICATION

The AES digital interface specification was standardized in 1985. An essentially identical specification was promulgated by the EBU. It is a serial interface so as to require a minimum of wiring between devices. It provides for two channels of 20-bit or 24-bit digital audio data. These channels are referred to as A channel and B channel. The structure of the serial word is detailed in Figure DIO1.3. If 20-bit data is transmitted the remaining 4 bits may be used for an unspecified auxiliary signal.

The digital audio data is sent LSB first. If the full 24-bit data size is not used the lower bits must be zero filled to place the MSB in the same position. There are also three individual bits per channel. One is dedicated to a validity flag which indicates if the corresponding audio sample is a valid reliable audio sample or if it has been interpolated due to the correct data being unavailable. The second individual bit is called the user bit and is available for carrying any data the user cares to send in it. This provides a single bit per audio sample, requiring a series of samples to carry a complete message. The framing of this bit is undefined in the standard, making any uniform use of the bit impossible. The third bit is the channel status bit which conveys one bit of a 192-bit data "block". After every 192 pairs of audio samples the block is refreshed. The 192 bits are divided into 24 bytes, and the bytes are allocated to various functions.

The last bit is a parity check bit which serves to force an even number of transitions in the transmitted signal and allows a simple check for errors in the received data. The parity checking function can determine that an odd number of errors (1, 3, 5, etc) occurred in the data stream. An even number of errors will result in correct parity and therefore will not indicate bad data.

The complete signal comprises 28 data bits to which is added a preamble occupying as much time as 4 data bits to make a total of 32 bit times per channel. The serial signal is bi-phase encoded with a technique called "bi-phase mark encoding" (there are other forms of bi-phase encoding). The bi-phase mark encoding process provides a transition from high to low or low to high at every cell boundary. If the data is a "1" there will also be a transition at the center of the data cell. If the data bit is a "0" there will be no transition at the center of the cell. This process is diagrammed in Figure DIO1.4. The advantage of this technique is that there is always a transition at a data cell boundary. This allows clock recovery circuits in the receiver to sense these edges to determine the start of each data cell. Since the information is contained in the timing of the transitions, not their direction, the resulting signal is polarity insensitive. If the signal is inverted there will be no change in the meaning of the data. This encoding also reduces the low frequency content in the signal, eliminating dc and allowing ac coupling.

The preamble added to the start of the 28 data bits occupies a time period equivalent to that of 4 data bits. However, the preambles violate the bi-phase mark encoding rules by not necessarily having a transition at each cell boundary. There are three preambles defined in the standard; one for the B channel data words, one for normal A channel data words, and one which replaces the A channel sync every 192 pairs of data words to establish block sync of the channel status data. These preambles are illustrated in Figure DIO1.5. There are two versions shown for each, the appropriate one depends on the polarity of the signal on the line.

To understand the interface timings, consider the high or low pulse widths encountered at each of the three standard sample rates. Data bits are one of two widths, depending on whether they are a 1 or a 0. The sync pattern contains a wider high and low level, equivalent in width to three data 1 pulses.

Rate	"1" Width	"0" Width	Sync Width
48 kHz	163 ns	326 ns	488 ns
44.1 kHz	177 ns	354 ns	531 ns
32 kHz	244 ns	488 ns	732 ns

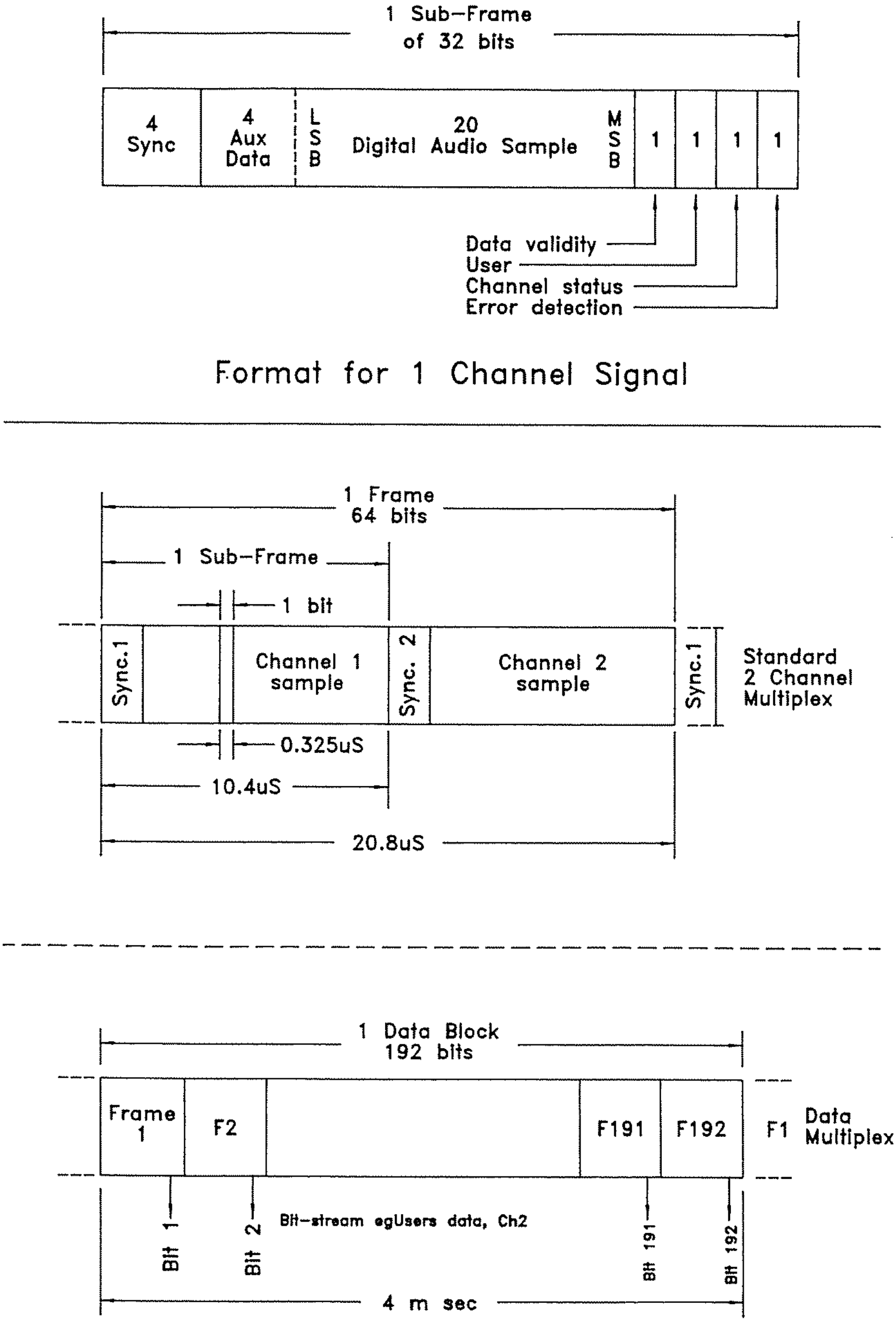
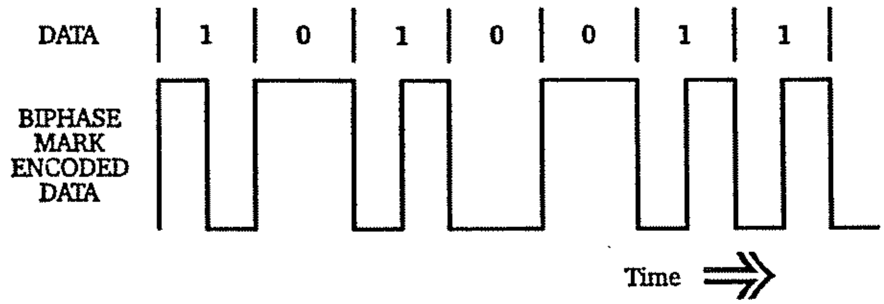


Figure DIO1.3 AES-EBU BIT STRUCTURE

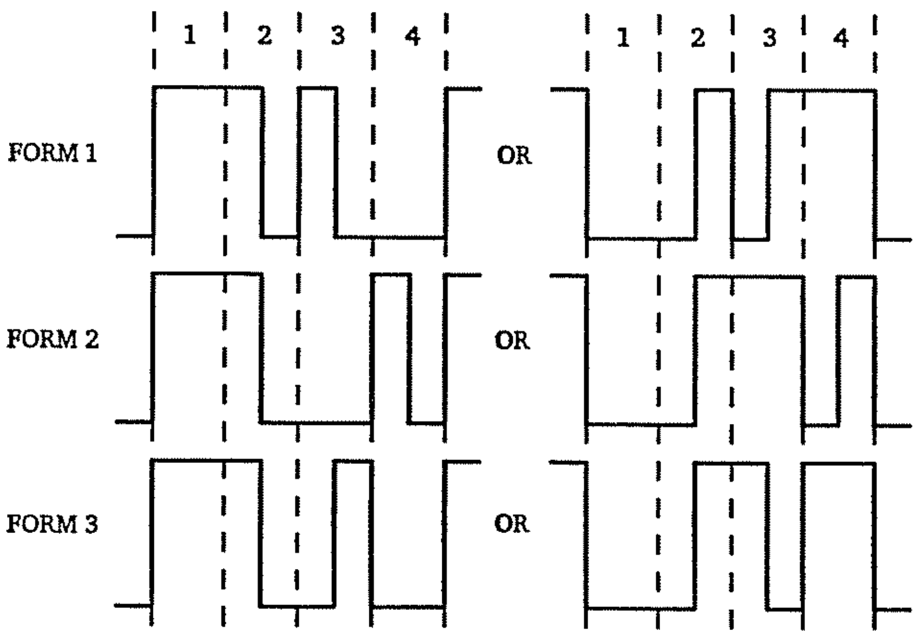


Biphase Mark always transitions at beginning of interval.

Logical 1 encodes a transition in the center of the data bit.

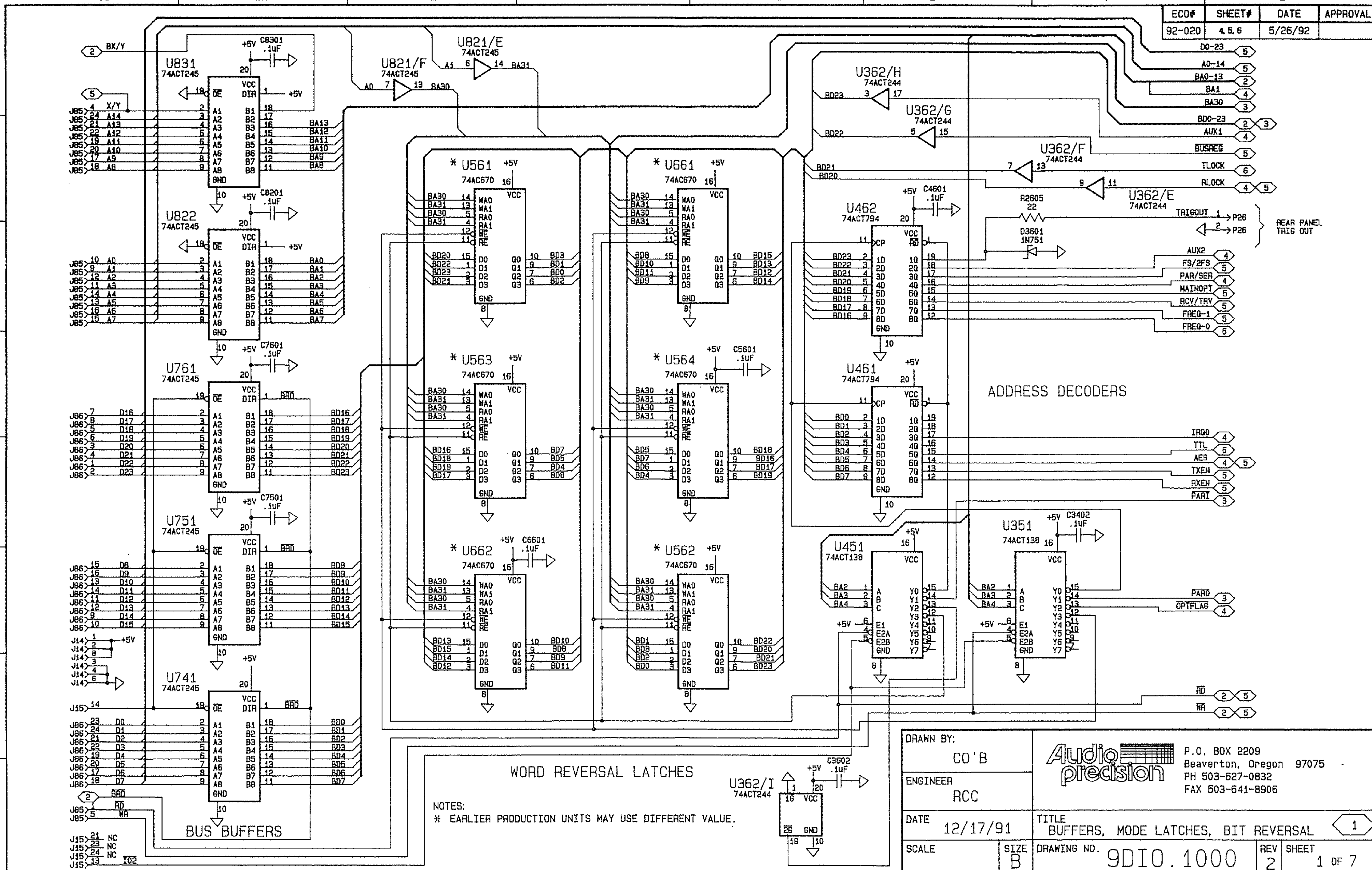
Logical 0 has no transition in the center of the data bit.

Figure DIO1.4 BIPHASE ENCODING

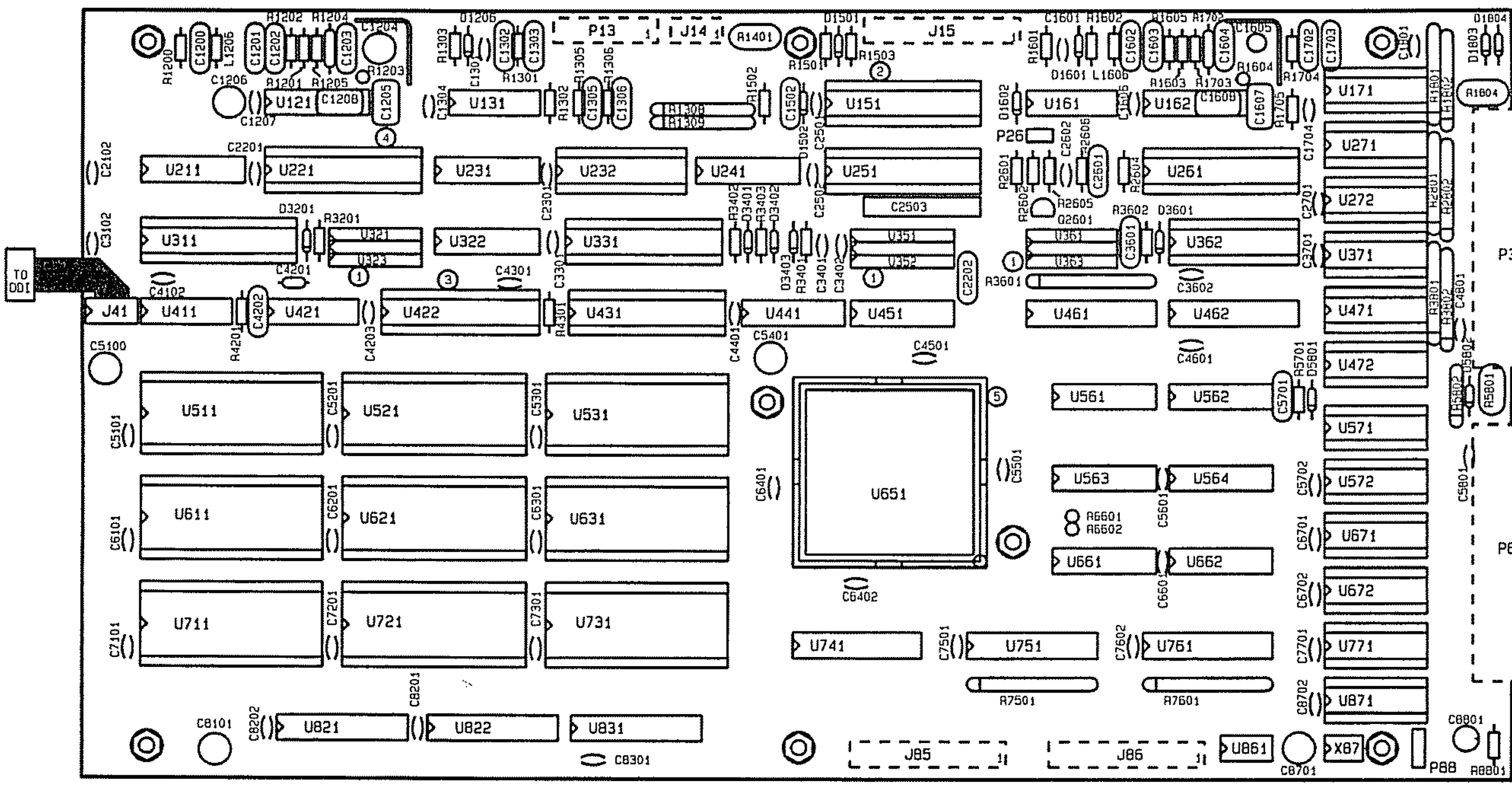


Preamble forms. The three types of sample preamble used are (1) channel A, subframe, and block synchronizing; (2) channel A, otherwise; and (3) channel B.

Figure DIO1.5 AES SYNCHRONIZATION



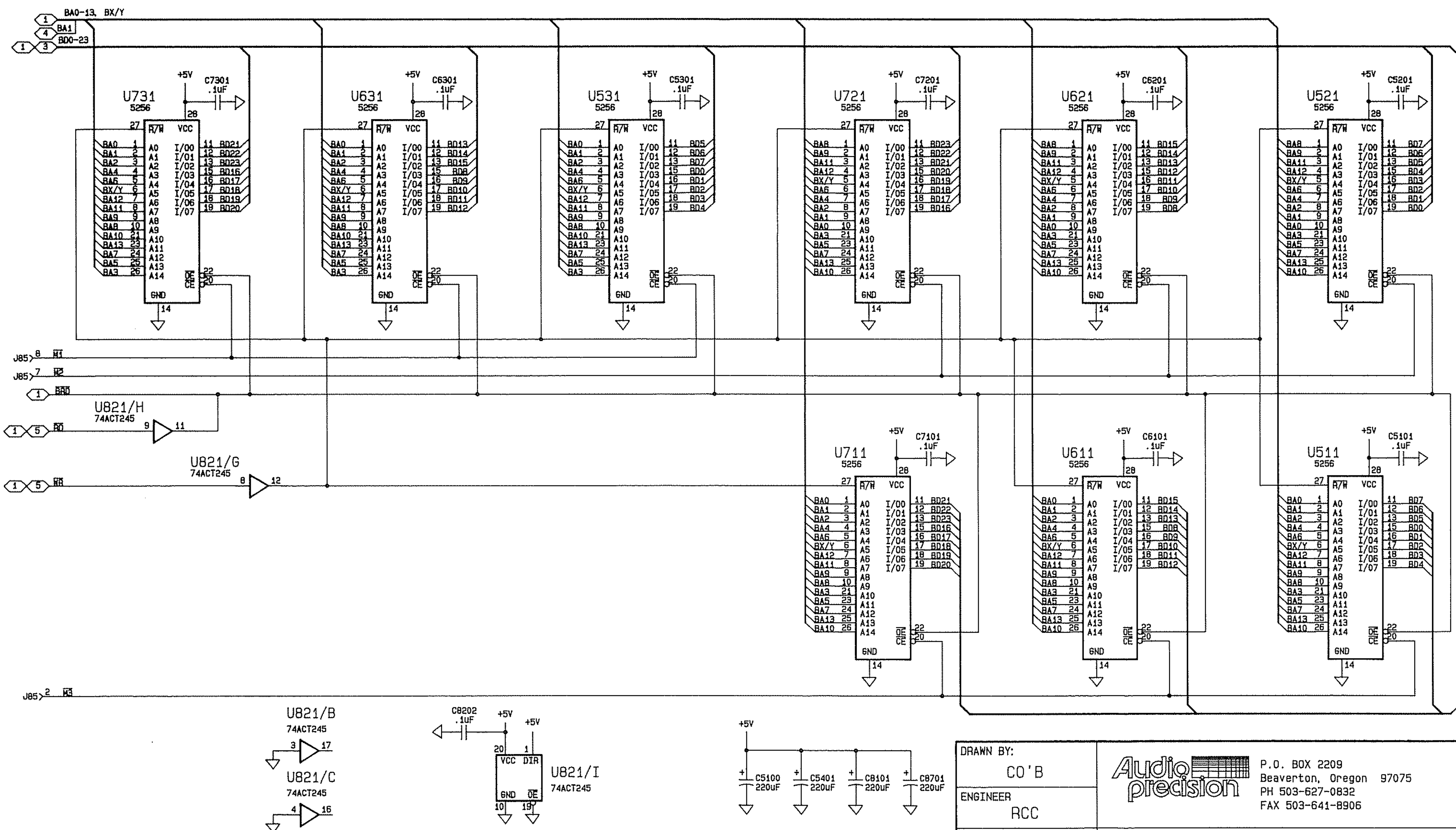
FILE: DIO1.SCH



DIGITAL INPUT/OUTPUT OPTION 9DIO.1000 (6400.DIO1.2)

NOTES:

1. U323, U352, U363 are mounted on top of U321, U351, U361.
2. R1504, R1505 are mounted under U151 on solderside.
3. R4202, R4203 are mounted under U422 on solderside.
4. R2202 is mounted under U221 on solderside.
5. R6501 R6502 are mounted under U651 on solderside.



DRAWN BY: CO'B

ENGINEER: RCC

DATE: 12/17/91

SCALE:

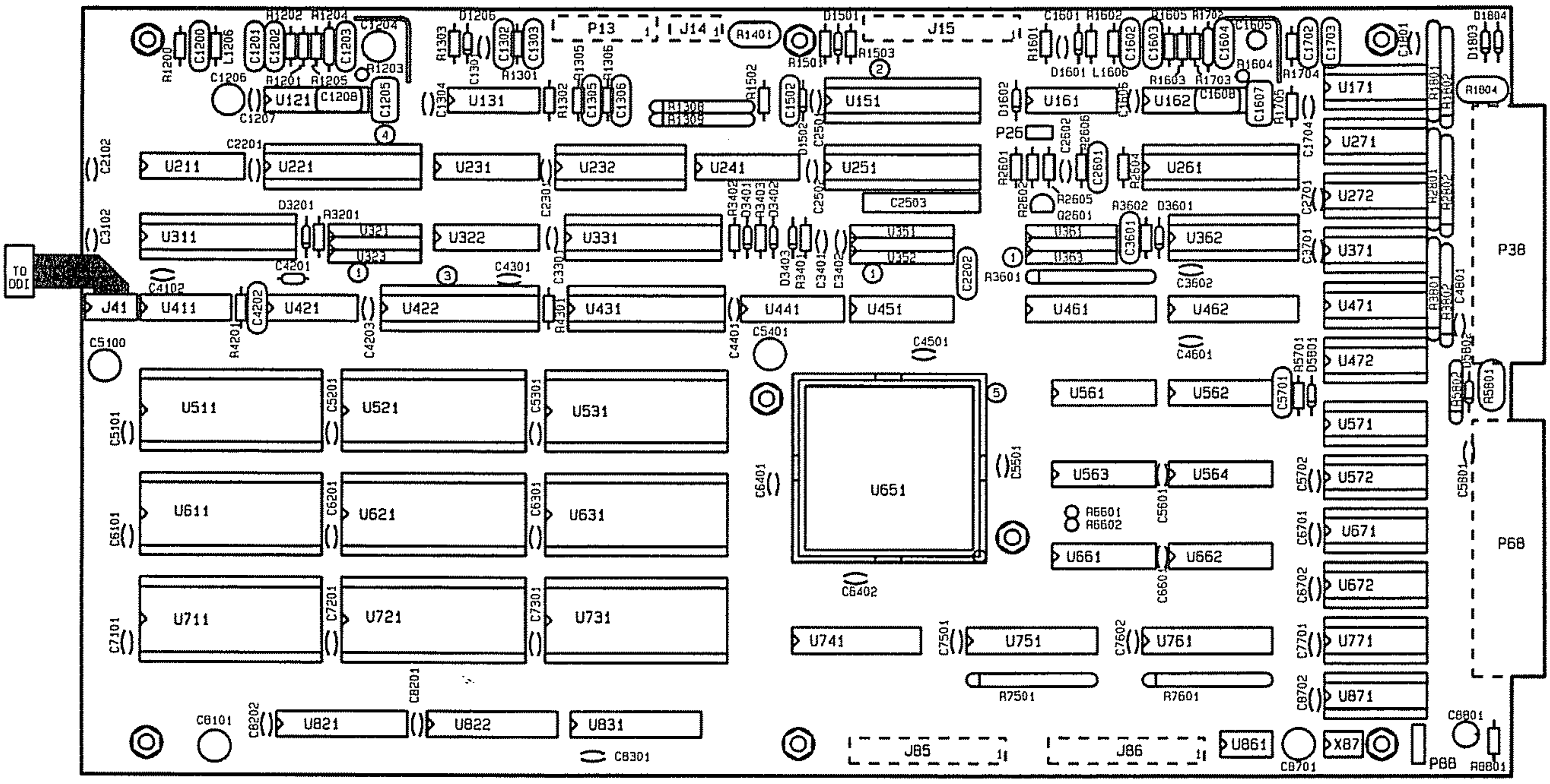
SIZE: B

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

TITLE: DATA MEMORY

DRAWING NO. 9DIO.1000 REV 2 SHEET 2 OF 7

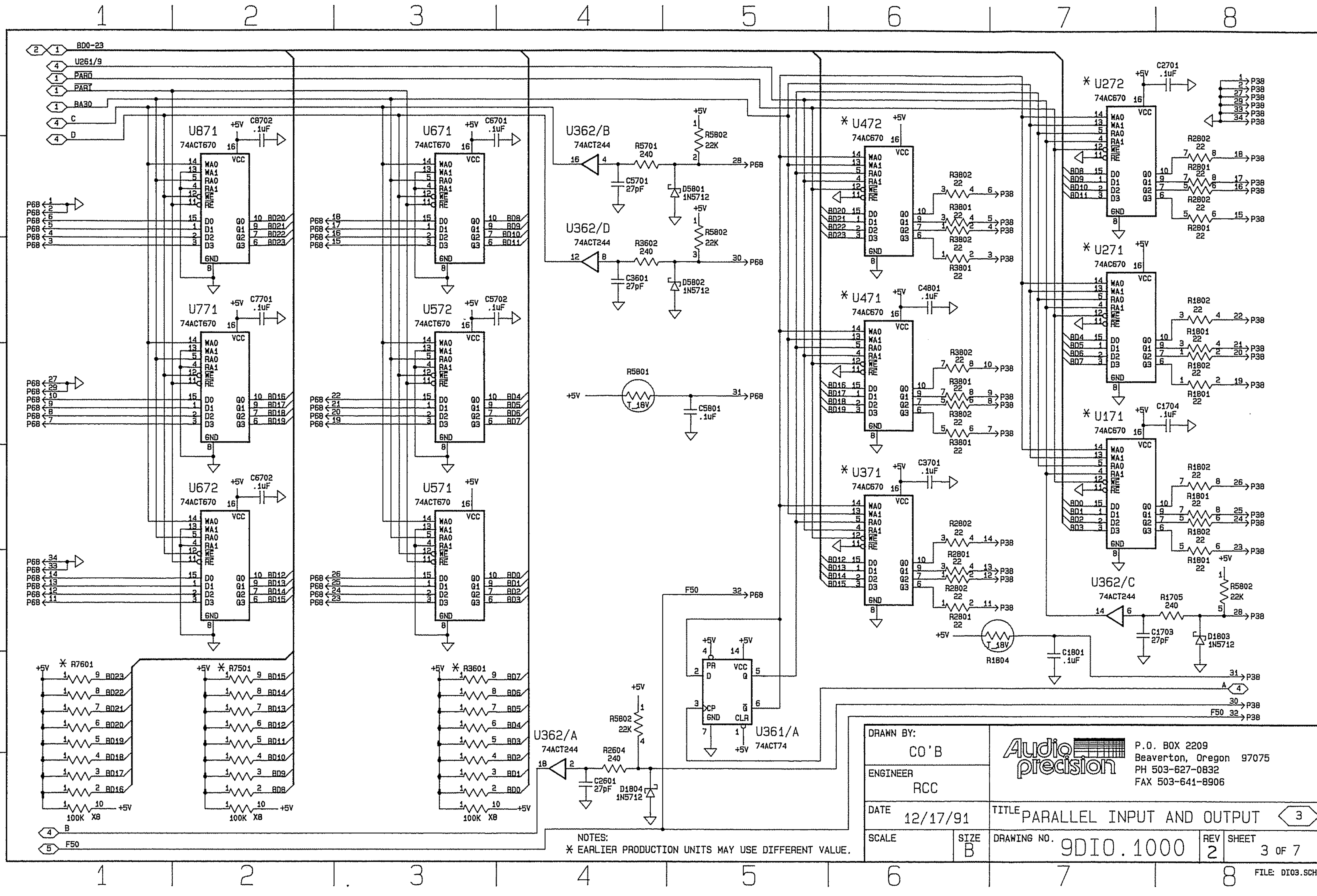
FILE: DIO2.SCH

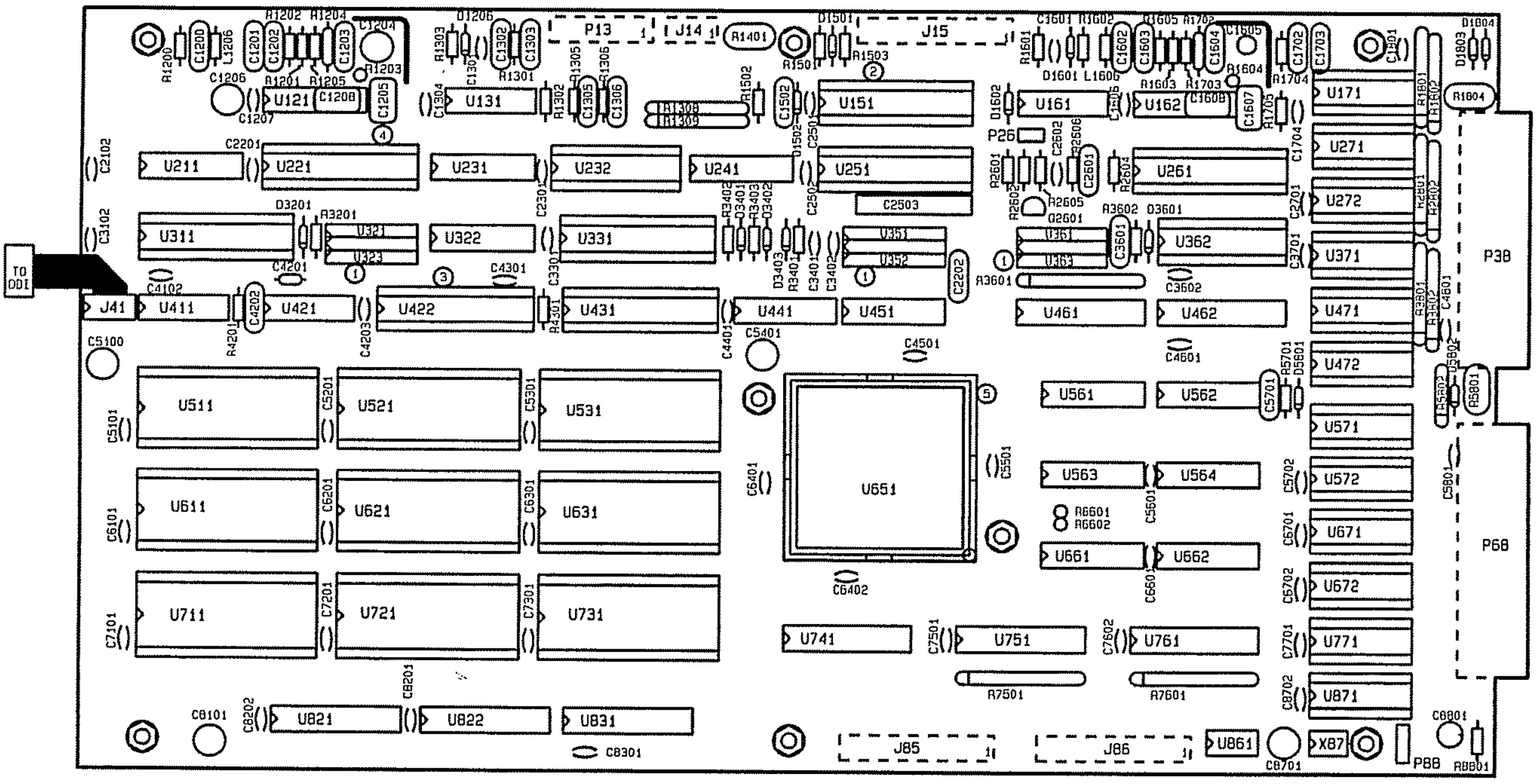


DIGITAL INPUT/OUTPUT OPTION 9DIO.1000 (6400.DIO1.2)

NOTES:

1. U323, U352, U363 are mounted on top of U321, U351, U361.
2. R1504, R1505 are mounted under U151 on solderside.
3. R4202, R4203 are mounted under U422 on solderside.
4. R2202 is mounted under U221 on solderside.
5. R6501 R6502 are mounted under U651 on solderside.

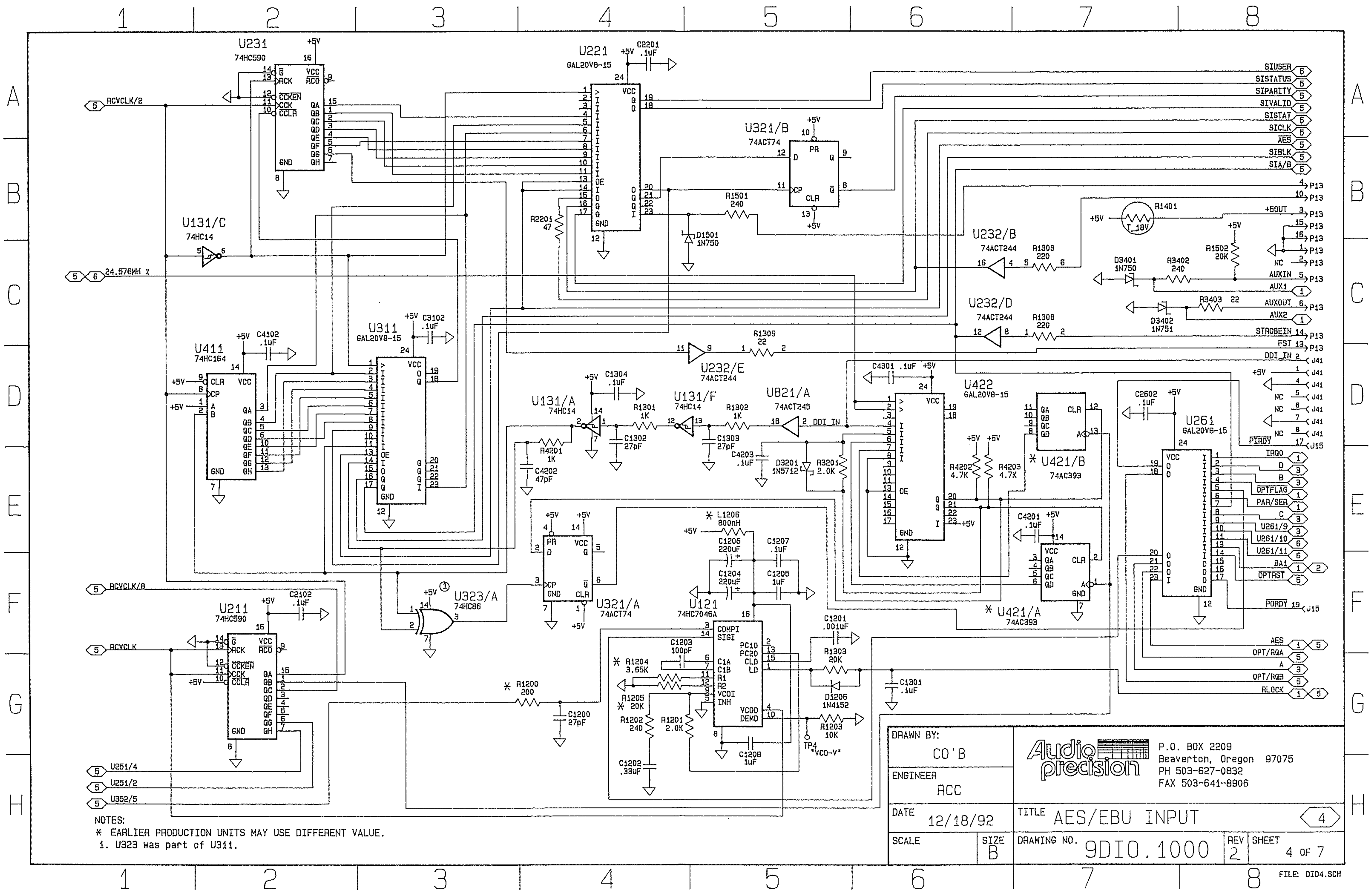

U871 74ACT670
U671 74ACT670
U771 74ACT670
U572 74ACT670
U672 74ACT670
U571 74ACT670
U362/B 74ACT244
U362/D 74ACT244
U362/A 74ACT244
U362/C 74ACT244
* U472 74AC670
* U471 74AC670
* U371 74AC670
* U272 74AC670
* U271 74AC670
* U171 74AC670
U361/A 74ACT74
BD0-23
U261/9
PAR0
PAR1
BA30
* R7601
* R7501
* R3601
100K X8
R5801
R1804
DRAWN BY: CO'B
ENGINEER RCC
DATE 12/17/91
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
TITLE PARALLEL INPUT AND OUTPUT
SCALE
SIZE B
DRAWING NO. 9DIO.1000
REV 2
SHEET 3 OF 7
NOTES:
* EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUE.
FILE: DIO3.SCH



NOTES:

1. U323, U352, U363 are mounted on top of U321, U351, U361.
2. R1504, R1505 are mounted under U151 on solderside.
3. R4202, R4203 are mounted under U422 on solderside.
4. R2202 is mounted under U221 on solderside.
5. R6501 R6502 are mounted under U651 on solderside.

DIGITAL INPUT/OUTPUT OPTION 9DIO.1000 (6400.DIO1.2)



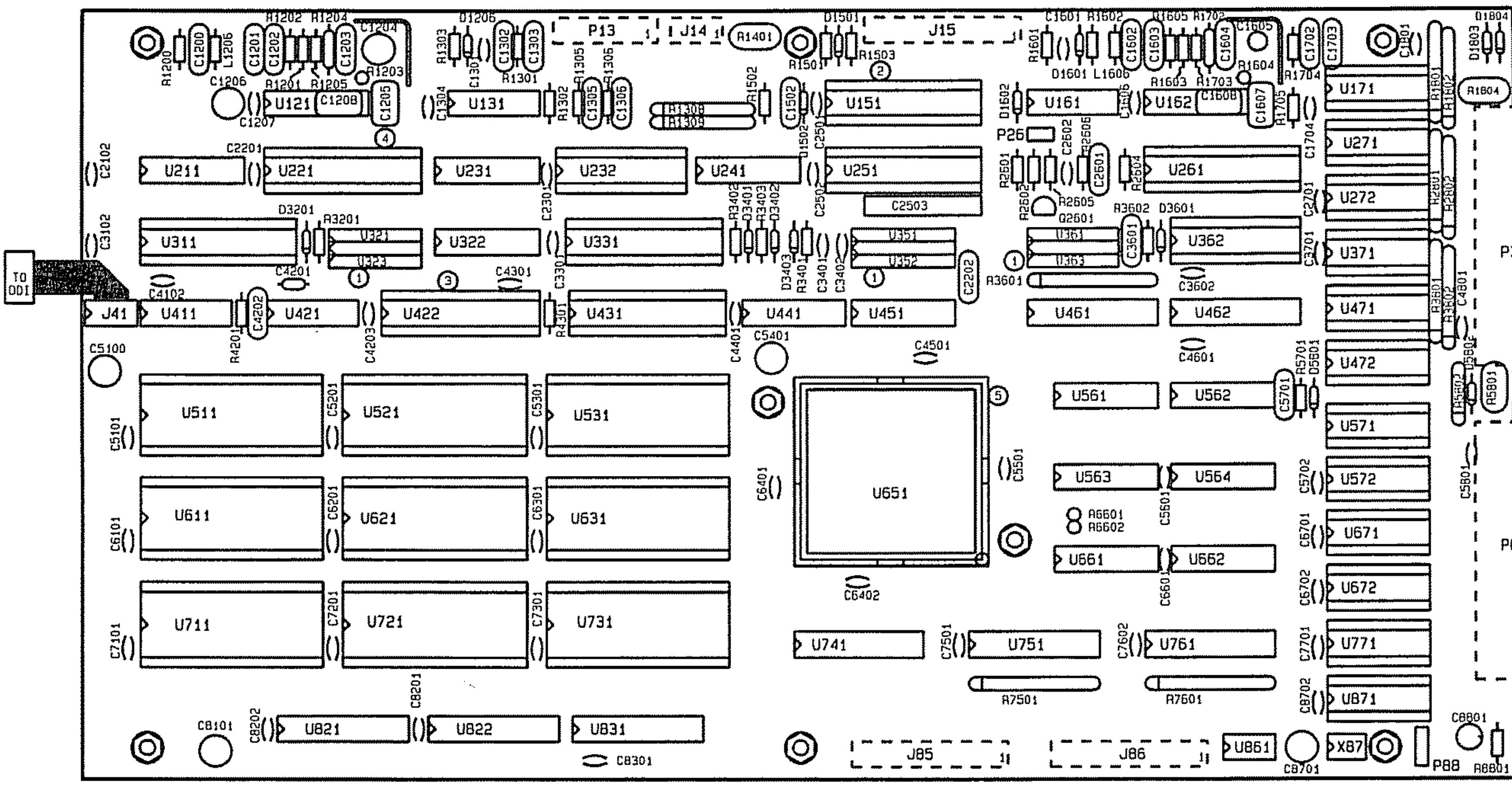
NOTES:

* EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUE.

1. U323 was part of U311.

DRAWN BY: CO'B	Audio precision	P.O. BOX 2209 Beaverton, Oregon 97075 PH 503-627-0832 FAX 503-641-8906	
ENGINEER RCC			
DATE 12/18/92	TITLE AES/EBU INPUT		4
SCALE	SIZE B	DRAWING NO. 9DIO.1000	REV 2 / SHEET 4 OF 7

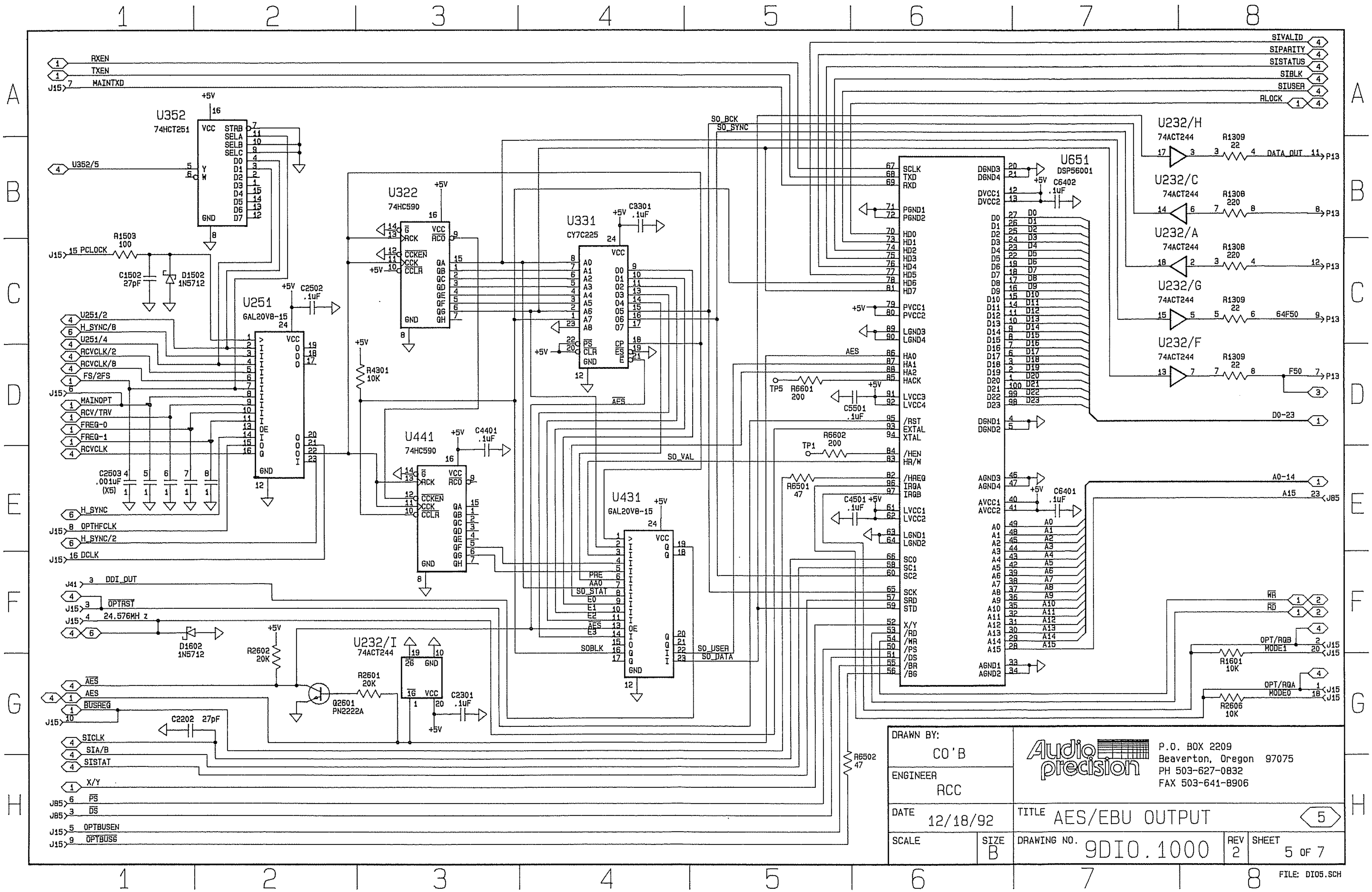
FILE: DIO4.SCH



DIGITAL INPUT/OUTPUT OPTION 9DIO.1000 (6400.DIO1.2)

NOTES:

1. U323, U352, U363 are mounted on top of U321, U351, U361.
2. R1504, R1505 are mounted under U151 on solderside.
3. R4202, R4203 are mounted under U422 on solderside.
4. R2202 is mounted under U221 on solderside.
5. R6501 R6502 are mounted under U651 on solderside.



DRAWN BY: CO'B

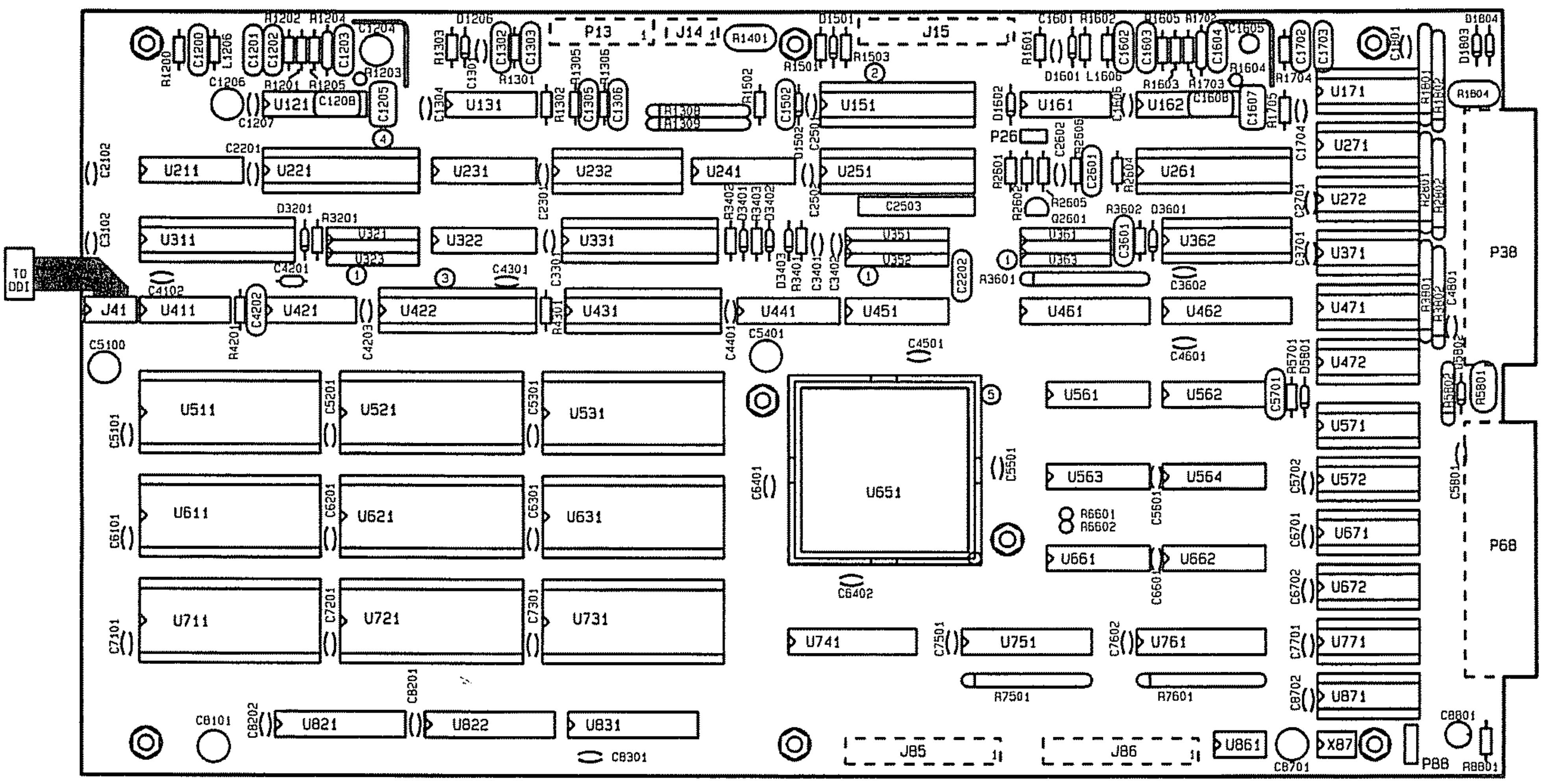
ENGINEER: RCC

DATE: 12/18/92

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

TITLE: AES/EBU OUTPUT

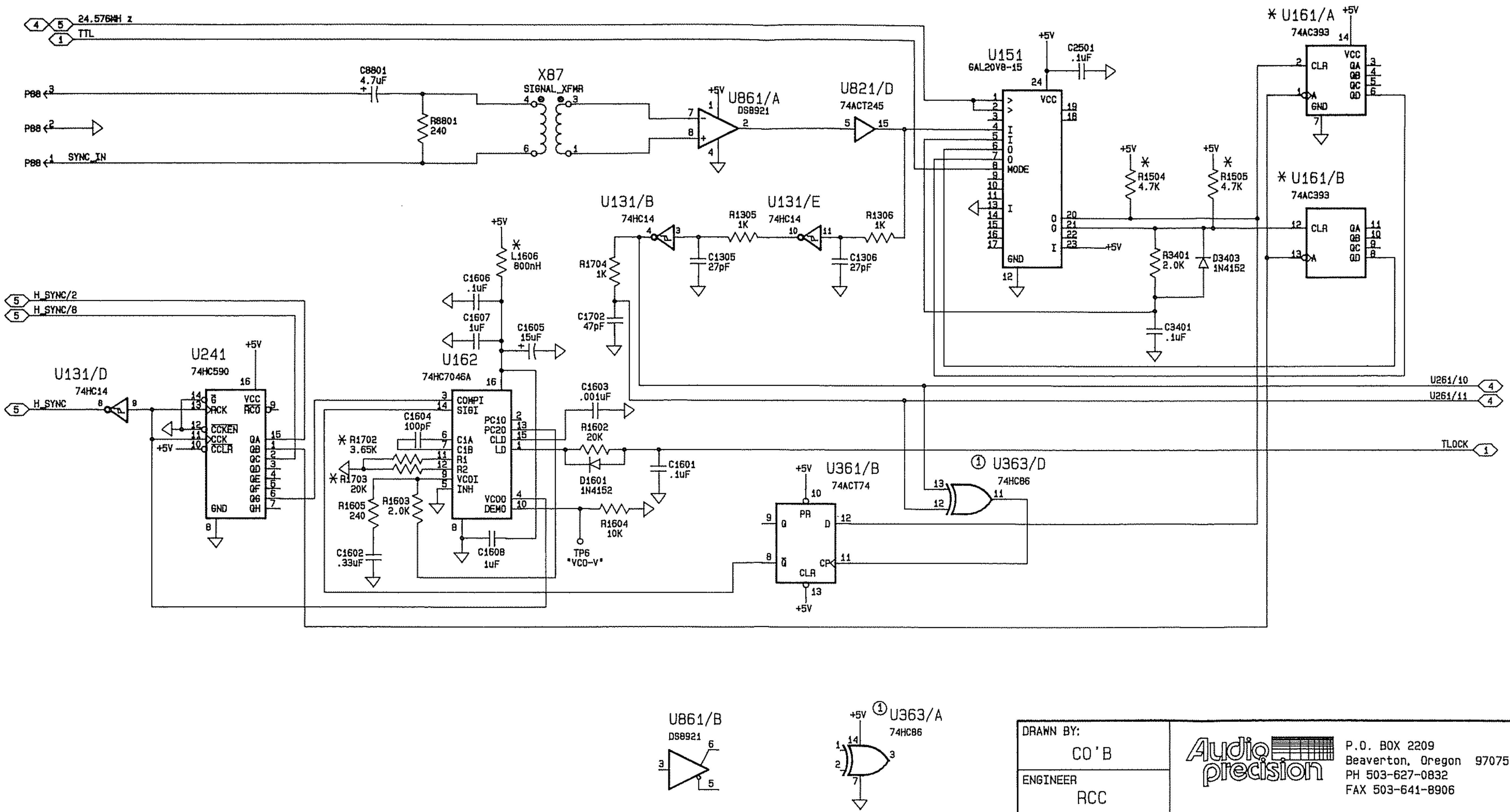
SCALE | SIZE: B | DRAWING NO. 9DIO.1000 | REV 2 | SHEET 5 OF 7



DIGITAL INPUT/OUTPUT OPTION 9DIO.1000 (6400.DIO1.2)

NOTES:

1. U323, U352, U363 are mounted on top of U321, U351, U361.
2. R1504, R1505 are mounted under U151 on solderside.
3. R4202, R4203 are mounted under U422 on solderside.
4. R2202 is mounted under U221 on solderside.
5. R6501 R6502 are mounted under U651 on solderside.

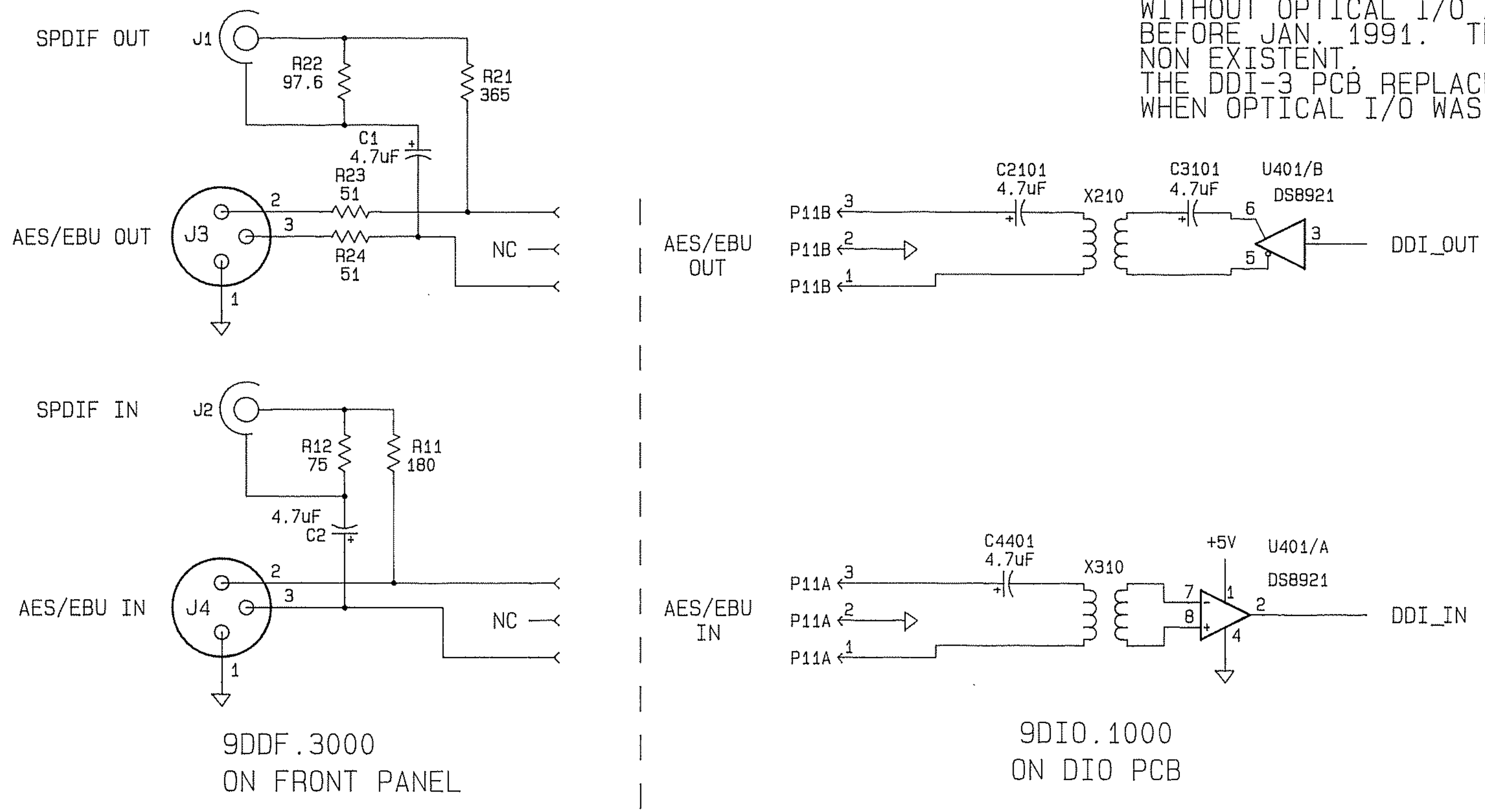


NOTES:
* EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUE.
1. U363/A was part of U261.

DRAWN BY: CO'B	
ENGINEER RCC	
DATE 6/1/92	TITLE EXTERNAL SYNC INPUT (6)
SCALE	SIZE B
DRAWING NO. 9DIO.1000	REV 2
SHEET 6 OF 7	

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

FILE: DIO6.SCH



NOTE:
THIS CIRCUITRY IS INCLUDED IN UNITS WITHOUT OPTICAL I/O AND MANUFACTURED BEFORE JAN. 1991. THE DDI-3 PCB IS NON EXISTENT.
THE DDI-3 PCB REPLACED THIS CIRCUITRY WHEN OPTICAL I/O WAS INTRODUCED.

(UNITS MANUFACTURED BEFORE JANUARY 1991)

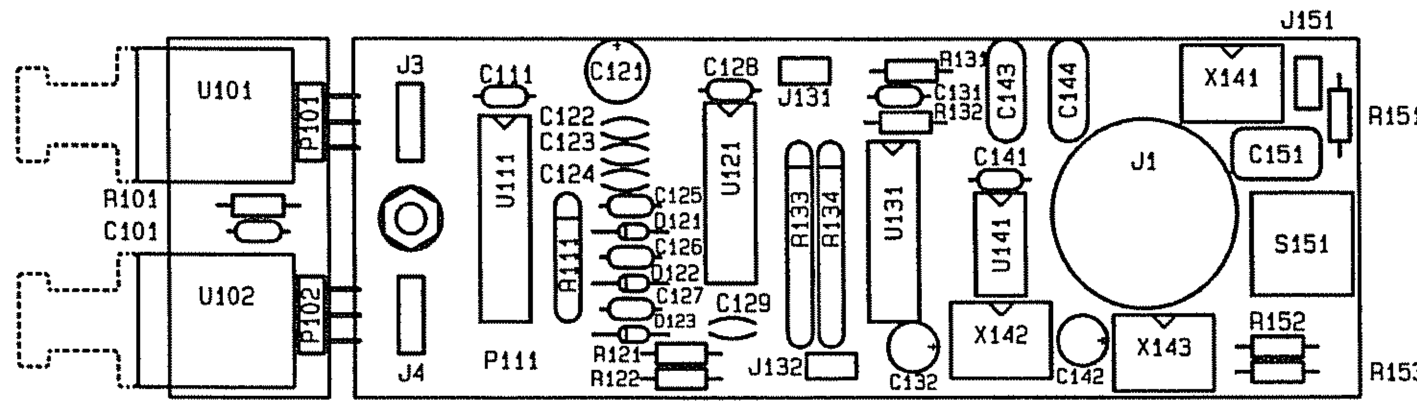
ECO#	SHEET#	DATE	APPROVAL

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

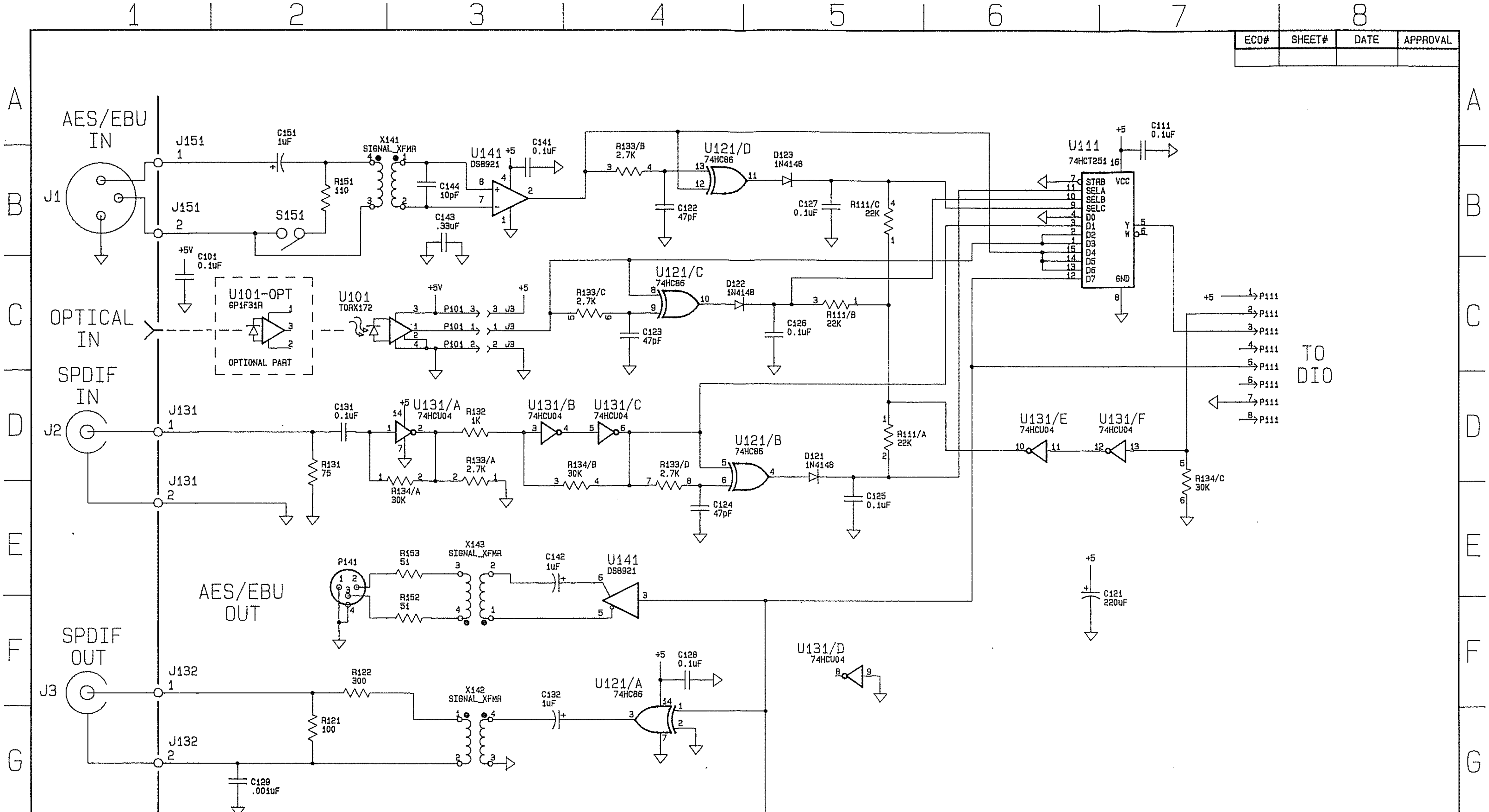
DATE 12/19/91 | TITLE DIO DUAL DOMAIN I/O | 7a

SCALE | SIZE B | DRAWING NO. 9DDF.3000 | REV 1 | SHEET 7a OF 7

FILE: DDF.SCH



DUAL DOMAIN INTERFACE 9DDI.3000 (6200.DDI3.3)



Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 12/19/91

TITLE DIO DUAL DOMAIN I/O 7b

SCALE SIZE B

DRAWING NO. 9DDI.3000

REV 3

SHEET 7b OF 7

FILE: DDI3-3.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1200	4G4	2294.0270	CAP MICA 500V 5%	27pF
C1201	4F5	2172.0102	CAP CERAM 100V 20%	.001uF
C1202	4H4	2454.0334	CAP POLYE 50V 5%	.33uF
C1203	4G4	2296.0101	CAP MICA 500V 1%	100pF
C1204	4F5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1205	4F5	2454.0105	CAP POLYE 50V 5%	1uF
C1206	4F5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1207	4F5	2172.0104	CAP CERAM 100V 20%	.1uF
C1208	4G5	454.0105	CAP POLYE 50V 5%	1uF
C1301	4G6	2172.0104	CAP CERAM 100V 20%	.1uF
C1302	4D4	2294.0270	CAP MICA 500V 5%	27pF
C1303	4D5	2294.0270	CAP MICA 500V 5%	27pF
C1304	4D4	2172.0104	CAP CERAM 100V 20%	.1uF
C1305	6D4	2294.0270	CAP MICA 500V 5%	27pF
C1306	6D5	2294.0270	CAP MICA 500V 5%	27pF
C1502	5C1	2294.0270	CAP MICA 500V 5%	27pF
C1601	6E4	2172.0104	CAP CERAM 100V 20%	.1uF
C1602	6F2	2454.0334	CAP POLYE 50V 5%	.33uF
C1603	6E4	2172.0102	CAP CERAM 100V 20%	.001uF
C1604	6E3	2296.0101	CAP MICA 500V 1%	100pF
C1605	6D3	2832.0156	CAP TA-EL 25V 20%	15uF
C1606	6D3	2172.0104	CAP CERAM 100V 20%	.1uF
C1607	6D3	2454.0105	CAP POLYE 50V 5%	1uF
C1608	6F3	2454.0105	CAP POLYE 50V 5%	1uF
C1702	6D4	2294.0470	CAP MICA 500V 5%	47pF
C1703	3F7	2294.0270	CAP MICA 500V 5%	27pF
C1704	3D8	2172.0104	CAP CERAM 100V 20%	.1uF
C1801	3G7	2172.0104	CAP CERAM 100V 20%	.1uF
C2102	4F2	2172.0104	CAP CERAM 100V 20%	.1uF
C2201	4A4	2172.0104	CAP CERAM 100V 20%	.1uF
C2202	5G1	2294.0270	CAP MICA 500V 5%	27pF
C2301	5G3	2172.0104	CAP CERAM 100V 20%	.1uF
C2501	6B6	2172.0104	CAP CERAM 100V 20%	.1uF
C2502	5C2	2172.0104	CAP CERAM 100V 20%	.1uF
C2503	5E1,5E2	2051.8102	CAP CERNET SIP +80/-20%	.001uF
C2601	3H4	2294.0270	CAP MICA 500V 5%	27pF
C2602	4D7	2172.0104	CAP CERAM 100V 20%	.1uF
C2701	3A8	2172.0104	CAP CERAM 100V 20%	.1uF
C3101	4G6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3102	4C3	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	5B4	2172.0104	CAP CERAM 100V 20%	.1uF
C3401	6D6	2172.0104	CAP CERAM 100V 20%	.1uF
C3402	1E7	2172.0104	CAP CERAM 100V 20%	.1uF
C3601	3C4	2294.0270	CAP MICA 500V 5%	27pF
C3602	1H5	2172.0104	CAP CERAM 100V 20%	.1uF
C3701	3E6	2172.0104	CAP CERAM 100V 20%	.1uF
C4102	4C2	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	4E7	2172.0104	CAP CERAM 100V 20%	.1uF
C4202	4E4	2294.0470	CAP MICA 500V 5%	47pF
C4203	4E5	2172.0104	CAP CERAM 100V 20%	.1uF
C4301	4D6	172.0104	CAP CERAM 100V 20%	.1uF
C4401	5D3	2172.0104	CAP CERAM 100V 20%	.1uF

REPLACEABLE ELECTRICAL PARTS LIST: 9DIO.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C4501	5E5	2172.0104	CAP CERAM 100V 20%	.1uF
C4601	1B6	2172.0104	CAP CERAM 100V 20%	.1uF
C4801	3C6	2172.0104	CAP CERAM 100V 20%	.1uF
C5100	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5101	2E8	2172.0104	CAP CERAM 100V 20%	.1uF
C5201	2B8	2172.0104	CAP CERAM 100V 20%	.1uF
C5301	2B4	2172.0104	CAP CERAM 100V 20%	.1uF
C5401	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5501	5D5	2172.0104	CAP CERAM 100V 20%	.1uF
C5601	1D5	2172.0104	CAP CERAM 100V 20%	.1uF
C5701	3B4	2294.0270	CAP MICA 500V 5%	27pF
C5702	3C3	2172.0104	CAP CERAM 100V 20%	.1uF
C5801	3D5	2172.0104	CAP CERAM 100V 20%	.1uF
C6101	2E7	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	2B7	2172.0104	CAP CERAM 100V 20%	.1uF
C6301	2B3	2172.0104	CAP CERAM 100V 20%	.1uF
C6401	5E7	2172.0104	CAP CERAM 100V 20%	.1uF
C6402	5B7	2172.0104	CAP CERAM 100V 20%	.1uF
C6601	1F4	2172.0104	CAP CERAM 100V 20%	.1uF
C6701	3B3	2172.0104	CAP CERAM 100V 20%	.1uF
C6702	3E2	2172.0104	CAP CERAM 100V 20%	.1uF
C7101	2E6	2172.0104	CAP CERAM 100V 20%	.1uF
C7201	2B6	2172.0104	CAP CERAM 100V 20%	.1uF
C7301	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C7501	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C7601	1D2	2172.0104	CAP CERAM 100V 20%	.1uF
C7701	3C2	2172.0104	CAP CERAM 100V 20%	.1uF
C8101	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C8201	1B2	2172.0104	CAP CERAM 100V 20%	.1uF
C8202	2G3	2172.0104	CAP CERAM 100V 20%	.1uF
C8301	1A2	2172.0104	CAP CERAM 100V 20%	.1uF
C8701	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C8702	3A2	2172.0104	CAP CERAM 100V 20%	.1uF
C8801	6B2	2942.0475	CAP AL-EL 35V 20%	4.7uF
D1206	4G5	3110.4152	DIODE SIGNAL	4152
D1501	4C5	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D1502	5C1	3120.0000	DIODE SCHOTTKY	1SS97
D1601	6E4	3110.4152	DIODE SIGNAL	4152
D1602	5F1	3120.0000	DIODE SCHOTTKY	1SS97
D1803	3F8	3120.0000	DIODE SCHOTTKY	1SS97
D1804	3H4	3120.0000	DIODE SCHOTTKY	1SS97
D3201	4E5	3110.4152	DIODE SIGNAL	4152
D3401	4C7	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D3402	4C7	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D3403	6D7	3110.4152	DIODE SIGNAL	4152
D3601	1C6	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D5801	3B5	3120.0000	DIODE SCHOTTKY	1SS97
D5802	3C5	3120.0000	DIODE SCHOTTKY	1SS97
J14	1G1	4221.1008	JACK PC 2 X .1	8 PIN
J15	1G1,1H1,4D8,4F8,5A1-5H1,5G8	4221.1024	JACK PC 2 X .1	24 PIN

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
J41	4D8,5F1	4151.0905	CABLE ASSY 05RBN/DIP	9" 5 CND
J85	1A1-1C1,1H1,2D1,2G1,5E8	4221.1024	JACK PC 2 X .1	24 PIN
J86	1D1-1H1,5H1	4221.1024	JACK PC 2 X .1	24 PIN
L1206	4E5	4510.0801	INDUCTOR 10 OHM	800nH
L1606	6D3	4510.0801	INDUCTOR 10 OHM	800nH
P11		4221.0172	PLUG PC 90' 2X.1 X.39	72 PIN
P13	4B8-4D8,5B8-5D8	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P14		4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P15		4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P26	1C8	4221.0036	PLUG PC .1 X.43	36 PIN
P38	3A8-3G8	4221.0134	PLUG PC 90' SHROUDED	34 PIN
P68	3B1-3D1,3B5-3F5,3F1	4221.0134	PLUG PC 90' SHROUDED	34 PIN
P85		4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P86		4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P88	6B1,6C1	4221.0036	PLUG PC .1 X.43	36 PIN
Q2601	5G2	3211.2222	XSTR NPN TO92	PN2222A
R1200	4G4	1214.0201	RES 1/4W C FLM 5%	200
R1201	4G4	1214.0202	RES 1/4W C FLM 5%	2.0K
R1202	4G4	1214.0241	RES 1/4W C FLM 5%	240
R1203	4G5	1214.0103	RES 1/4W C FLM 5%	10K
R1204	4G4	1136.3651	RES 1/8W M FLM 1%	3.65K
R1205	4G4	1214.0203	RES 1/4W C FLM 5%	20K
R1301	4D4	1214.0102	RES 1/4W C FLM 5%	1K
R1302	4D5	1214.0102	RES 1/4W C FLM 5%	1K
R1303	4G5	1214.0203	RES 1/4W C FLM 5%	20K
R1305	6C4	1214.0102	RES 1/4W C FLM 5%	1K
R1306	6C5	214.0102	RES 1/4W C FLM 5%	1K
R1308	4C7,5B8,5C8	1984.4221	RES NET SIP 5% I	4 X 220
R1309	4D5,5B8-5D8	1984.4220	RES NET SIP 5% I	4 X 22
R1401	4B7	1061.0601	RES PTC CERAM 18V	600mA
R1501	4B5	1214.0241	RES 1/4W C FLM 5%	240
R1502	4C8	1214.0203	RES 1/4W C FLM 5%	20K
R1503	5C1	1214.0101	RES 1/4W C FLM 5%	100
R1504	6C6	1214.0472	RES 1/4W C FLM 5%	4.7K
R1505	6C7	1214.0472	RES 1/4W C FLM 5%	4.7K
R1601	5G8	1214.0103	RES 1/4W C FLM 5%	10K
R1602	6E4	1214.0203	RES 1/4W C FLM 5%	20K
R1603	6F3	1214.0202	RES 1/4W C FLM 5%	2.0K
R1604	6F4	1214.0103	RES 1/4W C FLM 5%	10K
R1605	6F2	1214.0241	RES 1/4W C FLM 5%	240
R1702	6E3	1136.3651	RES 1/8W M FLM 1%	3.65K
R1703	6E3	1214.0203	RES 1/4W C FLM 5%	20K
R1704	6D4	1214.0102	RES 1/4W C FLM 5%	1K
R1705	3F8	1214.0241	RES 1/4W C FLM 5%	240
R1801	3B8-3E8	1984.4220	RES NET SIP 5% I	4 X 22
R1802	3B8-3E8	1984.4220	RES NET SIP 5% I	4 X 22
R1804	3G7	1061.0601	RES PTC CERAM 18V	600mA
R2201	4C4	1214.0270	RES 1/4W C FLM 5%	27

REPLACEABLE ELECTRICAL PARTS LIST: 9DIO.1000

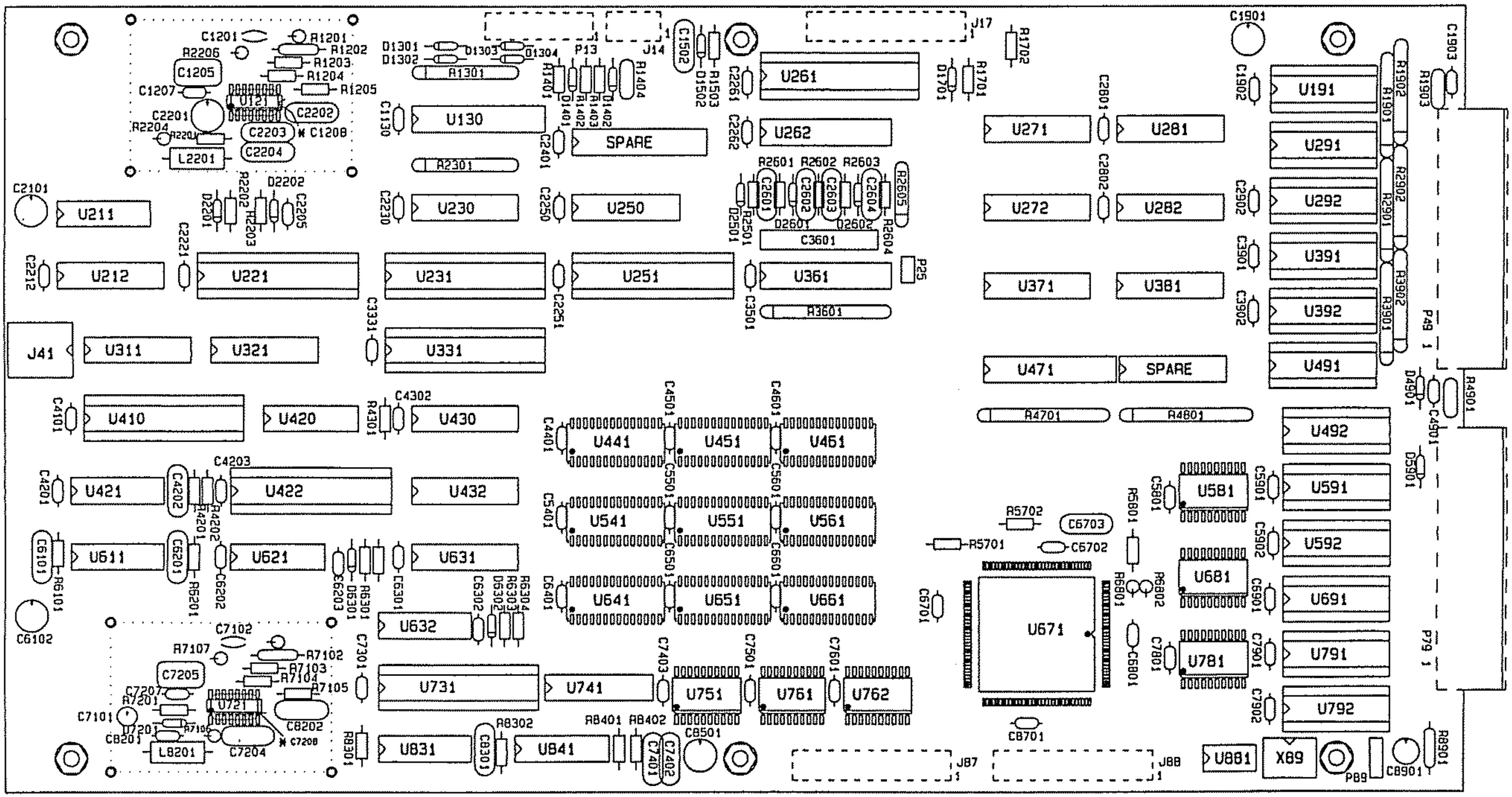
ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R2601	5G3	1214.0203	RES 1/4W C FLM 5%	20K
R2602	5G2	1214.0203	RES 1/4W C FLM 5%	20K
R2604	3H4	1214.0241	RES 1/4W C FLM 5%	240
R2605	1B6	1214.0220	RES 1/4W C FLM 5%	22
R2606	5G8	1214.0103	RES 1/4W C FLM 5%	10K
R2801	3B6-3F6	1984.4220	RES NET SIP 5% I	4 X 22
R2802	3B6-3F6	1984.4220	RES NET SIP 5% I	4 X 22
R3201	4E6	1214.0202	RES 1/4W C FLM 5%	2.0K
R3401	6D6	1214.0202	RES 1/4W C FLM 5%	2.0K
R3402	4C7	1214.0241	RES 1/4W C FLM 5%	240
R3403	4C8	1214.0220	RES 1/4W C FLM 5%	22
R3601	3G3,3H3	1984.9104	RES NET SIP 5% B	9 X 100K
R3602	3C4	1214.0241	RES 1/4W C FLM 5%	240
R3801	3B9,3E9	1984.4220	RES NET SIP 5% I	4 X 22
R3802	3B9,3C9	1984.4220	RES NET SIP 5% I	4 X 22
R4201	4E4	1214.0102	RES 1/4W C FLM 5%	1K
R4202	4E6	1214.0472	RES 1/4W C FLM 5%	4.7K
R4203	4E6	1214.0472	RES 1/4W C FLM 5%	4.7K
R4301	5D3	1214.0103	RES 1/4W C FLM 5%	10K
R5701	3B4	1214.0241	RES 1/4W C FLM 5%	240
R5801	3D4	1061.0601	RES PTC CERAM 18V	600mA
R5802	3B5,3G4	1985.4223	RES NET SIP 2% B	4 X 22K
R6501	5E5	1214.0470	RES 1/4W C FLM 5%	47
R6502	5H5	1214.0470	RES 1/4W C FLM 5%	47
R6601	5D5	1214.0201	RES 1/4W C FLM 5%	200
R6602	5D5	1214.0201	RES 1/4W C FLM 5%	200
R7501	3G2,3H2	1984.9104	RES NET SIP 5% B	9 X 100K
R7601	3G1,3H1	1984.9104	RES NET SIP 5% B	9 X 100K
R8801	6B3	1214.0241	RES 1/4W C FLM 5%	240
U121	4F5	3323.7046	PHASE LOCK LOOP	74HC7046A
U131	4C2,4D4,6D4,6D5	3323.0014	TRIGGER SCHMITT 8X	74HC14
U151	6B6	3342.20V8	GENERIC ARRAY	GAL20V8-15
U161	6C7,6B7	3326.0393	COUNTER 2X 4-BIT	74ACT393
U162	6D3	3323.7046	PHASE LOCK LOOP	74HC7046A
U171	3D7	3326.0670	REGISTER FILE 4X4	74AC670
U211	4F2	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U221	4A4	3342.20V8	GENERIC ARRAY	GAL20V8-15
U231	4A2	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U232	4C6,4D5,5A7-5D7,5F3	3326.0244	BUFFER 8X TRI-STATE	74ACT244
U241	6E2	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U251	5C2	3342.20V8	GENERIC ARRAY	GAL20V8-15
U261	4D8	3342.20V8	GENERIC ARRAY	GAL20V8-15
U271	3C7	3326.0670	REGISTER FILE 4X4	74AC670
U272	3A7	3326.0670	REGISTER FILE 4X4	74AC670
U311	4C3	3342.20V8	GENERIC ARRAY	GAL20V8-15
U321	4B5,4F4	3326.0074	FLIP-FLOP 2X D	74ACT74
U322	5B3	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U323	4F3	3323.0086	GATE 4-IN XOR	74HC86
U331	5B4	3723.7225	PROM CMOS 25ns	512 X 8
U351	1E6	3326.0138	DECODER 3-LN/8-LN	74ACT138
U352	5A1	3324.0251	MULTIPLEXER TRI-ST	74HCT251

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U361	3F5,6E5	3326.0074	FLIP-FLOP 2X D	74ACT74
U362	1A6,1B6,1H5,3B4,3C4,3F7,3H4	3326.0244	BUFFER 8X TRI-STATE	74ACT244
U363	6E5,6G5	3323.0086	GATE 4-IN XOR	74HC86
U371	3E6E8	3326.0670	REGISTER FILE 4X4	74AC670
U411	4D2	3323.0164	SHFT REG SERIAL-PARA	74HC164
U421	4D7,4F7	3326.0393	COUNTER 2X 4-BIT	74ACT393
U422	4D6	3342.20V8	GENERIC ARRAY	GAL20V8-15
U431	5E4	3342.20V8	GENERIC ARRAY	GAL20V8-15
U441	5E3	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U451	1F6	3326.0138	DECODER 3-LN/8-LN	74ACT138
U461	1D6	3326.0794	REGISTER 8X W/READBK	74ACT794
U462	1B6	3326.0794	REGISTER 8X W/READBK	74ACT794
U471	3C6	3326.0670	REGISTER FILE 4X4	74AC670
U472	3B6	3326.0670	REGISTER FILE 4X4	74AC670
U511	2E8	3722.5256.1	SRAM CMOS 85ns	32K X 8
U521	2B8	3722.5256.1	SRAM CMOS 85ns	32K X 8
U531	2B4	3722.5256.1	SRAM CMOS 85ns	32K X 8
U561	1B3	3326.0670	REGISTER FILE 4X4	74ACT670
U562	1F4	3326.0670	REGISTER FILE 4X4	74ACT670
U563	1D3	3326.0670	REGISTER FILE 4X4	74ACT670
U564	1D4	3326.0670	REGISTER FILE 4X4	74ACT670
U571	3E3	3326.0670	REGISTER FILE 4X4	74ACT670
U572	3C3	3326.0670	REGISTER FILE 4X4	74ACT670
U611	2E6	3722.5256.1	SRAM CMOS 85ns	32K X 8
U621	2B6	3722.5256.1	SRAM CMOS 85ns	32K X 8
U631	2B3	3722.5256.1	SRAM CMOS 85ns	32K X 8
U651	5B6	3331.5600	uPROCESSOR	DSP56001
U661	1B4	3326.0670	REGISTER FILE 4X4	74ACT670
U662	1F3	3326.0670	REGISTER FILE 4X4	74ACT670
U671	3B3	3326.0670	REGISTER FILE 4X4	74ACT670
U672	3E2	3326.0670	REGISTER FILE 4X4	74ACT670
U711	2E5	3722.5256.1	SRAM CMOS 85ns	32K X 8
U721	2B5	3722.5256.1	SRAM CMOS 85ns	32K X 8
U731	2B1	3722.5256.1	SRAM CMOS 85ns	32K X 8
U741	1G2	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U751	1E2	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U761	1D2	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U771	3C2	3326.0670	REGISTER FILE 4X4	74ACT670
U821	1A3,2D1,2E2,2H2,2H4,4D5	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U822	1C1	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U831	1A2	3326.0245	TRANSCVR 8X TRI-ST	74ACT245
U861	6B4,6B5,6G4	3333.8921	RS-422 DIFF TRANSCVR	DS8921
U871	3B2	3326.0670	REGISTER FILE 4X4	74ACT670
X87	6B3	4521.0011	TRANSFORMER SIGNAL DIP	100MHz

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION		
C101	1B2	2172.0104	CAP CERAM 100V 20%		.1uF
C111	1A7	2172.0104	CAP CERAM 100V 20%		.1uF
C121	1E7	2911.0227	CAP AL-EL 10V +80/-20%		220uF
C122	1B4	2172.0104	CAP CERAM 100V 20%		.1uF
C123	1C4	2172.0470	CAP CERAM 100V 20%		47pF
C124	1D4	2172.0470	CAP CERAM 100V 20%		47pF
C125	1D5	2172.0470	CAP CERAM 100V 20%		47pF
C126	1C5	2172.0104	CAP CERAM 100V 20%		.1uF
C127	1B5	2172.0104	CAP CERAM 100V 20%		.1uF
C128	1F4	2172.0104	CAP CERAM 100V 20%		.1uF
C129	1G2	2172.0102	CAP CERAM 100V 20%		.001uF
C131	1D2	2172.0104	CAP CERAM 100V 20%		.1uF
C132	1F4	2952.0105	CAP AL-EL 50V 20%		1uF
C141	1A4	2172.0104	CAP CERAM 100V 20%		.1uF
C142	1F4	2952.0105	CAP AL-EL 50V 20%		1uF
C143	1B2	2454.0334	CAP POLYE 50V 5%		.33uF
C144	1A3	2454.0105	CAP MICA 500V 5%		10pF
C151	1A2	2454.0223	CAP POLYE 50V 5%		.022uF
D121	1D5	3110.4152	DIODE SIGNAL		4152
D122	1C5	3110.4152	DIODE SIGNAL		4152
D123	1A5	3110.4152	DIODE SIGNAL		4152
P101	1C3	4221.0136	PLUG PC 90'	.1 X.39	36 PIN
P102	1H3	4221.0136	PLUG PC 90'	.1 X.39	36 PIN
P111	1C8	4221.0036	PLUG PC	.1 X.43	36 PIN
P141	1E2	4253.0001	JACK XLR PNL MT		MALE
R111	1B5,1C5,1D5	1985.4223	RES	NET SIP 2% B	4 X 22K
R121	1F2	1214.0101	RES 1/4W C FLM 5%		100
R122	1F2	1214.0301	RES 1/4W C F;M 5%		300
R131	1D2	1214.0750	RES 1/4W C FLM 5%		75
R132	1D3	1214.0102	RES 1/4W C FLM 5%		1K
R133	1A4,1B4,1C4,1D3	1984.4272	RES	NET SIP 5% I	4 X 2.7K
R134	1D7,1D3,1D4	1984.4303	RES	NET SIP 5% I	4 X 30K
R141	1E4	1214.0222	RES 1/4W C FLM 5%		2.2K
R151	1A2	1136.1240	RES 1/8W M FLM 1%		124
R152	1E3	1214.0510	RES 1/4W C FLM 5%		51
R153	1E3	1214.0510	RES 1/4W C FLM 5%		51
S151	1B2	4321.0003	SWITCH PUSH VERT		DPDT
U101	1C2,1C3	3640.0031	OPTICAL INTERFACE SPDIF		REC
U102	1H2,1H3	3640.0131	OPTICAL INTERFACE SPDIF		XMT
U111	1A7	3324.0251	MULTIPLEXER TRI-ST		74HCT251
U121	1A5,1B4,1D5,1F4	3323.0086	GATE 4-IN EXCL OR		74HC86
U131	1D6,1D7,1F5,1D4	3327.0004	BUFFER 6X INV UNBUFF		74HCU04
U141	1A3,1D3,1E4,1F5	3333.8921	RS-422 DIFF TRANSCVR		DS8921
X141	1A3	4521.0011	TRANSFORMER SIGNAL DIP		100MHz
X142	1F3	4521.0011	TRANSFORMER SIGNAL DIP		100MHz
X143	1E3	4521.0011	TRANSFORMER SIGNAL DIP		100MHz

DIO-2

DIGITAL I/O MODULE



DIGITAL INPUT/OUTPUT OPTION 9DIO.2000 (6400.DIO2.1)

DIO-2, DIGITAL AUDIO INPUT/OUTPUT MODULE

NOTE: There have been two versions of the DIO module. The version can be determined from the production code number located on the decal attached to the circuit board. The code number will have the format "DIOx-yyyyy-zz" where "x" is the DIO version.

Buffers and Address Decoding <1>

Schematic <1> shows the data and address bus interface to the DSP module. The 24 unbuffered data lines enter the board through connector J88. The unbuffered data lines are buffered by tri-state octal transceivers U581, U681 and U781. The direction of these buffers is controlled by buffered read strobe /BRD. They are enabled by AIOII which is generated in the DSP module address decoder pal.

The 16 address lines A0 through A15 and several control lines enter the board through connector J87. The address lines are buffered by octal buffers U761 and U762 before driving the RAM array as BA0 through BA14. Address line A15 is never used in buffered form. The lowest two address lines (A0 and A1) also drive I/O devices and are therefore buffered separately for this by two sections of U751. A0 and A1 become BA30 and BA31 after buffering.

The addresses of I/O devices on board are selected by one-of-eight decoders U631 and U432. These select one of four address ranges, each 4 addresses wide. Decoder U631 decodes writes and U432 handles reads.

Word Reversal Latches <1>

Register files U271, U281, U272, U282, U381 and U371 form a 4 deep by 24-bit wide set of word reversal latches. Their input bits are wired in opposite order to their output bits. Any data written to the buffers will be read back in bit reverse order. This means that the LSB will be swapped with the MSB. Bit 1 will be swapped with bit 22, etc. Since the registers are four deep, four separate data words may be written to this array for later readback.

Mode Control <1>

Octal latches U471 and U361 on schematic <1> latch mode and sample rate control bits. They are strobed via pin 11 when the processor performs a write operation to the appropriate memory location. These latches may be read back by the processor when a read is performed from the same address. This readback is enabled via pin 1.

The most significant bit of U361 is clamped by zener diode D2501 and routed to a rear panel bnc connector via R2501. Bit 22 is latched in U361, clamped by zener diode D1401 and routed to the 15-pin rear panel connector via R1401.

Status Buffer <1>

Half of octal tri-state buffer U262 is used to read the state of four status bits on the DIO-2 board. These are the AES/EBU receiver phase lock loop lock indicator (RLOCK), house sync phase lock loop lock indicator (TLOCK), the option dsp bus request output (/BUSRQ3) and an auxiliary data input from the 15-pin rear panel serial connector (AUX1).

Expansion Data RAM <2>

The nine 32k-by-8 static RAMs on schematic <2> are organized into two banks of 48k by 24-bit memory. One bank is mapped into X memory space and one into Y memory space. The X/Y select line from the processor is buffered by one section of octal buffer U762 and used to drive the most significant address bit of each RAM. Read and write strobe signals from the processor are buffered in two more sections of U751 and used to drive the output enable and write enable pins respectively of each RAM. The chip enable signals for each set of three RAMs is obtained from the DSP address decoder pal via J87.

Data Bus Termination <3>

Resistor networks R4701, R4801 and R3601 pull the data bus high when tri-stated, preventing illegal logic levels and reducing power dissipation.

Parallel Digital Input <3>

The parallel input accepts two channels of 24-bit data on a rear panel 34-pin connector and latches it when the strobe line is low. The data is latched into the channel A input when the channel select line is held low and the strobe is asserted. The data is latched into the channel B input when the channel select line is held high and the strobe is asserted. Latching channel B data also generates an interrupt for the System One, causing it to read both channels of data just written to the latches. The channel select line must be held either high or low during the entire time the strobe line is low. A transition on the channel select line while the strobe line is low will cause an incorrect latch operation. Note that data must always be supplied to Channel B since its latch operation triggers the dsp to read the data. If a single channel interface is desired it must therefore be configured as Channel B and the channel select line connected to +5V.

The parallel input consists of 4 x 4 register files U492, U591, U592, U691, U791 and U792. Only two sections of each is used, forming a dual 24 bit wide latch. One latch is dedicated to each input channel. The channel selection bit is applied to pin 28 of the connector. This is buffered by one section of octal buffer U262 and applied to an address select input of the register files. Clamp diode D4901 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R2602 and capacitor C2602 reduce the effect of external cable crosstalk and noise. The write strobe is active low and is applied to pin 30 of the interface. This is buffered by one section of octal buffer U262 and applied to the write enable input of the register files. Clamp diode D5901 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R2604 and capacitor C2604 reduce the effect of external cable crosstalk and noise. The channel select and strobe inputs are internally pulled high by R2605. Strobe pulses are gated with the channel select line and coupled to the processors interrupt selection logic by an AND gate in U261. The processor will be interrupted (signalling new input data) only when the channel select line is high (channel B writes).

Parallel Digital Output <3>

The output port provides 24-bit data on the data lines at all times. The channel select line determines which channels data appears on these lines. The read strobe line causes both channels of data to be updated and signals the System One processor that another pair of data words are required. The data is buffered with a two stage FIFO which guarantees that data will be available when needed rather than after the service delay of the processor. As long as the maximum sample rate restriction is obeyed the two stage buffer will never empty. If a single channel output is desired the port may be configured as Channel B or Channel A and the channel select line connected to +5V or ground, respectively.

The parallel output consists of 4 x 4 register files U191, U291, U292, U391, U392 and U491. All four sections of each are used, creating four 24-bit wide latches. Two latches are dedicated to each output channel. The channel selection bit is applied to pin 28 of the connector. This is buffered by one section of octal buffer U262 and applied to an address select input of the register files. Clamp diode D2602 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R2603 and capacitor C2603 reduce the effect of external cable crosstalk and noise. The read strobe is active low and is applied to pin 30 of the interface. This is buffered by one section of octal buffer U262. Clamp diode D2601 prevents reverse voltage on the input and eliminates undershoot on long cables. Resistor R2601 and capacitor C2601 reduce the effect of external cable crosstalk and noise. The channel select and strobe inputs are internally pulled high by resistor network R2605. Strobe pulses are gated with the channel select line and coupled to the processors interrupt selection logic by an AND gate in U261. The processor will be interrupted (signalling new output data) only when the channel select line is high (channel B reads). The gated read strobe also causes flip-flop U831 to change state. The Q and /Q outputs are wired to the second address inputs of the register files. When a read is performed the two data latches are swapped with a alternate set. This creates a two stage FIFO, allowing the processor to update the channels consecutively without the interchannel delay being visible externally.

The 24 data output lines are isolated by resistor networks R3901, R3902, R2901, R2902, R1901 and R1902. These provide some damping when driving long lines and limit the rise time. There are no clamping circuits to prevent damage on either the input or output bits. Since this greatly increases the risk of damage due to misuse, all register files have been mounted in sockets. Both the parallel input and output connectors provide +5V on a connector pin through a series thermistor. These limit the current under short circuit conditions to prevent overloading of the System One power supply.

The parallel inputs and outputs may be operated at any sample rate selectable from the panel of the dsp program being run. The internal sample clock generator can produce a square wave sample clock at 32 kHz, 44.1 kHz or 48 kHz. The dsp program in use may limit the choice of sample rates based on processing time limitations. Many of the dsp programs limit the maximum sample rate to 48 kHz.

AES/EBU Interface Hardware

A block diagram of the AES/EBU interface circuitry contained in the Audio Precision System One Dual Domain test system is shown in Figure DIO2.1. Signal generation timing may be driven from the internal crystal oscillators or may be slaved to the received signal or an external sync signal. The external sync signal drives a phase locked loop to generate the high frequency clock (128 x Fs) necessary for clocking the internal logic. The hardware is timed by a master timing generator which is clocked from the selected source. The preambles are always generated with the same polarity to allow testing of polarity sensitivity in the device under test. The interface dsp then outputs the serial data signal with bit reversed order to the transmit logic at the appropriate time in the transmitted word. After the last bit in the data stream the validity, user and status bits are selected. These are bi-phase mark encoded in hardware, converted to a differential signal and output. An appropriately attenuated version is also output to drive consumer interface devices.

On the receive side, the input signal is taken from its balanced form and converted to an unbalanced form by the transformer and line receiver. This drives a sync detector and phase lock loop clock generator identical to that used for the external sync input. This clock operates the preamble detector and bi-phase decoder and is available to drive the transmit logic. The preamble detector identifies the presence of one of the three valid preambles and outputs a channel select signal indicating which channel is being received. When a block preamble is detected a pulse is generated lasting one frame indicating that the words being received are the first in the block. The bi-phase decoder takes the encoded data and flag bits and recreates a NRZ data stream. The data separator passes the audio data to the dsp serial input and latches the flag bits for later examination. A parity checker also accesses the NRZ data stream to compute parity on the data and flag bits.

AES/EBU and Serial Inputs <4>

In units manufactured before January 1991, the signal from the front panel enters the board via P11A. It is coupled through transformer X310 into differential line receiver U401A. The output of this gate is a ground referenced AES/EBU signal. In units manufactured after January 1991, components C4401, X310, and U401 are deleted and functionally moved to the DDI-3 circuit board mounted directly behind the front panel connectors. In these units the serial input signal enters the DIO-2 board via J41 and is labeled DDI_IN.

Programmable logic device U422 detects the sync preambles in the DDI_IN signal to provide a reference for the phase lock loop. There are two sync detector circuits inside U422, one is used for 32 kHz and the other for 44.1 kHz and 48 kHz sample rates. Pin 21 of U422 goes low whenever the 32 kHz sync detector finds a sync preamble. The combination of R6301, D6301 and C2603 senses this and holds pin 5 of U422 low if syncs are detected. The output on pin 20 will then be the output of the 32 kHz sync detector. If no syncs are detected pin 5 will go high and the 44.1kHz/48kHz detector will be enabled. The output on pin 20 will then be the output of the 44.1kHz/48kHz detector. Since preambles occur at the beginning of each channel of data the signal at the output of U422 will be at twice the audio sample rate.

The DDI_IN signal is also fed to a delay circuit consisting of R4201, C4202, U611, R6201 and C6201. The delayed signal drives shift register U421 and an exclusive-OR edge detector consisting of R6101, C6101 and part of U611. Its output is used to re-clock the sync preamble detection pulse in flip-flop U420. A high frequency clock at 256 times the audio sample rate is generated by a phase lock loop consisting of U121, U230 and the associated components. The phase lock loop U121 contains a phase detector, VCO and lock detect circuit. The re-clocked output of the sync detector from U420 drives the pin 14 input of the phase detector through U261. The reference input (pin 3) of the phase detector normally comes from the divide by 128 output of the counter through U251 (acting as a switch). The VCO center frequency and tuning range is determined by C2203, R1202 and R1203. The phase detector output is filtered by R1204, R1205 and C2202 to produce the loop control voltage into the VCO. The loop will seek a point at which the VCO output frequency is correct to produce equal input frequencies at the two phase detector inputs.

The outputs of the shift register U421 will be 8 consecutive cells in the AES/EBU signal. When U410 detects a preamble at these outputs it indicates whether it is a channel A, channel B or block sync type. This is used to create a channel A/channel B signal (SIA/B at pin 17) and a start of block signal (SIBLK at pin 16). A word sync output is also derived which pulses at the end of each channel A preamble to synchronize the bit counter U212.

The bit counter U212 tracks the current position in the AES/EBU word. This count is decoded by U221 and used to create the bit clock and word clock necessary to drive the dsp serial input port. The first two outputs of shift register U421 are decoded in U221 to create normal binary data from the bi-phase encoded data. This data is gated in U221 before being routed to the dsp serial input. The status, validity and user bits of the serial stream are also decoded and latched in U221 before driving dedicated input pins on the processor. U221 also derives the parity information for the received bits and this is latched in U420B. The parity flag (SIPARITY) is connected to an additional input of the processor.

AES/EBU Transmitter <5>

The clock to drive the AES/EBU transmit circuitry is at 128 times the sample rate and is selected by U251. Either the internal crystal oscillators, the AES/EBU receiver, or the house sync input may be used as the selected clock source. The selected clock source drives a 16 bit counter consisting of U311, U321, and U430. The lower 7 bits of the counter serve as an address for registered ROM U331. The ROM generates control and data signals for the bi-phase encoder U231 and the dsp processor U671. The timing diagram of the transmit circuitry is illustrated in Figure DIO2.2. Signals E0 through E3 (pins 9, 10, 11 and 14) are the state control signals for the encoder. PRE (U331 pin 14) is the preamble to be output over the interface. The dsp serial output bit clock is labeled SO_BCK and comes from U331 pin 15. This is gated on for 24 clock cycles to clock the data out of the processor. The word clock for the processor is labeled SO_SYNC and comes from U331 pin 16. The processor outputs data bits (SO_DATA), the validity bit (SO_VAL), the status bit (SO_STAT) and the user bit (SO_USER). These bits are combined and bi-phase encoded to produce the output signal at pin 19 of U231. In units manufactured before January 1991 this signal is balanced by U401B and coupled through transformer X210 to the output jack via P11B. In units manufactured after January 1991, the signal from pin 19 of U231 is labeled DDI_OUT and coupled to the DDF-3 circuit board through J41 pin 3.

Block sync is generated every 192 pairs of data words by U430 and a registered AND gate in U231. This block sync output appears on U231 pin 16 and shifts the address of U331 to generate the appropriate preamble for the block sync. This signal (SOBLK) also drives an input of the processor to signal that the start of a new status bit block has begun.

AES/EBU Interface Processor <5>

The dsp processor U671 accepts the serial data and bit flags from the AES/EBU receive input. It performs appropriate checking of those bits and sends the result to the main dsp for processing. It also accepts the AES/EBU data from the main processor and supplies the signals needed for the transmitter circuitry.

Part of U261 is used as an interrupt selector for the AES/EBU processor. The external interrupts may come from the parallel ports or from a flag input (/OPTFLAG) created by U631. The choice of interrupt sources is selected by IRQ0 from U471. U261 combines the flag input with the buffered address line BA1 to create two flag inputs, depending on the address written to U261. The /OPTRST signal, causes U261 to tri-state its outputs when asserted low. When this occurs the interrupt inputs are driven through resistors R1701 and R1702 from the MODE0 and MODE1 bits. The processor latches the levels on its interrupt inputs as it exits reset and uses the two bit value to select the memory map and reset vector. This allows the host computer to control the memory mode of the processor as it exits reset.

House Sync Receiver <6>

The signal from the rear panel enters the board via P89. It is coupled through transformer X89 into differential line receiver U881. The output of this gate is a ground referenced AES/EBU signal. Programmable logic device U731 detects the sync preambles on the signal to provide a reference signal for the phase lock loop. There are two sync detector circuits inside U731, one is used for 32 kHz and the other for 44.1 kHz and 48 kHz sample rates. Pin 21 of U731 goes low whenever the 32 kHz sync detector finds a sync preamble. The combination of R6303, D6303 and C6302 senses this and holds pin 5 of U731 low if syncs are detected. The output on pin 20 will then be the output of the 32 kHz sync detector. If no syncs are detected pin 5 will go high and the 44.1kHz/48kHz detector will be enabled. The output on pin 20 will then be the output of the 44.1kHz/48kHz detector. Since preambles occur at the beginning of each channel of data the signal at the output of U731 is twice the audio sample rate.

The AES/EBU signal is also fed to a delay circuit consisting of R8402, C7402, U841, R8401 and C7401. The delayed signal drives an exclusive-OR edge detector consisting of R8302, C8301 and part of U841. Its output is used to re-clock the sync preamble detection pulse in flip-flop U831. A high frequency clock at 256 times the audio sample rate is generated by a phase lock loop consisting of U721, U741 and the associated components. The phase lock loop U721 contains a phase detector, VCO and lock detect circuit. The re-clocked output of the sync detector from U831 drives the pin 14 input of the phase detector. The reference input (pin 3) of the phase detector comes from the divide-by-128 output of the counter. The VCO center frequency and tuning range is determined by C7204, R7102 and R7103. The phase detector output is filtered by R7104, R7105 and C8202 to produce the loop control voltage into the VCO. The loop will seek a point at which the

VCO output frequency is correct to produce equal input frequencies at the two phase detector inputs.

The house sync may also operate with a TTL squarewave instead of an AES/EBU input as a reference signal. In this mode pin 8 of U731 (TTL) is driven high, changing the logic of the sync detector. In the TTL mode the sync detection logic is bypassed and the input signal appears on pin 20 of U731. This is re-clocked by the flip-flop U831 and a delayed replica of the reference input appears at the phase comparator input. The phase lock loop is designed to lock onto a reference signal of twice the desired audio sample rate, requiring a 96 kHz reference input for a 48 kHz sample rate output.

Front Panel I/O without Optical <7a>

Schematic <7a> applies only to those units manufactured before January 1991, which have not been modified with a retrofit kit. U401 converts the unbalanced output signal to a balanced format and receives the balanced input and converts it to an unbalanced form. X310 and X210 provide additional ground loop rejection and isolation. Resistors are used to terminate the AES/EBU input with 240 Ohms and terminate the SPDIF input with 75 Ohms. The voltage of an AES/EBU output is 5 V behind a 120 Ohms output impedance. The SPDIF output is attenuated to provide 0.5 V from 75 Ohms when correctly terminated. The capacitors block dc from appearing across the transformers or attenuator resistors.

Front Panel I/O with Optical <7b>

The Digital I/O connector front panel assembly includes a small circuit board called the DDI-3. Circuits on the DDI3 board buffer the AES/EBU, SPDIF and optical EIAJ signals individually.

The AES/EBU input enters on connector J151, through dc blocking capacitor C151 to transformer X141. The input impedance is switchable by S151 between 120 Ohms and 10k Ohms to allow bridging operation. The transformer output is converted to unbalanced operation and buffered by U141A. The SPDIF input enters on J131 and is terminated by R131. U131A acts as a buffer amplifier to boost the incoming 0.5 V signal. U131B and U131C create a Schmitt trigger buffer which squares the input into a proper logic signal. U101 converts the optical input to an electrical signal.

The three input signals drive multiplexer U111 and edge detectors formed by U121B, U121C and U121D. The edge detectors sense the presence of signal and store this information in peak detectors. The multiplexer uses these three signal present indications to decide which input signal to pass to the output. If multiple inputs are present simultaneously the AES/EBU signal has the highest priority, followed by optical input. U131F overrides the input selection and forces the AES/EBU output signal (U111 pin 12) to be looped back for self test applications.

The AES/EBU output is balanced by U141 and isolated by transformer X143. Resistors R153 and R152 build out the impedance to approximately 110 Ohms. U121 drives the SPDIF output through X142. The attenuator formed by R122 and R121 drops the signal level to 0.5V at a source impedance of 75 Ohms. The optical conversion is provided by U102.

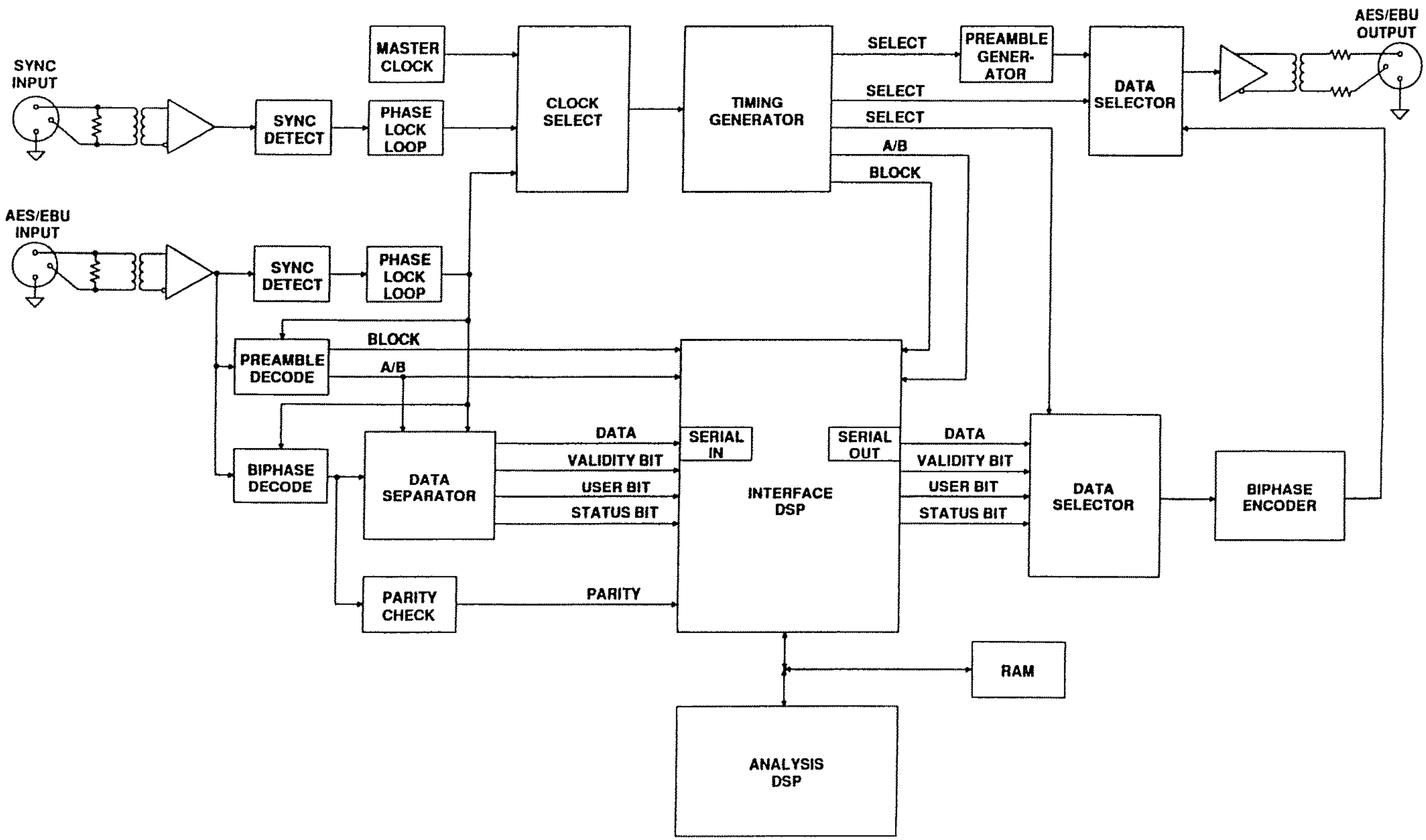


Figure DIO2.1 AES-EBU INTERFACE BLOCK DIAGRAM

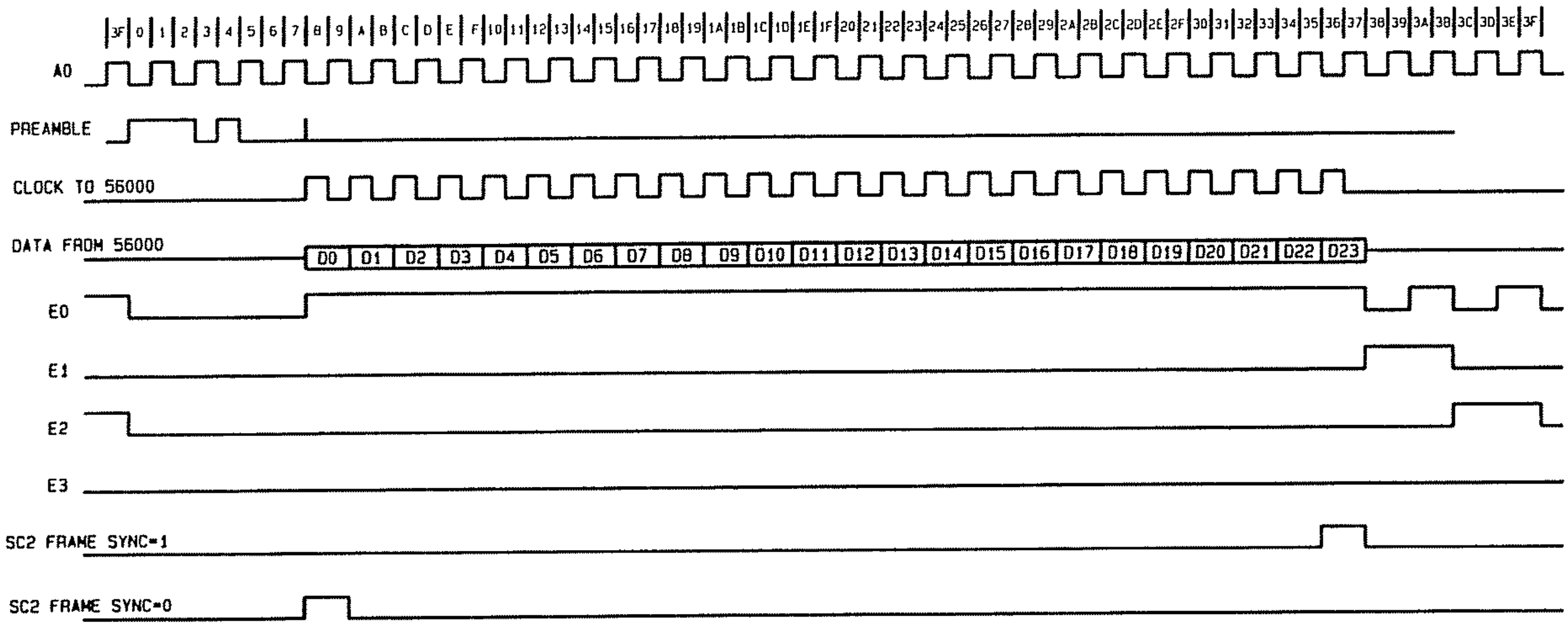


Figure DIO2.2 AES-EBU TRANSMITTER TIMING

AES/EBU INTERFACE SPECIFICATION

The AES digital interface specification was standardized in 1985. An essentially identical specification was promulgated by the EBU. It is a serial interface so as to require a minimum of wiring between devices. It provides for two channels of 20-bit or 24-bit digital audio data. These channels are referred to as A channel and B channel. The structure of the serial word is detailed in Figure DIO2.3. If 20-bit data is transmitted the remaining 4 bits may be used for an unspecified auxiliary signal.

The digital audio data is sent LSB first. If the full 24-bit data size is not used the lower bits must be zero filled to place the MSB in the same position. There are also three individual bits per channel. One is dedicated to a validity flag which indicates if the corresponding audio sample is a valid reliable audio sample or if it has been interpolated due to the correct data being unavailable. The second individual bit is called the user bit and is available for carrying any data the user cares to send in it. This provides a single bit per audio sample, requiring a series of samples to carry a complete message. The framing of this bit is undefined in the standard, making any uniform use of the bit impossible. The third bit is the channel status bit which conveys one bit of a 192-bit data "block". After every 192 pairs of audio samples the block is refreshed. The 192 bits are divided into 24 bytes, and the bytes are allocated to various functions.

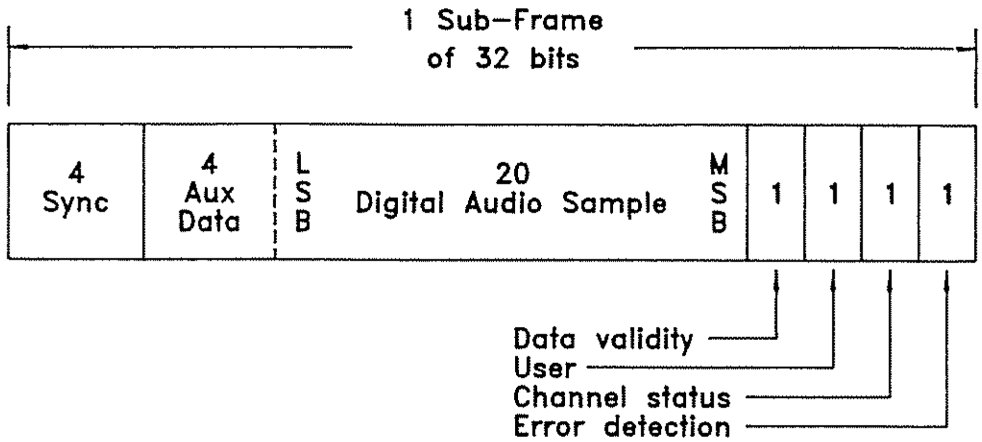
The last bit is a parity check bit which serves to force an even number of transitions in the transmitted signal and allows a simple check for errors in the received data. The parity checking function can determine that an odd number of errors (1, 3, 5, etc) occurred in the data stream. An even number of errors will result in correct parity and therefore will not indicate bad data.

The complete signal comprises 28 data bits to which is added a preamble occupying as much time as 4 data bits to make a total of 32 bit times per channel. The serial signal is bi-phase encoded with a technique called "bi-phase mark encoding" (there are other forms of bi-phase encoding). The bi-phase mark encoding process provides a transition from high to low or low to high at every cell boundary. If the data is a "1" there will also be a transition at the center of the data cell. If the data bit is a "0" there will be no transition at the center of the cell. This process is diagrammed in Figure DIO2.4. The advantage of this technique is that there is always a transition at a data cell boundary. This allows clock recovery circuits in the receiver to sense these edges to determine the start of each data cell. Since the information is contained in the timing of the transitions, not their direction, the resulting signal is polarity insensitive. If the signal is inverted there will be no change in the meaning of the data. This encoding also reduces the low frequency content in the signal, eliminating dc and allowing ac coupling.

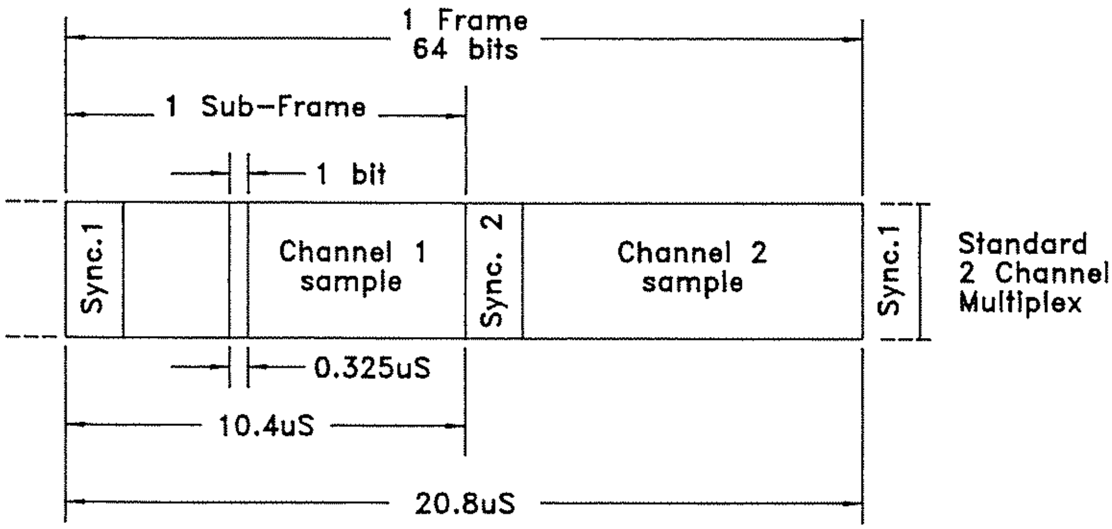
The preamble added to the start of the 28 data bits occupies a time period equivalent to that of 4 data bits. However, the preambles violate the bi-phase mark encoding rules by not necessarily having a transition at each cell boundary. There are three preambles defined in the standard; one for the B channel data words, one for normal A channel data words, and one which replaces the A channel sync every 192 pairs of data words to establish block sync of the channel status data. These preambles are illustrated in Figure DIO2.5. There are two versions shown for each, the appropriate one depends on the polarity of the signal on the line.

To understand the interface timings, consider the high or low pulse widths encountered at each of the three standard sample rates. Data bits are one of two widths, depending on whether they are a 1 or a 0. The sync pattern contains a wider high and low level, equivalent in width to three data 1 pulses.

Rate	"1" Width	"0" Width	Sync Width
48 kHz	163 ns	326 ns	488 ns
44.1 kHz	177 ns	354 ns	531 ns
32 kHz	244 ns	488 ns	732 ns



Format for 1 Channel Signal



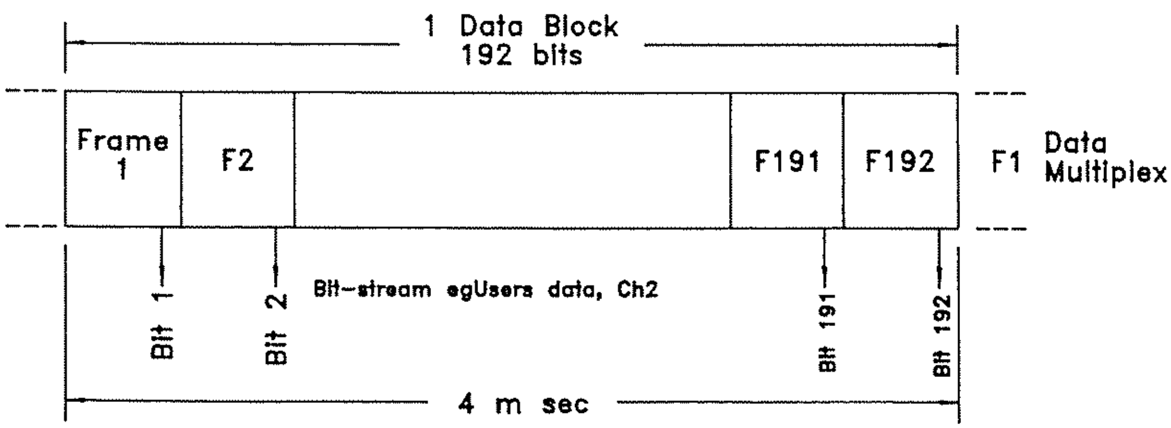
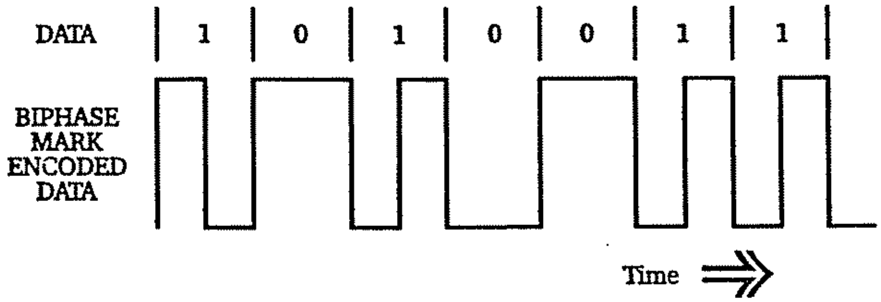


Figure DIO2.3 AES-EBU BIT STRUCTURE

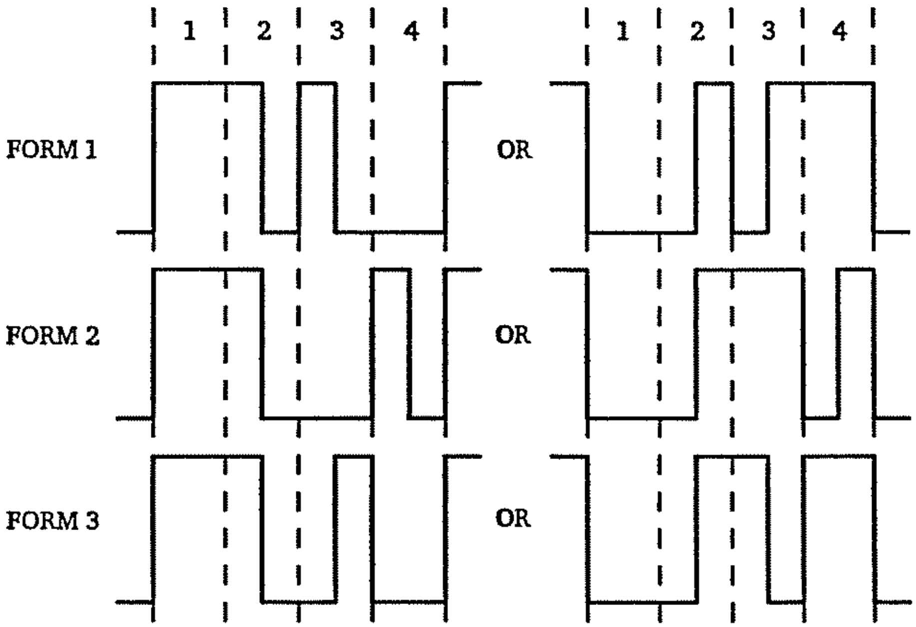


Biphase Mark always transitions at beginning of interval.

Logical 1 encodes a transition in the center of the data bit.

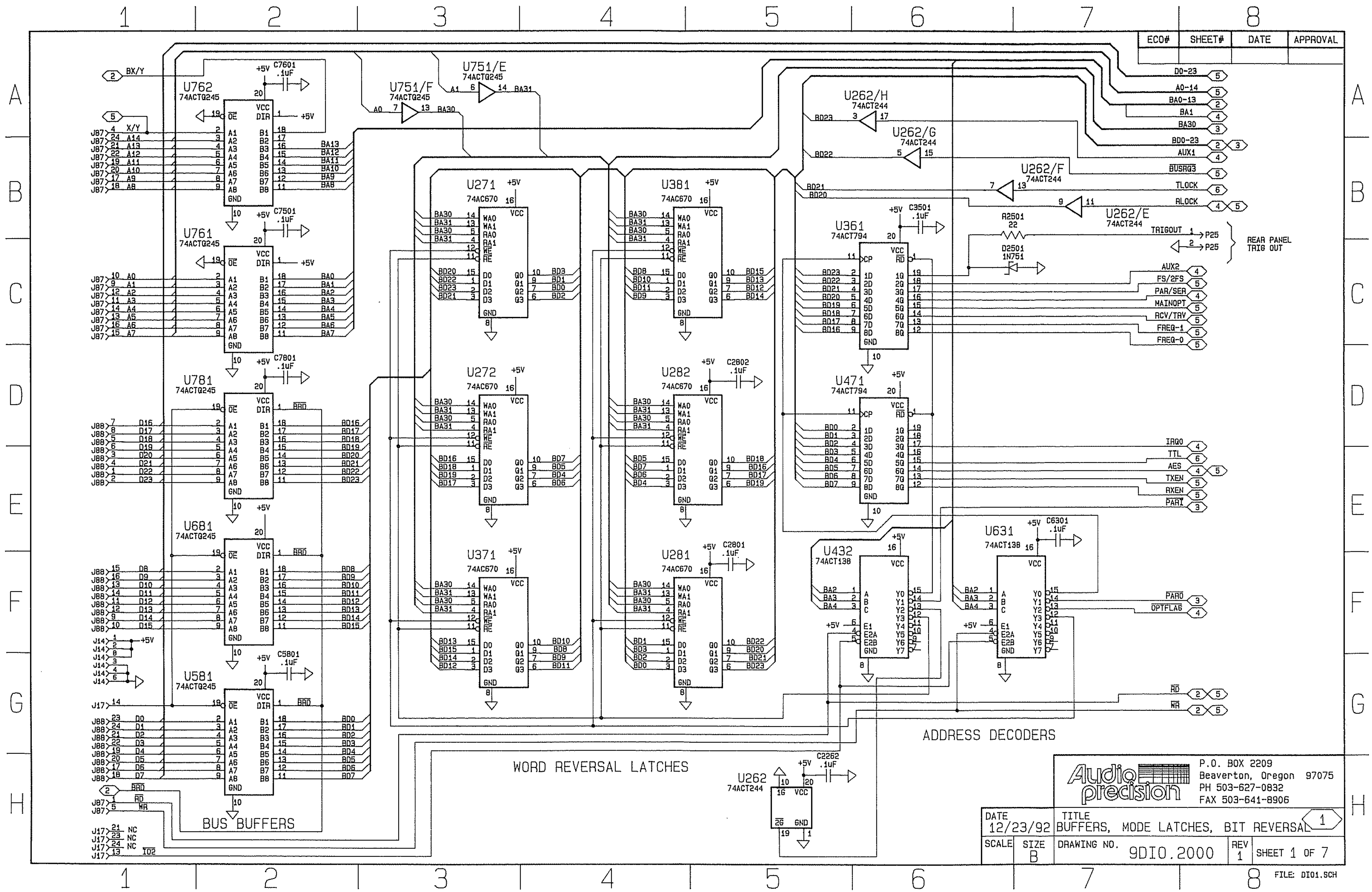
Logical 0 has no transition in the center of the data bit.

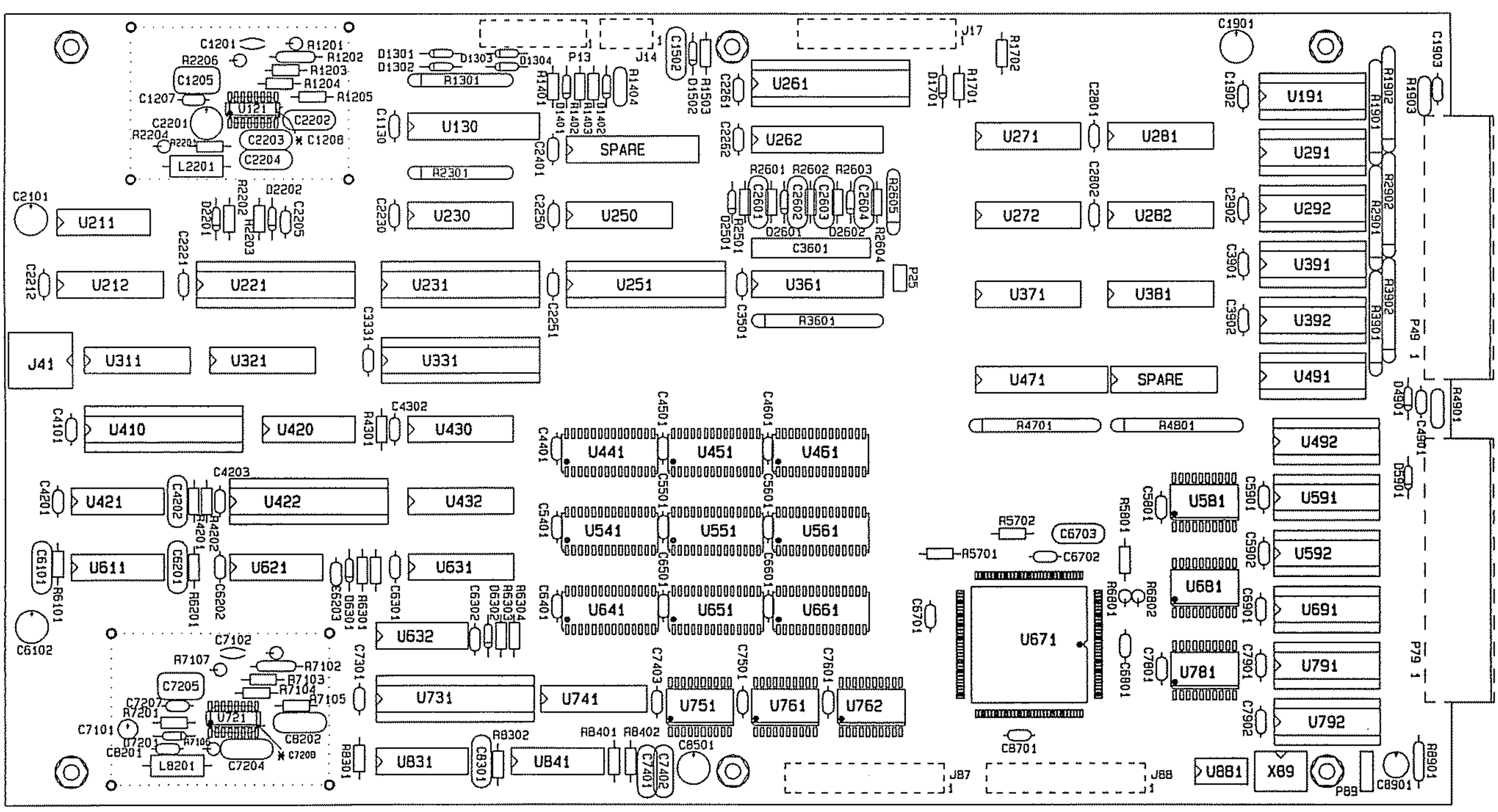
Figure DIO2.4 BIPHASE ENCODING



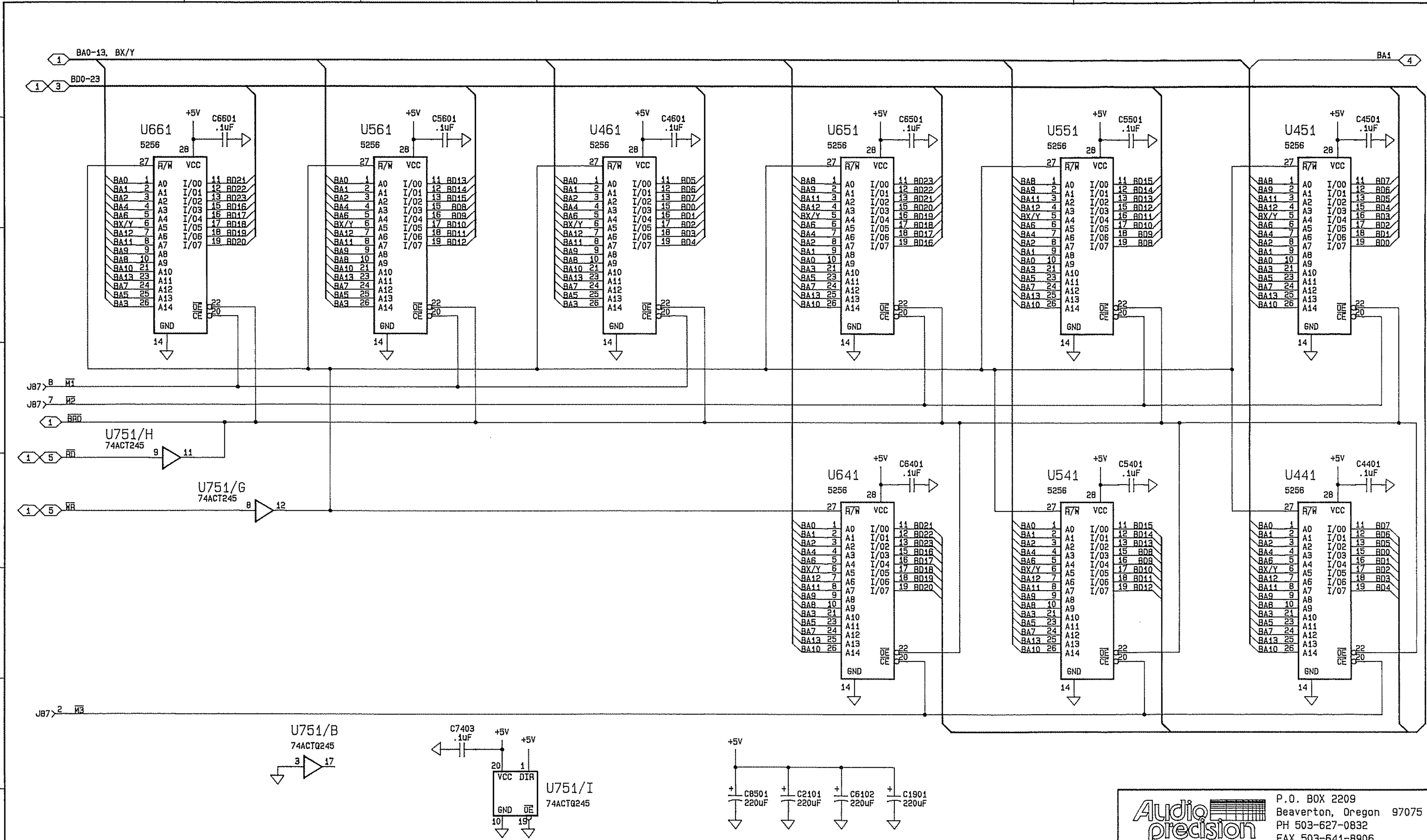
Preamble forms. The three types of sample preamble used are (1) channel A, subframe, and block synchronizing; (2) channel A, otherwise; and (3) channel B.

Figure DIO2.5 AES SYNCHRONIZATION


ECO#
SHEET#
DATE
APPROVAL
U762
74ACTQ245
U761
74ACTQ245
U781
74ACTQ245
U681
74ACTQ245
U581
74ACTQ245
U751/F
74ACTQ245
U751/E
74ACTQ245
U271
74AC670
U272
74AC670
U371
74AC670
U381
74AC670
U282
74AC670
U281
74AC670
U262/H
74ACT244
U262/G
74ACT244
U262/F
74ACT244
U262/E
74ACT244
U361
74ACT794
U471
74ACT794
U432
74ACT138
U631
74ACT138
U262
74ACT244
REAR PANEL
TRIG OUT
BUS BUFFERS
WORD REVERSAL LATCHES
ADDRESS DECODERS
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
12/23/92
TITLE
BUFFERS, MODE LATCHES, BIT REVERSAL
SCALE
SIZE
B
DRAWING NO.
9DIO.2000
REV
1
SHEET 1 OF 7
FILE: DIO1.SCH



DIGITAL INPUT/OUTPUT OPTION 9DIO.2000 (6400.DIO2.1)

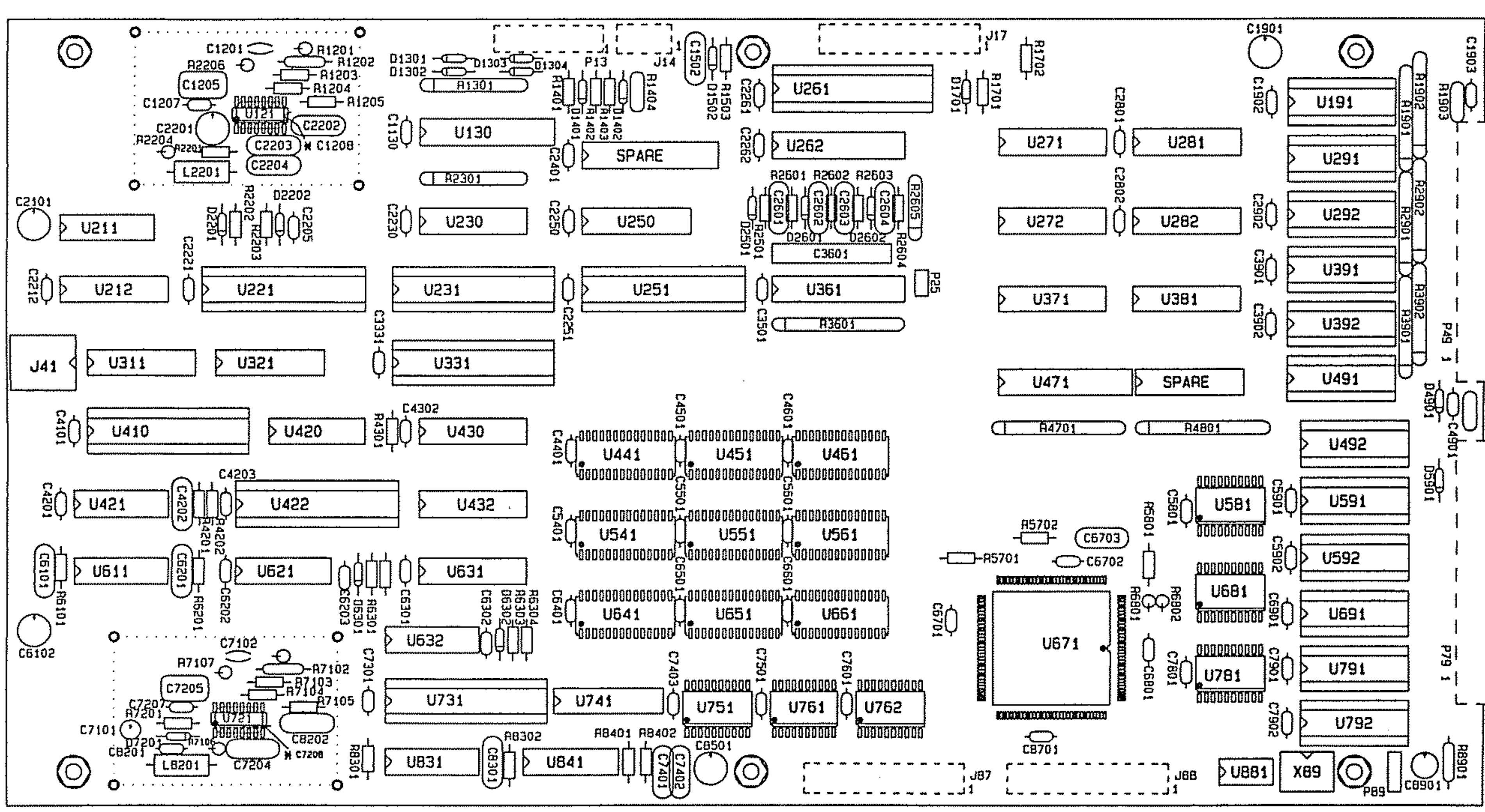


Audio precision

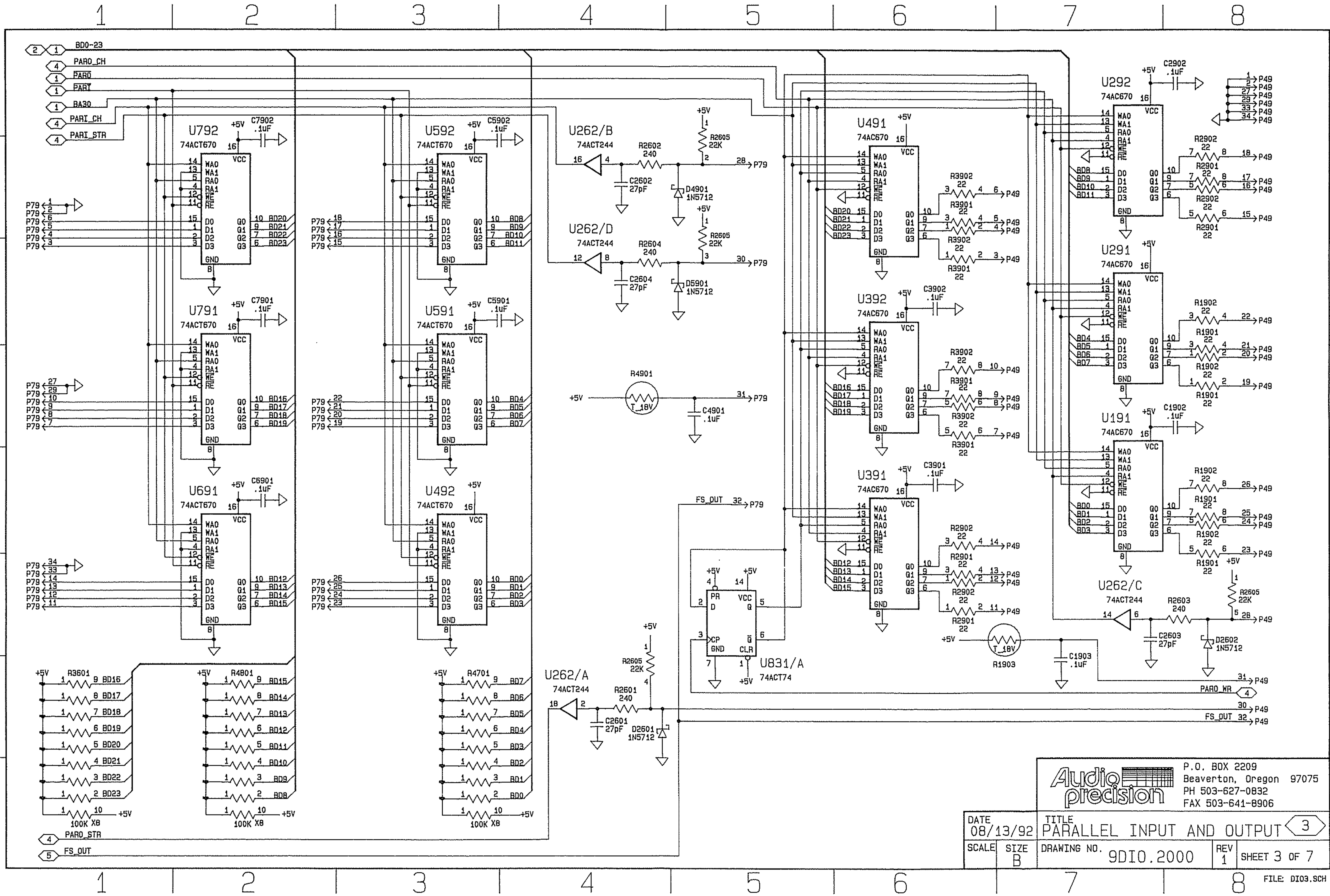
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE	
08/13/92	DATA MEMORY	2
SCALE / SIZE B	DRAWING NO. 9DI0.2000	REV 1 — SHEET 2 OF 7

FILE: DI02.SCH



DIGITAL INPUT/OUTPUT OPTION 9DIO.2000 (6400.DIO2.1)

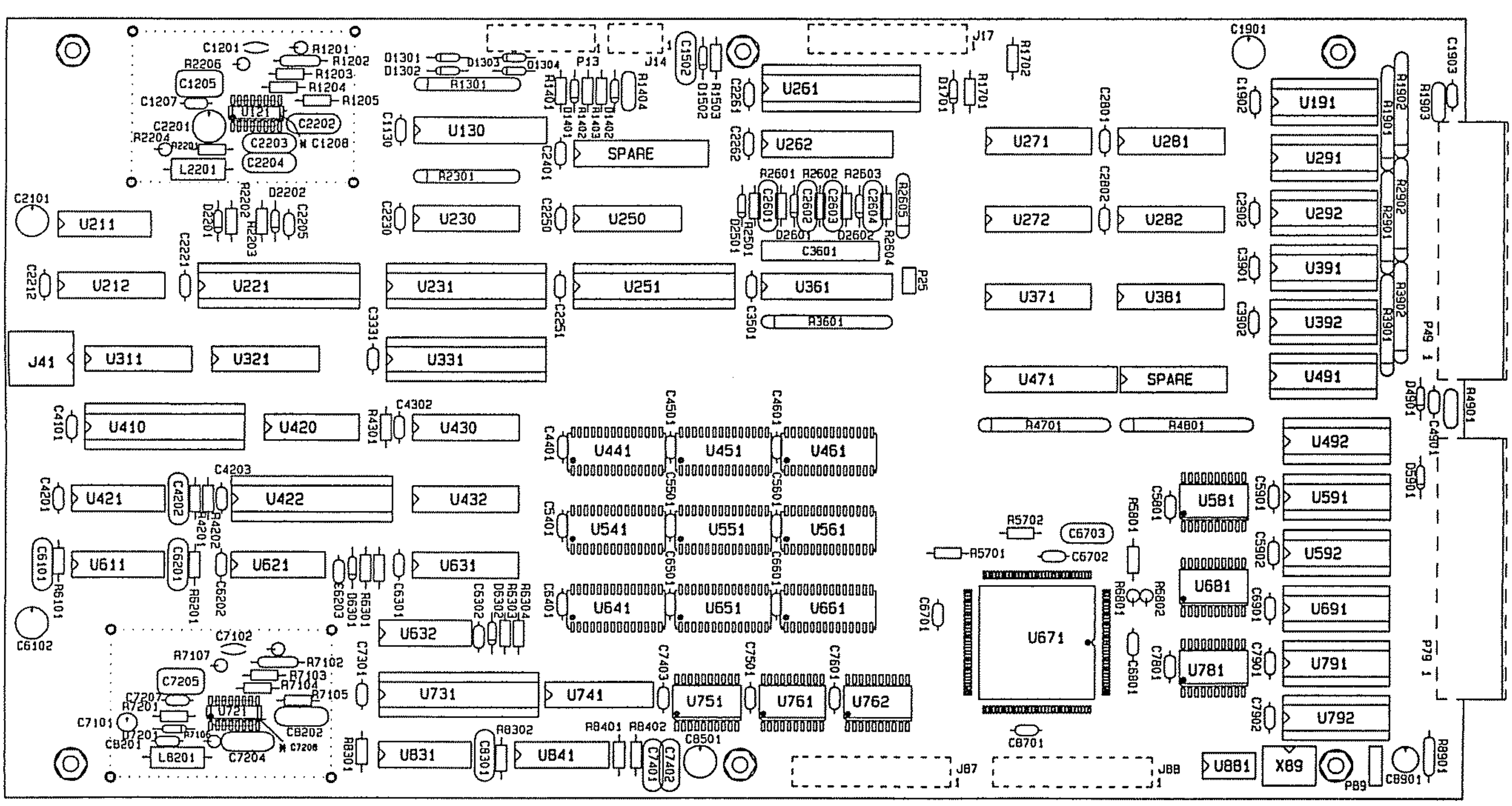


P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

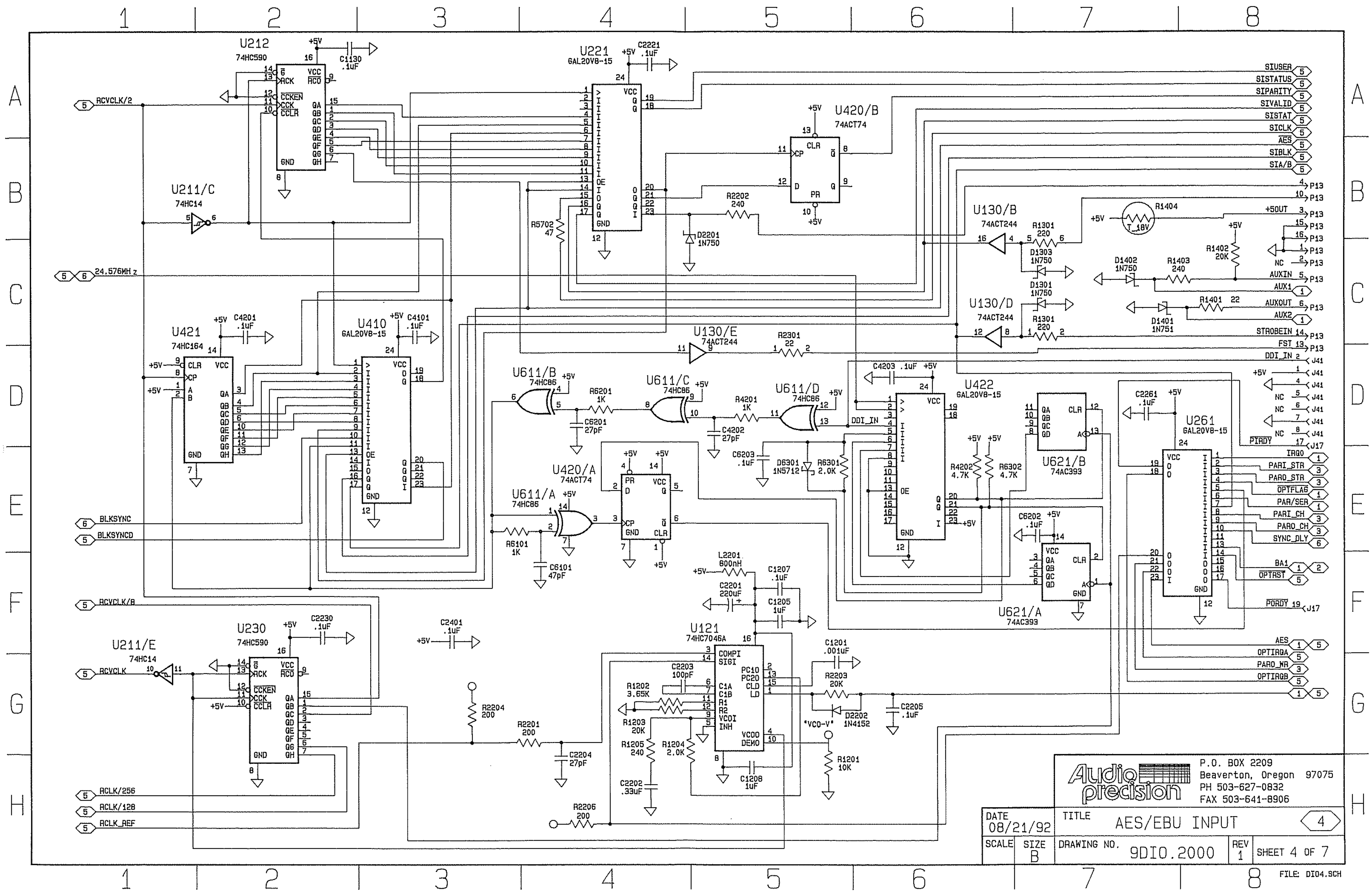
DATE	TITLE	
08/13/92	PARALLEL INPUT AND OUTPUT	3

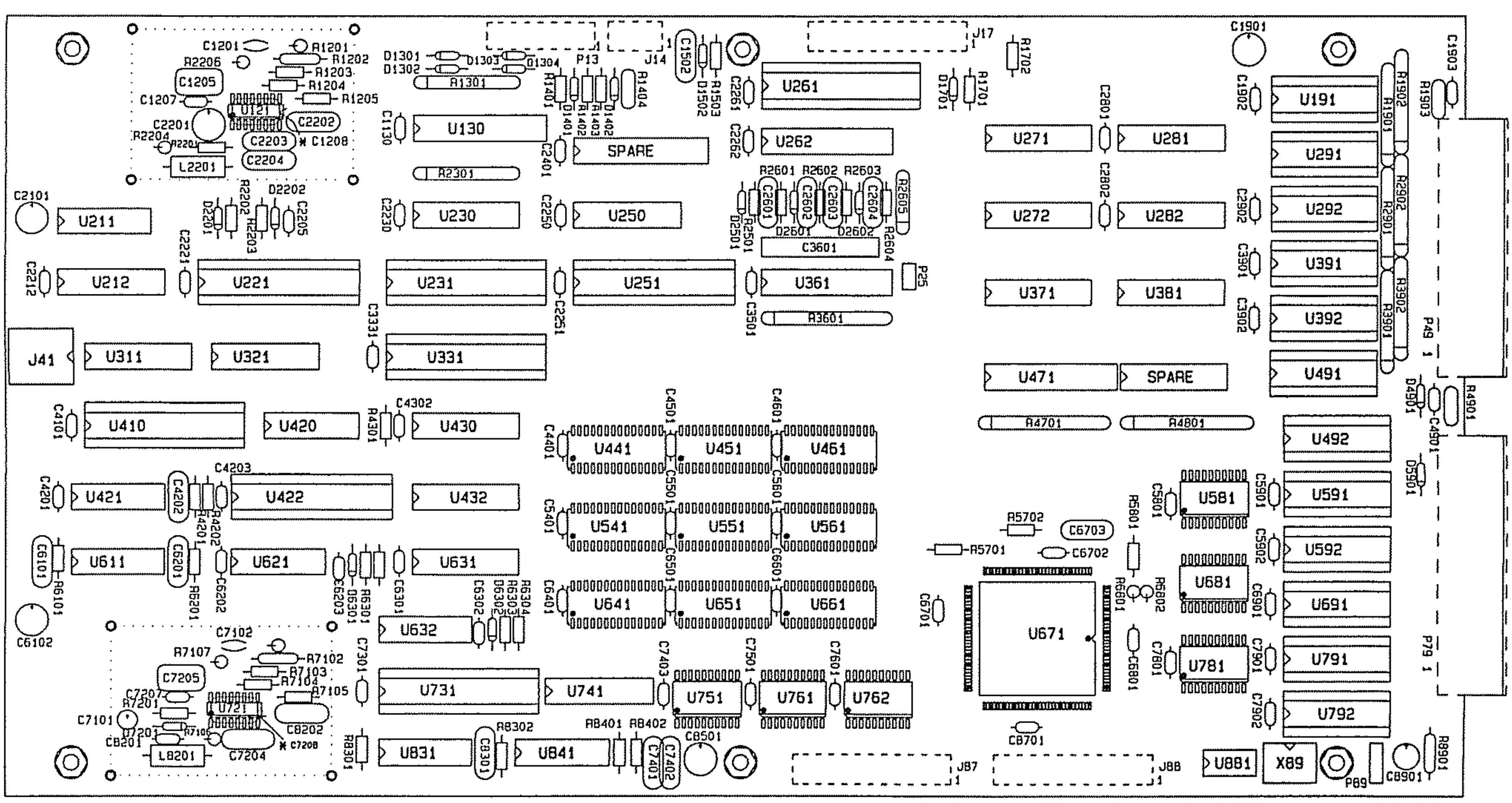
SCALE	SIZE	DRAWING NO.	REV	
	B	9DIO.2000	1	SHEET 3 OF 7

FILE: DIO3.SCH

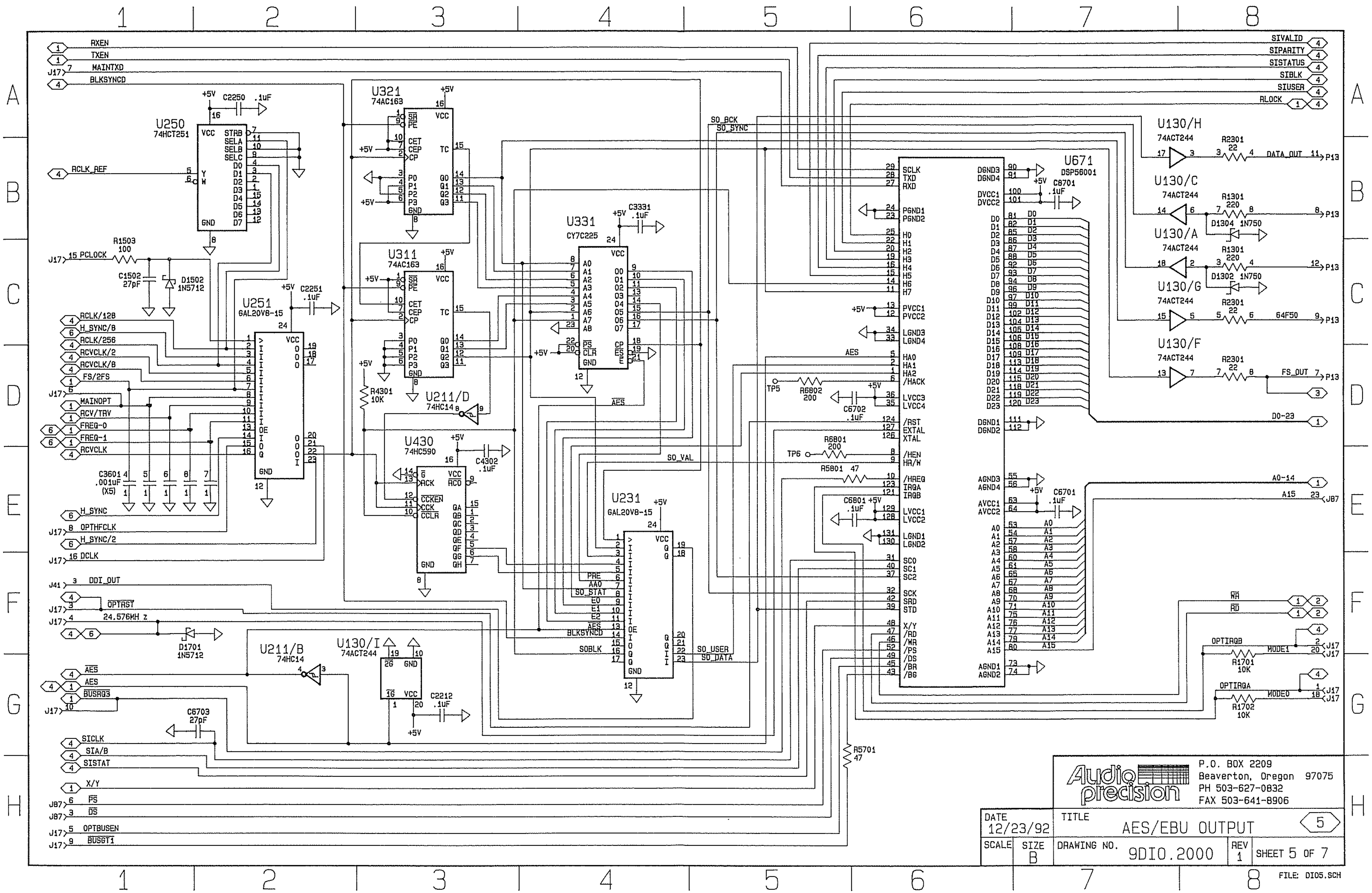


DIGITAL INPUT/OUTPUT OPTION 9DIO.2000 (6400.DIO2.1)


U212
74HC590
U221
GAL20V8-15
U420/B
74ACT74
U211/C
74HC14
RCVCLK/2
24.576MHz
U421
74HC164
U410
GAL20V8-15
U130/B
74ACT244
U130/D
74ACT244
U130/E
74ACT244
U611/B
74HC86
U611/C
74HC86
U611/D
74HC86
U611/A
74HC86
U420/A
74ACT74
U422
GAL20V8-15
U621/B
74AC393
U621/A
74AC393
U261
GAL20V8-15
BLKSYNC
BLKSYNCD
RCVCLK/8
U211/E
74HC14
RCVCLK
U230
74HC590
U121
74HC7046A
RCLK/256
RCLK/128
RCLK_REF
SIUSER
SISTATUS
SIPARITY
SIVALID
SISTAT
SICLK
AES
SIBLK
SIA/B
+50UT
AUXIN
AUX1
AUXOUT
AUX2
STROBEIN
FST
DDI_IN
PIRDY
IRQ0
PARI_STR
PARO_STR
OPTFLAG
PAR/SER
PARI_CH
PARO_CH
SYNC_DLY
BA1
OPTRST
PORDY
AES
OPTIRQA
PARO_WR
OPTIRQB
"VCO-V"
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 08/21/92
TITLE AES/EBU INPUT
4
SCALE
SIZE B
DRAWING NO. 9DIO.2000
REV 1
SHEET 4 OF 7
FILE: DIO4.SCH



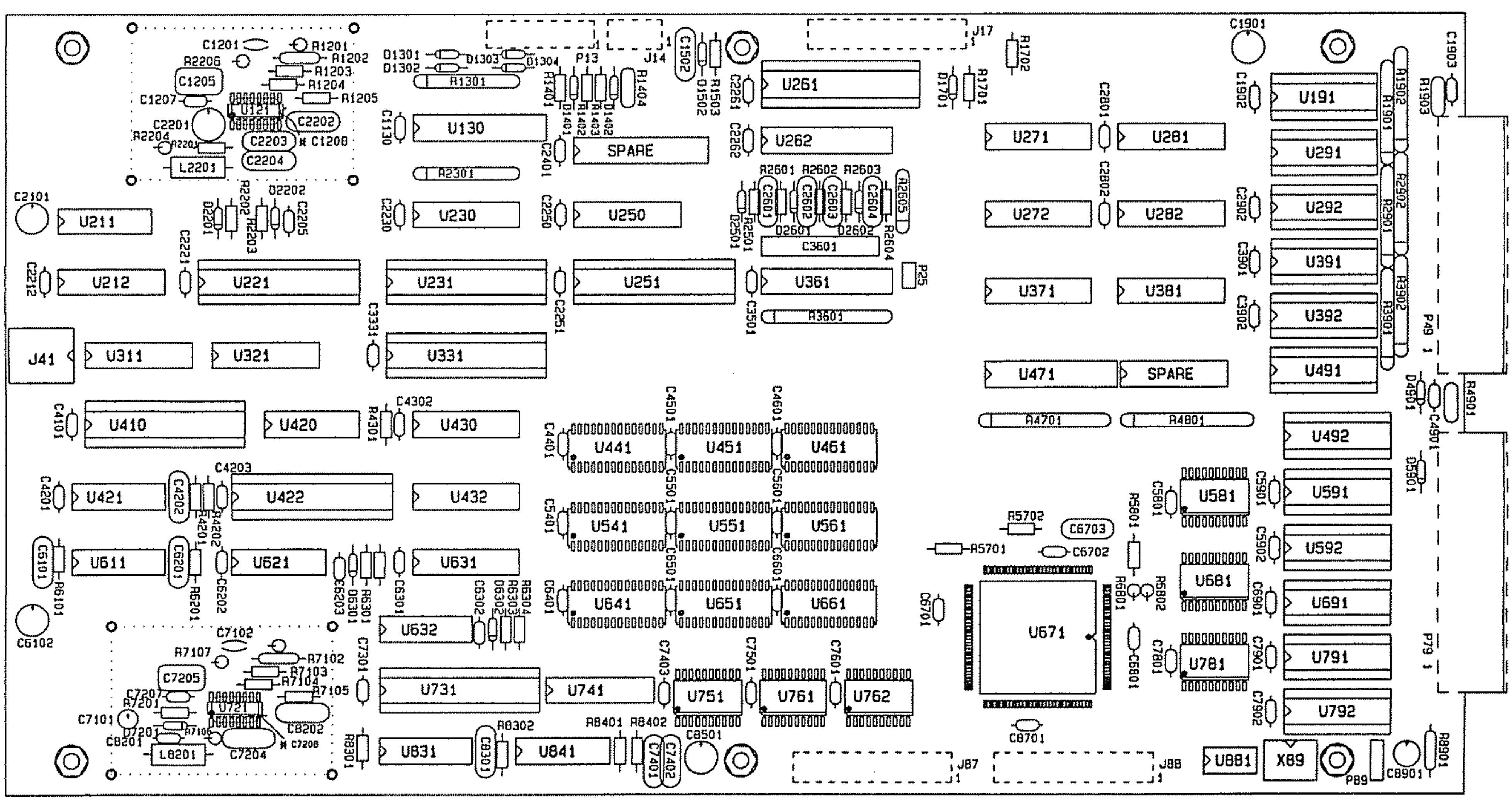
DIGITAL INPUT/OUTPUT OPTION 9DIO.2000 (6400.DIO2.1)



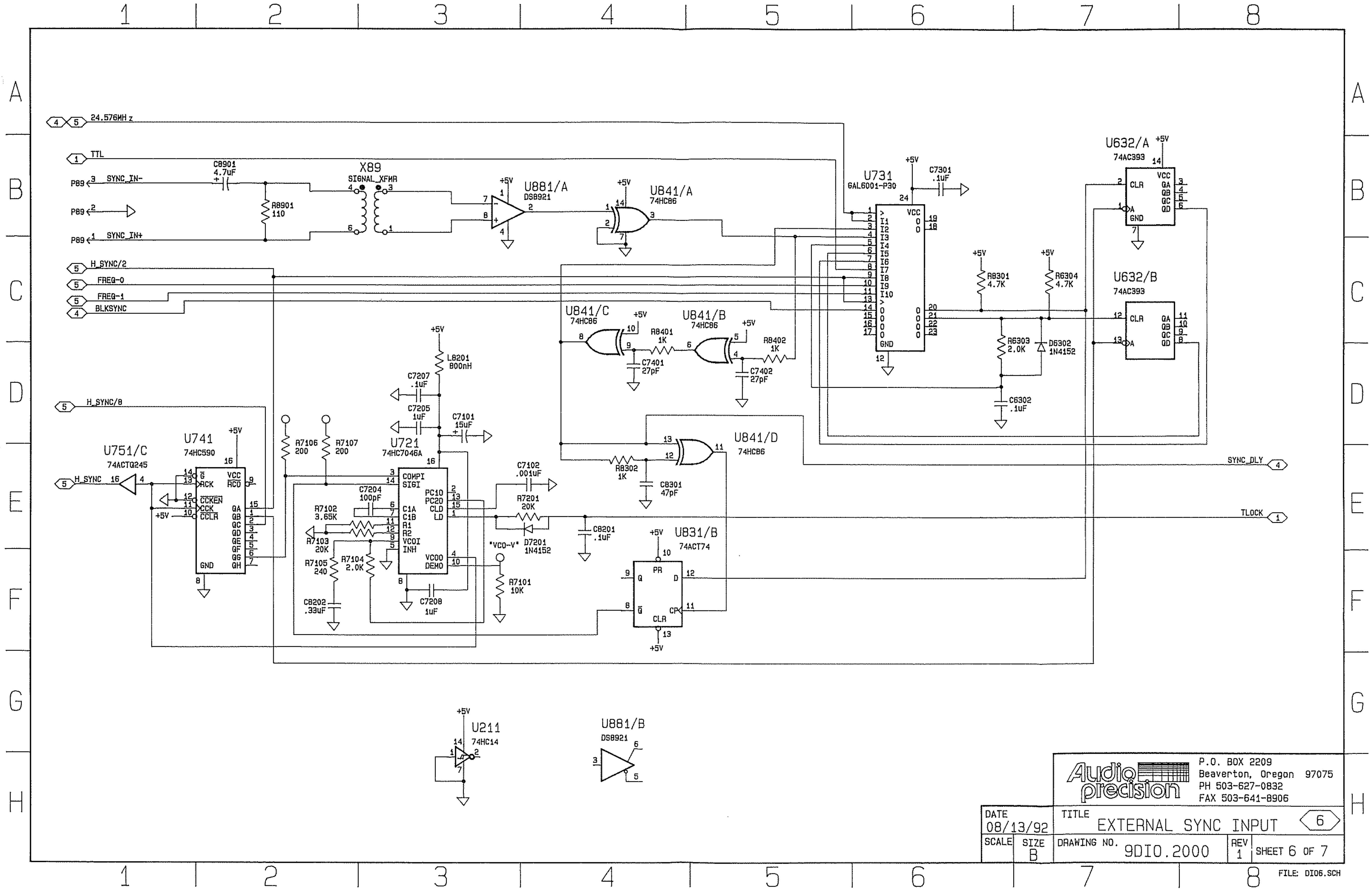
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 12/23/92
TITLE AES/EBU OUTPUT
5
SCALE
SIZE B
DRAWING NO. 9DIO.2000
REV 1
SHEET 5 OF 7

FILE: DIO5.SCH

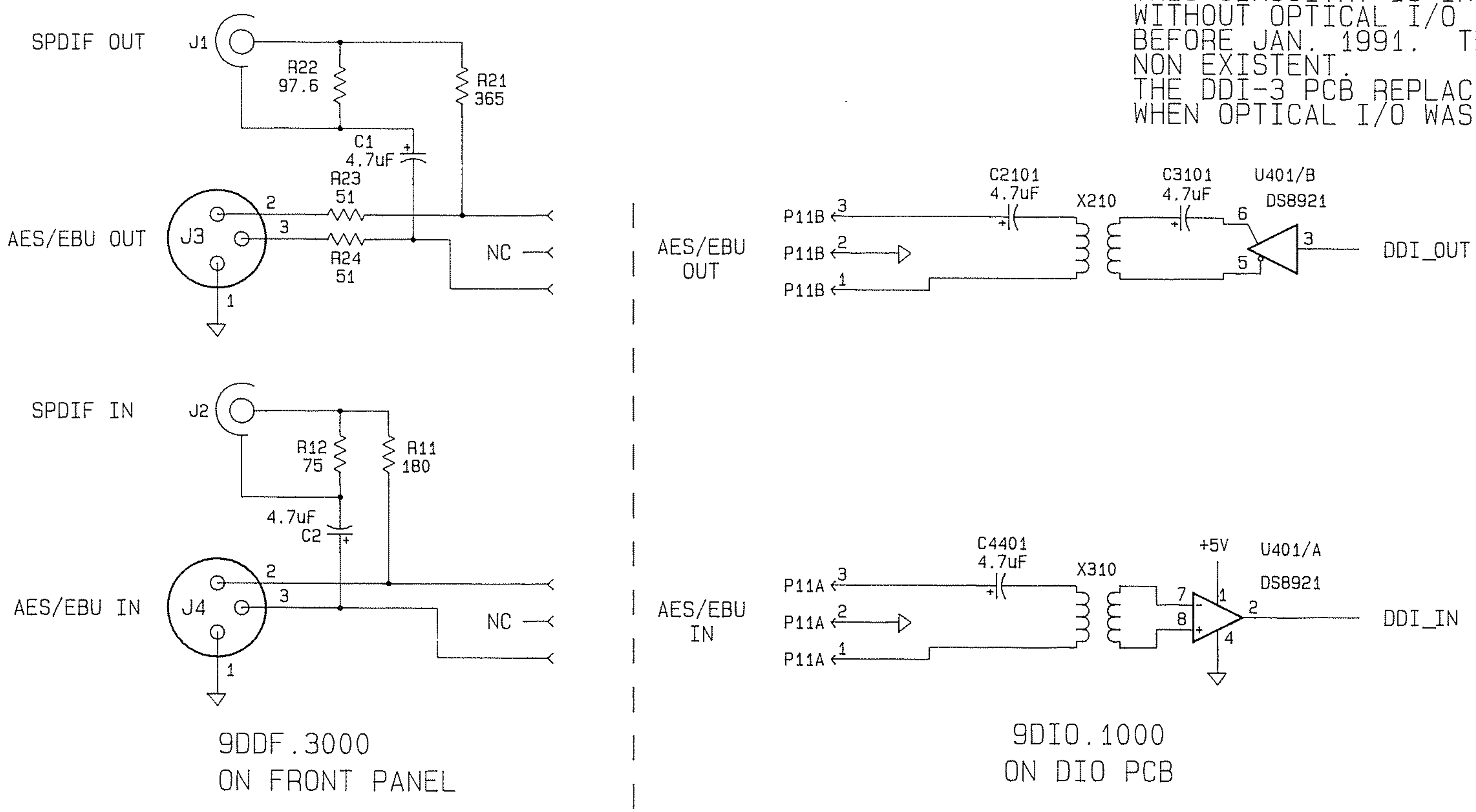


DIGITAL INPUT/OUTPUT OPTION 9DIO.2000 (6400.DIO2.1)


24.576MHz
TTL
SYNC_IN-
SYNC_IN+
P89
C8901 4.7uF
R8901 110
X89 SIGNAL_XFMR
U881/A DS8921
U841/A 74HC86
U731 GAL6001-P30
C7301 .1uF
U632/A 74AC393
U632/B 74AC393
H_SYNC/2
FREQ-0
FREQ-1
BLKSYNC
U841/C 74HC86
U841/B 74HC86
R8401 1K
R8402 1K
C7401 27pF
C7402 27pF
R8301 4.7K
R6304 4.7K
R6303 2.0K
D6302 1N4152
C6302 .1uF
H_SYNC/8
U751/C 74ACTQ245
H_SYNC
U741 74HC590
R7106 200
R7107 200
L8201 800nH
C7207 .1uF
C7205 1uF
C7101 15uF
U721 74HC7046A
C7204 100pF
R7102 3.65K
R7103 20K
R7105 240
R7104 2.0K
C8202 .33uF
C7208 1uF
C7102 .001uF
R7201 20K
D7201 1N4152
"VCO-V"
R7101 10K
C8201 .1uF
U841/D 74HC86
R8302 1K
C8301 47pF
SYNC_DLY
TLOCK
U831/B 74ACT74
U211 74HC14
U881/B DS8921
+5V
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 08/13/92
TITLE EXTERNAL SYNC INPUT
SCALE
SIZE B
DRAWING NO. 9DIO.2000
REV 1
SHEET 6 OF 7
FILE: DIO6.SCH

ECO#	SHEET#	DATE	APPROVAL

NOTE:
THIS CIRCUITRY IS INCLUDED IN UNITS WITHOUT OPTICAL I/O AND MANUFACTURED BEFORE JAN. 1991. THE DDI-3 PCB IS NON EXISTENT.
THE DDI-3 PCB REPLACED THIS CIRCUITRY WHEN OPTICAL I/O WAS INTRODUCED.

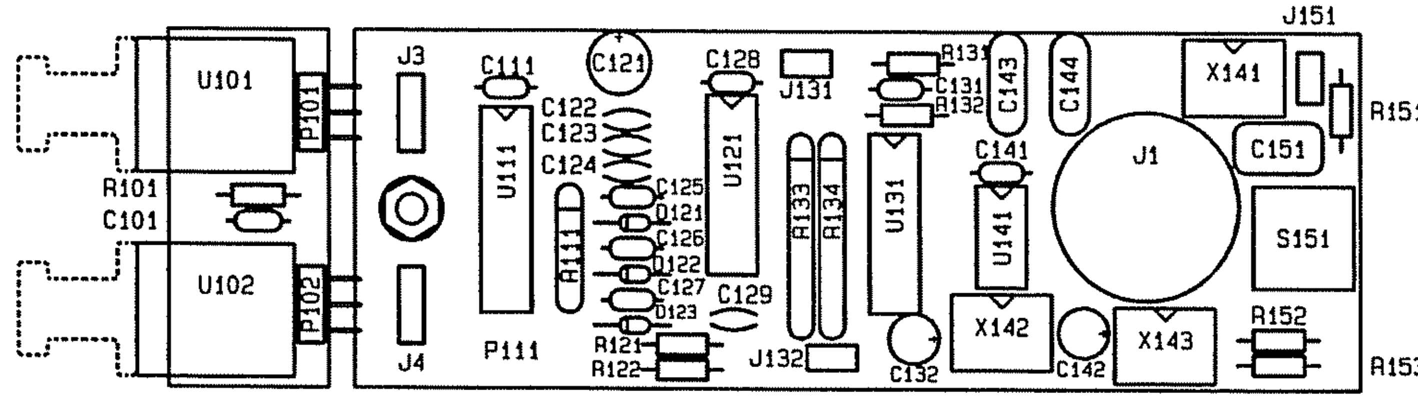


(UNITS MANUFACTURED BEFORE JANUARY 1991)

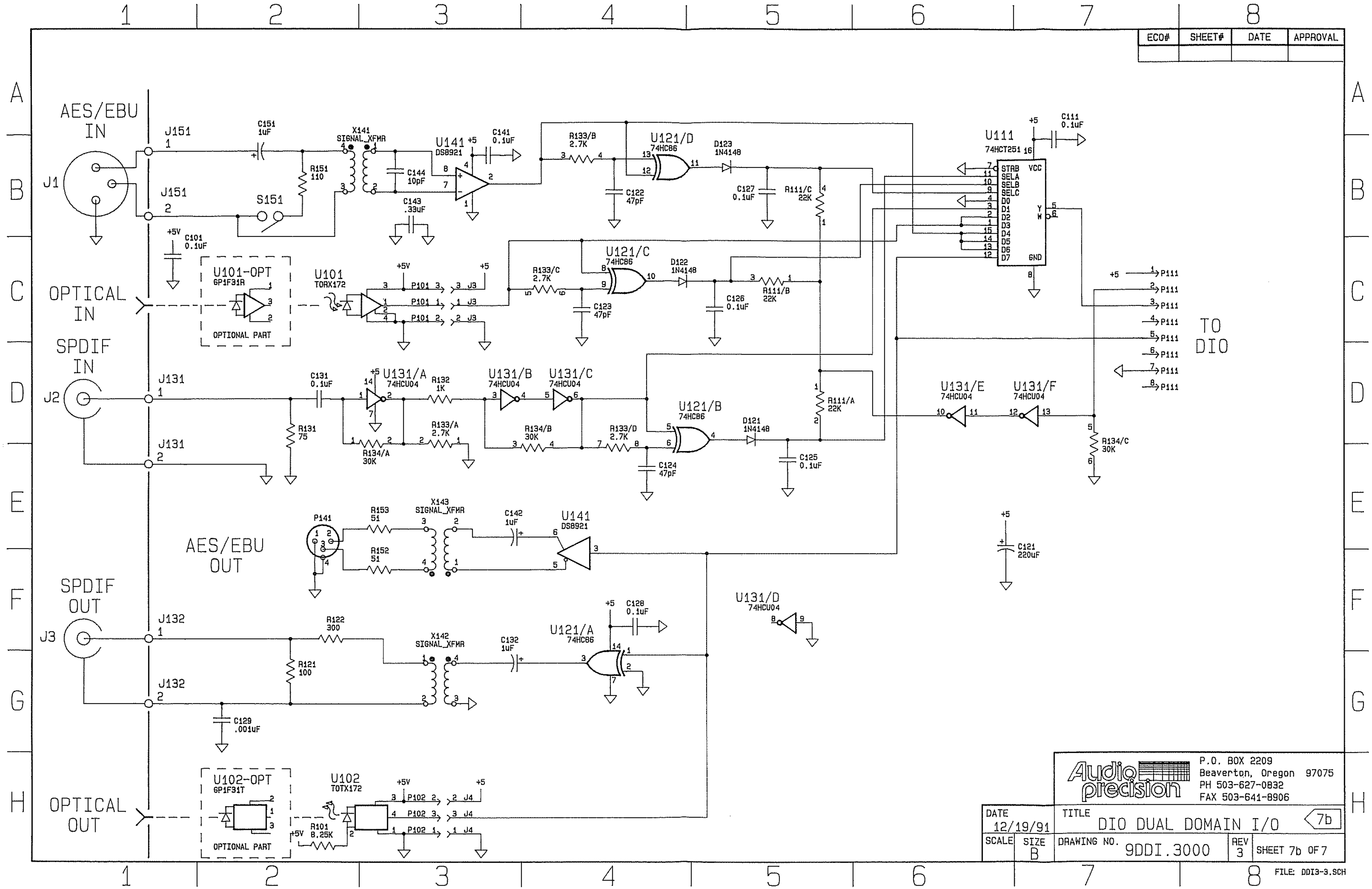
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 12/19/91	TITLE DIO DUAL DOMAIN I/O	7a
SCALE / SIZE B	DRAWING NO. 9DDF.3000	REV 1 / SHEET 7a OF 7

FILE: DDF.SCH



DUAL DOMAIN INTERFACE 9DDI.3000 (6200.DDI3.3)


ECO#
SHEET#
DATE
APPROVAL
AES/EBU IN
J1
J151
C151 1uF
X141 SIGNAL_XFMR
U141 DS8921
C141 0.1uF
R151 110
C144 10pF
C143 .33uF
S151
+5V
C101 0.1uF
R133/B 2.7K
C122 47pF
U121/D 74HC86
D123 1N4148
C127 0.1uF
R111/C 22K
U111 74HCT251
C111 0.1uF
STRB
SELA
SELB
SELC
D0
D1
D2
D3
D4
D5
D6
D7
VCC
GND
OPTICAL IN
U101-OPT GP1F31R
OPTIONAL PART
U101 TORX172
P101
J3
R133/C 2.7K
C123 47pF
U121/C 74HC86
D122 1N4148
C126 0.1uF
R111/B 22K
P111
TO DIO
SPDIF IN
J2
J131
C131 0.1uF
R131 75
U131/A 74HCU04
R132 1K
R134/A 30K
R133/A 2.7K
U131/B 74HCU04
U131/C 74HCU04
R134/B 30K
R133/D 2.7K
C124 47pF
U121/B 74HC86
D121 1N4148
C125 0.1uF
R111/A 22K
U131/E 74HCU04
U131/F 74HCU04
R134/C 30K
AES/EBU OUT
P141
R153 51
R152 51
X143 SIGNAL_XFMR
C142 1uF
U141 DS8921
C121 220uF
SPDIF OUT
J3
J132
R122 300
R121 100
X142 SIGNAL_XFMR
C132 1uF
U121/A 74HC86
C128 0.1uF
U131/D 74HCU04
C129 .001uF
OPTICAL OUT
U102-OPT GP1F31T
OPTIONAL PART
U102 TOTX172
R101 8.25K
P102
J4
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 12/19/91
TITLE DIO DUAL DOMAIN I/O
7b
SCALE
SIZE B
DRAWING NO. 9DDI.3000
REV 3
SHEET 7b OF 7
FILE: DDI3-3.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1130	4A2	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	4F5	2172.0102	CAP CERAM 100V 20%	.001uF
C1205	4F5	2454.0105	CAP POLYE 50V 5%	1uF
C1207	4F5	2172.0104	CAP CERAM 100V 20%	.1uF
C1208	4H5	2454.0105	CAP POLYE 50V 5%	1uF
C1502	5C1	2294.0270	CAP MICA 500V 5%	27pF
C1901	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1902	3D8	2172.0104	CAP CERAM 100V 20%	.1uF
C1903	3G7	2172.0104	CAP CERAM 100V 20%	.1uF
C2101	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2201	4F5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2202	4H4	2454.0334	CAP POLYE 50V 5%	.33uF
C2203	4G4	2296.0101	CAP MICA 500V 1%	100pF
C2204	4H4	2294.0270	CAP MICA 500V 5%	27pF
C2205	4G6	2172.0104	CAP CERAM 100V 20%	.1uF
C2212	5G3	2172.0104	CAP CERAM 100V 20%	.1uF
C2221	4A4	2172.0104	CAP CERAM 100V 20%	.1uF
C2230	4F2	2172.0104	CAP CERAM 100V 20%	.1uF
C2250	5A2	2172.0104	CAP CERAM 100V 20%	.1uF
C2251	5C2	2172.0104	CAP CERAM 100V 20%	.1uF
C2261	4D7	2172.0104	CAP CERAM 100V 20%	.1uF
C2262	1H5	2172.0104	CAP CERAM 100V 20%	.1uF
C2401	4F3	2172.0104	CAP CERAM 100V 20%	.1uF
C2601	3G4	2294.0270	CAP MICA 500V 5%	27pF
C2602	3B4	2294.0270	CAP MICA 500V 5%	27pF
C2603	3F7	2294.0270	CAP MICA 500V 5%	27pF
C2604	3C4	2294.0270	CAP MICA 500V 5%	27pF
C2801	1F5	2172.0104	CAP CERAM 100V 20%	.1uF
C2802	1D5	2172.0104	CAP CERAM 100V 20%	.1uF
C2902	3A8	2172.0104	CAP CERAM 100V 20%	.1uF
C3331	5C4	2172.0104	CAP CERAM 100V 20%	.1uF
C3501	1B6	2172.0104	CAP CERAM 100V 20%	.1uF
C3601	5E1,5E2	2051.8102	CAP CERNET SIP +80/-20%	.001u
C3901	3E6	2172.0104	CAP CERAM 100V 20%	.1uF
C3902	3C6	2172.0104	CAP CERAM 100V 20%	.1uF
C4101	4C3	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	4C2	2172.0104	CAP CERAM 100V 20%	.1uF
C4202	4D5	2294.0270	CAP MICA 500V 5%	27pF
C4203	4D6	2172.0104	CAP CERAM 100V 20%	.1uF
C4302	5E3	2172.0104	CAP CERAM 100V 20%	.1uF
C4401	2E8	2172.0104	CAP CERAM 100V 20%	.1uF
C4501	2B8	2172.0104	CAP CERAM 100V 20%	.1uF
C4601	2B4	2172.0104	CAP CERAM 100V 20%	.1uF
C4901	3D5	2172.0104	CAP CERAM 100V 20%	.1uF
C5401	2E7	2172.0104	CAP CERAM 100V 20%	.1uF
C5501	2B7	2172.0104	CAP CERAM 100V 20%	.1uF
C5601	2B3	2172.0104	CAP CERAM 100V 20%	.1uF
C5801	1G2	2172.0104	CAP CERAM 100V 20%	.1uF
C5901	3DB	2172.0104	CAP CERAM 100V 20%	.1uF
C5902	3B3	2172.0104	CAP CERAM 100V 20%	.1uF
C6101	4F4	2294.0470	CAP MICA 500V 5%	47pF
C6102	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF

Replaceable Electrical Parts List: 9DIO.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C6201	4D4	2294.0270	CAP MICA 500V 5%	27pF
C6202	4E7	2172.0104	CAP CERAM 100V 20%	.1uF
C6203	4E5	2172.0104	CAP CERAM 100V 20%	.1uF
C6301	1E7	2172.0104	CAP CERAM 100V 20%	.1uF
C6302	6D6	2172.0104	CAP CERAM 100V 20%	.1uF
C6401	2E5	2172.0104	CAP CERAM 100V 20%	.1uF
C6501	2B5	2172.0104	CAP CERAM 100V 20%	.1uF
C6601	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C6701	5E7	2172.0104	CAP CERAM 100V 20%	.1uF
C6702	5D5	2172.0104	CAP CERAM 100V 20%	.1uF
C6703	5G2	2294.0270	CAP MICA 500V 5%	27pF
C6801	5D6	2172.0104	CAP CERAM 100V 20%	.1uF
C6901	3E2	2172.0104	CAP CERAM 100V 20%	.1uF
C7101	6E3	2832.0156	CAP TA-EL 25V 20%	15uF
C7102	6E4	2172.0102	CAP CERAM 100V 20%	.001uF
C7204	6E3	2296.0101	CAP MICA 500V 1%	100pF
C7205	6E3	2454.0105	CAP POLYE 50V 5%	1uF
C7207	5D3	2172.0104	CAP CERAM 100V 20%	.1uF
C7208	6F3	2454.0105	CAP POLYE 50V 5%	1uF
C7301	6B6	2172.0104	CAP CERAM 100V 20%	.1uF
C7401	6D4	2294.0270	CAP MICA 500V 5%	27pF
C7402	6D5	2294.0270	CAP MICA 500V 5%	27pF
C7403	2G3	2172.0104	CAP CERAM 100V 20%	.1uF
C7501	1B2	2172.0104	CAP CERAM 100V 20%	.1uF
C7601	1A2	2172.0104	CAP CERAM 100V 20%	.1uF
C7801	1D2	2172.0104	CAP CERAM 100V 20%	.1uF
C7901	3C2	2172.0104	CAP CERAM 100V 20%	.1uF
C7902	3B2	2172.0104	CAP CERAM 100V 20%	.1uF
C8201	6E4	2172.0104	CAP CERAM 100V 20%	.1uF
C8202	6F2	2454.0334	CAP POLYE 50V 5%	.33uF
C8301	6E4	2294.0470	CAP MICA 500V 5%	47pF
C8501	2H5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C8701	5B7	2172.0104	CAP CERAM 100V 20%	.1uF
C8901	6B2	2942.0475	CAP AL-EL 35V 20%	4.7uF
D1301	4C7	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D1302	5C8	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D1303	4C7	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D1304	5B8	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D1401	4C7	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D1402	4C7	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D1502	5C2	3120.0000	DIODE SCHOTTKY	1SS97
D1701	5F2	3120.0000	DIODE SCHOTTKY	1SS97
D2201	4B4	3130.0047	DIODE ZEN 1/2W 5% 4.7V	1N750
D2202	4G5	3110.4152	DIODE SIGNAL	4152
D2501	1C6	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D2601	3G4	3120.0000	DIODE SCHOTTKY	1SS97
D2602	3F8	3120.0000	DIODE SCHOTTKY	1SS97
D4901	3B5	3120.0000	DIODE SCHOTTKY	1SS97
D5901	3C5	3120.0000	DIODE SCHOTTKY	1SS97
D6301	4E5	3120.0000	DIODE SCHOTTKY	1SS97
D6302	6D7	3110.4152	DIODE SIGNAL	4152
D7201	6E4	3110.4152	DIODE SIGNAL	4152

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
J14	1F1,1G1	4221.1008	JACK PC 2 X .1	8 PIN
J17	1G1,1H1,4E8,4F8, 5A1-5H1,5F8,5G7	4221.1024	JACK PC 2 X .1	24 PIN
J41	4D8,5F1	4151.0905	CABLE ASSY .05RBN/DIP	9" 5 CND
J87	1A1-1C1,1H1,2D1, 2G1,5H1	4221.1024	JACK PC 2 X .1	24 PIN
J88	1D1-1H1	4221.1024	JACK PC 2 X .1	24 PIN
L2201	4F5	4510.0801	INDUCTOR 10 OHM	800nH
L8201	6D3	4510.0801	INDUCTOR 10 OHM	800nH
P13	4B4-4D8,5B8-5E8	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P25	1B8	4221.0036	PLUG PC .1 X.43	36 PIN
P49	3B7-3F7,3A8-3G8	4221.0134	PLUG PC 90' SHROUDED	34 PIN
P79	3B1-3F1,3B6-3E6	4221.0134	PLUG PC 90' SHROUDED	34 PIN
P89	6B1	4221.0036	PLUG PC.1 X.43	36 PIN
R1201	4G5	1214.0103	RES 1/4W C FLM 5%	10K
R1202	4G4	1136.3651	RES 1/8W M FLM 1%	3.65K
R1203	4G4	1214.0203	RES 1/4W C FLM 5%	20K
R1204	4G4	1214.0202	RES 1/4W C FLM 5%	2.0K
R1205	4G4	1214.0241	RES 1/4W C FLM 5%	240
R1301	4C7,5B8-5D8	1984.4221	RES NET SIP 5% I	4 X 220
R1401	4C8	1214.0220	RES 1/4W C FLM 5%	22
R1402	4C8	1214.0203	RES 1/4W C FLM 5%	20K
R1403	4C7	1214.0241	RES 1/4W C FLM 5%	240
R1404	4B7	1061.0601	RES PTC CERAM 18V	600mA
R1503	5C1	1214.0101	RES 1/4W C FLM 5%	100
R1701	5G8	1214.0103	RES 1/4W C FLM 5%	10K
R1702	5G8	1214.0103	RES 1/4W C FLM 5%	10K
R1901	3D8,3E8	1984.4220	RES NET SIP 5% I	4 X 22
R1902	3C8-3F8	1984.4220	RES NET SIP 5% I	4 X 22
R1903	3F7	1061.0601	RES PTC CERAM 18V	600mA
R2201	4G4	1214.0201	RES 1/4W C FLM 5%	200
R2202	4B5	1214.0241	RES 1/4W C FLM 5%	240
R2203	4G5	1214.0203	RES 1/4W C FLM 5%	20K
R2204	4G3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R2206	4H4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R2301	4C5,5B8	1984.4220	RES NET SIP 5% I	4 X 22
R2501	1B6	1214.0220	RES 1/4W C FLM 5%	22
R2601	3G4	1214.0241	RES 1/4W C FLM 5%	240
R2602	3B4	1214.0241	RES 1/4W C FLM 5%	240
R2603	3F8	1214.0241	RES 1/4W C FLM 5%	240
R2604	3C4	1214.0241	RES 1/4W C FLM 5%	240
R2605	3B5,3C5,3G4,3F8	1985.4223	RES NET SIP 2% B	4 X 22K
R2901	3F6	1984.4220	RES NET SIP 5% I	4 X 22
R2902	3E6,3F6,3B8	1984.4220	RES NET SIP 5% I	4 X 22
R3601	3G1,3H1	1984.9104	RES NET SIP 5% B	9 X 100K
R3901	3B6,3D6	1984.4220	RES NET SIP 5% I	4 X 22
R3902	3B6-3D6	1984.4220	RES NET SIP 5% I	4 X 22
R4201	4D5	1214.0102	RES 1/4W C FLM 5%	1K
R4202	4E6	1214.0474	RES 1/4W C FLM 5%	470K
R4301	453	1214.0103	RES 1/4W C FLM 5%	10K
R4701	3G3,3H3	1984.9104	RES NET SIP 5% B	9 X 100K
R4801	3G2,3H2	1984.9104	RES NET SIP 5% B	9 X 100K

Replaceable Electrical Parts List: 9DIO.2000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R4901	3D4	1061.0601	RES PTC CERAM 18V	600mA
R5701	5H6	1214.0101	RES 1/4W C FLM 5%	100
R5702	4C4	1214.0470	RES 1/4W C FLM 5%	47
R5801	5E5	1214.0101	RES 1/4W C FLM 5%	100
R6101	4E3	1214.0102	RES 1/4W C FLM 5%	1K
R6201	4D4	1214.0102	RES 1/4W C FLM 5%	1K
R6301	4E5	1214.0202	RES 1/4W C FLM 5%	2.0K
R6302	4E6	1214.0474	RES 1/4W C FLM 5%	470K
R6303	6C6	1214.0202	RES 1/4W C FLM 5%	2.0K
R6304	6C7	1214.0472	RES 1/4W C FLM 5%	4.7K
R6801	5E5	1214.0201	RES 1/4W C FLM 5%	200
R6802	5D5	1214.0201	RES 1/4W C FLM 5%	200
R7101	6F3	1214.0103	RES 1/4W C FLM 5%	10K
R7102	6E2	1136.3651	RES 1/8W M FLM 1%	3.65K
R7103	6E2	1214.0203	RES 1/4W C FLM 5%	20K
R7104	6F2	1214.0202	RES 1/4W C FLM 5%	2.0K
R7105	6F2	1214.0241	RES 1/4W C FLM 5%	240
R7106	6E2	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R7107	6E2	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R7201	6E4	1214.0203	RES 1/4W C FLM 5%	20K
R8301	6C6	1214.0472	RES 1/4W C FLM 5%	4.7K
R8302	6E4	1214.0102	RES 1/4W C FLM 5%	1K
R8401	6D4	1214.0102	RES 1/4W C FLM 5%	1K
R8402	6D5	1214.0102	RES 1/4W C FLM 5%	1K
R8901	6B2	1136.1100	RES 1/8W M FLM 1%	110
U121	4F5	3323.7046.1	PHASE LOCK LOOP SMD	74HC7046A
U130	4B7,4C7,5G3,5A8-5D8	3326.0244	BUFFER 8X TRI-STATE	74ACT244
U191	3E7	3325.0670	REGISTER FILE 4X4	74AC670
U211	4B1,4G1,5D3,5G2,66H3	3323.0014	TRIGGER SCHMITT 8X	74HC14
U212	4A2	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U221	4A4	3342.20V8	GENERIC ARRAY	GAL20V8-15
U230	2F2	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U231	5E4	3342.20V8	GENERIC ARRAY	GAL20V8-15
U250	5A2	3324.0251	MULTIPLEXER TRI-ST	74HCT251
U251	5C2	3342.20V8	GENERIC ARRAY	GAL20V8-15
U261	4D7	3342.20V8	GENERIC ARRAY	GAL20V8-15
U262	1A5,1B6,1B7,1H5, 3A4-3G4,3F7	3326.0244	BUFFER 8X TRI-STATE	74ACT244
U271	1B3	3325.0670	REGISTER FILE 4X4	74AC670
U272	1D3	3325.0670	REGISTER FILE 4X4	74AC670
U281	1F4	3325.0670	REGISTER FILE 4X4	74AC670
U282	1D4	3325.0670	REGISTER FILE 4X4	74AC670
U291	3C7	3325.0670	REGISTER FILE 4X4	74AC670
U292	3A7	3325.0670	REGISTER FILE 4X4	74AC670
U311	5C3	3325.0163	COUNTER 4-BIT BIN/DEC	74AC163
U321	5A3	3325.0163	COUNTER 4-BIT BIN/DEC	74AC163
U331	5C4	3723.7225	PROM CMOS 25ns	512 X 8
U361	1C6	3326.0794	REGISTER 8X W/READBK	74ACT794
U371	1F3	3325.0670	REGISTER FILE 4X4	74AC670
U381	1B4	3325.0670	REGISTER FILE 4X4	74AC670
U391	3E6	3325.0670	REGISTER FILE 4X4	74AC670
U392	3D6	3325.0670	REGISTER FILE 4X4	74AC670

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U410	4D3	3342.20V8	GENERIC ARRAY	GAL20V8-15
U420	4E4,4A5	3326.0074	FLIP-FLOP 2X D	74ACT74
U421	4C2	3323.0164	SHFT REG SERIAL-PARA	74HC164
U422	4D6	3342.20V8	GENERIC ARRAY	GAL20V8-15
U430	5E3	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U432	1F6	3326.0138	DECODER 3-LN/8-LN	74ACT138
U441	2E8	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U451	2B8	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U461	2B4	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U471	1D6	3326.0794	REGISTER 8X W/READBK	74ACT794
U491	3B6	3325.0670	REGISTER FILE 4X4	74AC670
U492	3E3	3326.0670	REGISTER FILE 4X4	74ACT670
U541	2E6	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U551	2B7	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U561	2B3	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U581	1G2	3326.0245.1	TRANSCVR 8X 3-ST SMD	74ACTQ245
U591	3D3	3326.0670	REGISTER FILE 4X4	74ACT670
U592	3B3	3326.0670	REGISTER FILE 4X4	74ACT670
U611	4D4,4D5,4E4	3323.0086	GATE 4-IN EXCL OR	74HC86
U621	4E7,4F7	3325.0393	COUNTER 2 X 4-BIT BIN	74AC393
U631	1F7	3326.0138	DECODER 3-LN/8-LN	74ACT138
U632	6B7,6C7	3325.0393	COUNTER 2 X 4-BIT BIN	74AC393
U641	2E5	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U651	2B5	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U661	2B2	3722.5256.2	SRAM CMOS 35ns SMD	32K X 8
U671	5B6-5F6	3331.5600.1	uPROCESSOR SMD	DSP56001
U681	1F2	3326.0245.1	TRANSCVR 8X 3-ST SMD	74ACTQ245
U691	3E2	3326.0670	REGISTER FILE 4X4	74ACT670
U721	6E3	3323.7046.1	PHASE LOCK LOOP SMD	74HC7046A
U731	6B6	3342.20V8	GENERIC ARRAY	GAL20V8-15
U741	6E1	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U751	1A3,2E2,2H2.2H3,6E1	3326.0245.1	TRANSCVR 8X 3-ST SMD	74ACTQ245
U761	1C2	3326.0245.1	TRANSCVR 8X 3-ST SMD	74ACTQ245
U762	1A2	3326.0245.1	TRANSCVR 8X 3-ST SMD	74ACTQ245
U781	1D2	3326.0245.1	TRANSCVR 8X 3-ST SMD	74ACTQ245
U791	3C2	3326.0670	REGISTER FILE 4X4	74ACT670
U792	3B2	3326.0670	REGISTER FILE 4X4	74ACT670
U831	3F5,6F4	3326.0074	FLIP-FLOP 2X D	74ACT74
U841	6B4,6C4,6E5	3323.0086	GATE 4-IN EXCL OR	74HC86
U881	6B3,6H4	3333.8921	RS-422 DIFF TRANSCVR	DS8921
X89	6B3	4521.0011	TRANSFORMER SIGNAL DIP	100MHz

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C101	1B2	2172.0104	CAP CERAM 100V 20%	.1uF
C111	1A7	2172.0104	CAP CERAM 100V 20%	.1uF
C121	1E7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C122	1B4	2172.0104	CAP CERAM 100V 20%	.1uF
C123	1C4	2172.0470	CAP CERAM 100V 20%	47pF
C124	1D4	2172.0470	CAP CERAM 100V 20%	47pF
C125	1D5	2172.0470	CAP CERAM 100V 20%	47pF
C126	1C5	2172.0104	CAP CERAM 100V 20%	.1uF
C127	1B5	2172.0104	CAP CERAM 100V 20%	.1uF
C128	1F4	2172.0104	CAP CERAM 100V 20%	.1uF
C129	1G2	2172.0102	CAP CERAM 100V 20%	.001uF
C131	1D2	2172.0104	CAP CERAM 100V 20%	.1uF
C132	1F4	2952.0105	CAP AL-EL 50V 20%	1uF
C141	1A4	2172.0104	CAP CERAM 100V 20%	.1uF
C142	1F4	2952.0105	CAP AL-EL 50V 20%	1uF
C143	1B2	2454.0334	CAP POLYE 50V 5%	.33uF
C144	1A3	2454.0105	CAP MICA 500V 5%	10pF
C151	1A2	2454.0223	CAP POLYE 50V 5%	.022uF
D121	1D5	3110.4152	DIODE SIGNAL	4152
D122	1C5	3110.4152	DIODE SIGNAL	4152
D123	1A5	3110.4152	DIODE SIGNAL	4152
P101	1C3	4221.0136	PLUG PC 90' .1 X.39	36 PIN
P102	1H3	4221.0136	PLUG PC 90' .1 X.39	36 PIN
P111	1C8	4221.0036	PLUG PC .1 X.43	36 PIN
P141	1E2	4253.0001	JACK XLR PNL MT	MALE
R111	1B5,1C5,1D5	1985.4223	RES NET SIP 2% B	4 X 22K
R121	1F2	1214.0101	RES 1/4W C FLM 5%	100
R122	1F2	1214.0301	RES 1/4W C F;M 5%	300
R131	1D2	1214.0750	RES 1/4W C FLM 5%	75
R132	1D3	1214.0102	RES 1/4W C FLM 5%	1K
R133	1A4,1B4,1C4,1D3	1984.4272	RES NET SIP 5% I	4 X 2.7K
R134	1D7,1D3,1D4	1984.4303	RES NET SIP 5% I	4 X 30K
R141	1E4	1214.0222	RES 1/4W C FLM 5%	2.2K
R151	1A2	1136.1240	RES 1/8W M FLM 1%	124
R152	1E3	1214.0510	RES 1/4W C FLM 5%	51
R153	1E3	1214.0510	RES 1/4W C FLM 5%	51
S151	1B2	4321.0003	SWITCH PUSH VERT	DPDT
U101	1C2,1C3	3640.0031	OPTICAL INTERFACE SPDIF	REC
U102	1H2,1H3	3640.0131	OPTICAL INTERFACE SPDIF	XMT
U111	1A7	3324.0251	MULTIPLEXER TRI-ST	74HCT251
U121	1A5,1B4,1D5,1F4	3323.0086	GATE 4-IN EXCL OR	74HC86
U131	1D6,1D7,1F5,1D4	3327.0004	BUFFER 6X INV UNBUFF	74HCU04
U141	1A3,1D3,1E4,1F5	3333.8921	RS-422 DIFF TRANSCVR	DS8921
X141	1A3	4521.0011	TRANSFORMER SIGNAL DIP	100MHz
X142	1F3	4521.0011	TRANSFORMER SIGNAL DIP	100MHz
X143	1E3	4521.0011	TRANSFORMER SIGNAL DIP	100MHz

SECTION 5
ACCESSORY CIRCUIT DESCRIPTIONS, SCHEMATICS, & ELECTRICAL PARTS LISTS

This section contains schematics, circuit descriptions, and electrical parts lists for the SWR-122, DCX-127, and the SIA-322 accessories. All information is believed to be accurate as of the publication date, however Audio Precision reserves the right to make changes without prior notice. If a component value differs from that shown on the schematics use the value of the existing component for replacement purposes, or contact Audio Precision.

COMPONENT AND ASSEMBLY DESIGNATIONS

A	Assembly
BT	Battery
C	Capacitor, fixed or variable
D	Diode
E	Socket or mechanical part
F	Fuse
H	Heat sink or radiator
HS	Heatsink or mounting hardware
J	Connector, female
K	Relay
L	Inductor, fixed or variable
P	Connector, male
Q	Transistor, FET, or SCR
R	Resistor, fixed or variable
S	Switch or contact
TP	Test Point
U	Integrated Circuit
W	Wirestrap or Cable
X	Transformer
Y	Crystal

SPECIAL SCHEMATIC SYMBOLS

SWR-122 SWITCHER FAMILY

SWR-122, SWITCHER FAMILY

Versions

The Audio Precision SWR-122 family is available in four versions: the input switcher (**SWR-122F**), the output switcher (**SWR-122M**), the patch point switcher (**SWR-122P**), and the terminal strip switcher (**SWR-122T**). All use the same circuit board and switching circuitry but differ in connectors, panels, and jumper positions. The jumper position differences are covered in the accompanying discussion of configuring an SWR-122T for each of the other three versions.

Logic and Interface <1>

The digital information from the host computer is routed through the switcher via 25-pin D-subminiature connectors P51 and J41. All signals are looped from one jack to the next, whether or not they are used in the switcher.

The data/address lines are filtered by resistor/capacitor lowpass networks which reduce susceptibility to RFI and intersignal interference. Their outputs are buffered by Schmitt trigger octal buffer U421. This buffered address and data information drives the address decoding circuitry consisting of U611 and U521. It also drives the high-nibble / low-nibble selectors U523 and U522. In older units this selection was performed with jumpers P521 through P528.

The lower four bits (which represent the switcher address) are compared to the settings of the rear panel DIP switch (S61) by four bit magnitude comparator U611. When the bit patterns match and bit 7 is high the output (pin 6) of U611 will go high. This drives the enable input of a 3-to-8 line decoder U521. The select inputs are driven from bits 4, 5, and 6. The outputs of the decoder will therefore respond to address 14 and address 15 on the Audio Precision bus.

The address strobe line EA is filtered by R4203 and C4202 and buffered/inverted by U431. The output of this buffer is normally high and strobes low to latch valid address information. This latching is performed by flip-flop U623A and U623B. When operating as an input or output switcher the jumpers P622 and P621 are connected as shown in the schematic. One of the flip-flops latches Channel A information and the other latches Channel B information. When used as a patch point switcher these jumpers are removed and one is placed between the two D inputs of U623 (pins 2 and 12). The two sections of switch S61 are then used to select the patch point switcher between Channel A and Channel B. The /Q outputs of U623 will be high when the corresponding address has been written to the switcher. This will turn on pulling the /ATT line and telling the host computer that the switcher has responded to its address. The Q outputs will go low, enabling U622A and U622B.

When the write strobe EW is pulsed high by the host computer to write data it is filtered by R4204 and C4203. U431A buffers and inverts this signal, driving NOR gates U622A and U622B. These gates will go high when both inputs are low, or when the correct address has been latched by U623 and the write strobe pulses. This high going pulse drives U532 and U531, latching the data present at their inputs. These ICs are 4-bit latches and 4-to-16 line decoders in one package. Their outputs go to the relay drive transistors on the schematic <2>. Input data is supplied by the 4-bit data selectors U523 and U522 mentioned earlier. These are arranged to select between the upper and lower four bits of the data word. The selection is programmed by jumpers P522 and P521. In older units this selection was accomplished directly with eight jumpers P521 through P528. The upper four bits of the data byte are used to select the channel for an output switcher, the lower four bits are used to select the channel for an input switcher. For an input switcher the jumpers are set to select the low order bits to both latch/decoders. For an output switcher the jumpers are set to select the high order bits to both latch/decoders. A patch point switcher selects the high order bits to U532 and the lower order bits to U531.

When power is first applied to the circuit C6301, D6301 and R6301 provide a power on reset pulse through NOR gate U622D. The host computer may also generate a reset pulse by strobing ERST which drives the other input of the NOR gate. The low going pulse from U622D presets the address latches U623 and also presets U621. Dual flip-flop U621 holds latch/decoders U532 and U531 in the inhibit state until they are written to. The write strobe from U622A and U622B clocks the outputs of U621 low, enabling the decoders. U622C senses when either half of U621 is in the preset state and pulls the PWR line low. This signals the host computer that a power failure has occurred and that data in the switcher is no longer valid.

Switching Matrix <2>

Schematic <2> illustrates the relay matrix circuitry for the SWR-122 switchers. The audio signal to and from the System One is routed through the connectors in the upper left corner of the schematic. All of the switcher versions have a two pair of connectors (J711/J712, J811/J812) for this application. One of each pair may be wired to the System One and the other used to connect to the next switcher in the system. On the input and output switchers these are also wired to a pair of front panel connectors. These may be used for the System One connections, leaving the rear panel for switcher interconnect only.

From these connectors each signal passes through a double pole single throw relay to the 12-by-2 relay matrix. This serves to disconnect the switcher from the signal bus when none of the channels in the switcher are in use. The drive transistors for these relays are energized when none of the channels in the switcher are used. The relay matrix which routes the two signals to and from the 12 channels is composed of 48 relays. Two relays are used in series for each crosspoint. The first shorts the connection between the relays to ground when they are not selected. This reduces crosstalk to the point where it is limited by connector to connector capacitance and stray capacitances on the circuit board. The 12-by-2 matrix requires 24 crosspoints for a total of 48 relays.

When configured as an input switcher the unit is simply a 12-by-2 crosspoint switch. Any one of the 12 outputs of the device under test may be routed to either of the two inputs of the System One. To select a crosspoint the appropriate B or A drive line from schematic <1> goes high. This turns on the drive transistor and closes the two relays for that crosspoint.

When configured as an output switcher the unit operates as described for the input switcher case above. However, an additional feature is provided called the "complement mode". When selected, it causes all of the numbered channels which are not connected to channel A to be connected to channel B. This is useful for crosstalk testing whereby all inputs of a device under test may be driven simultaneously except the one being tested for crosstalk. It is connected to the channel A generator output which is turned off. This mode is enabled by setting channel B to 14. This sets pin 16 of U531 high, via R4301 driving the inverter U431C low. This low level enables the 12 inverters on U532's output. These inverters apply the inverse of the channel A programming to the channel B drive transistors via a second set of base resistors. When the unit is configured as an input switcher this mode is defeated by D4301 shorting the enable signal to the input of U431C. The software also locks this mode out.

In the patch point switcher the numbered channel connectors are a 5-pin male XLR. Two pins are used for the signal from the device under test and two are used for the signal to the device under test. The channel A bus is used for the input signal bus to the System One. The channel B bus is used for output signals from the System One. Using channel 12 as an example, when it is not selected relay K271 connects the terminals on the XLR together. This allows the circuit under test to operate normally. When one of the channel A (input) crosspoints is selected the signal at the patch point is routed to the System One input without disturbing the device under test. When one of the channel B (output) crosspoints is selected the patch point connection is broken and the device input is driven from the System One output.

Power Supply <3>

The power supply is a conventional full wave bridge rectifier design. U31 is a fixed +5 V regulator and contains integral short circuit and thermal overload protection. Its case is grounded, enabling direct connection to chassis. Reverse protection is provided by D2401. C3202 insures stability for all loads.

Note: The +5V regulator circuit in early production units was composed of a discrete zener plus a series pass compound darlington.

The primary of the power transformer is split into two sections to allow operation on 100-120V or 220-240V lines. Switch S11 configures the two windings in parallel or series, as appropriate. Fuse F31 guards against short circuits or excessive power draw.

Installation & Configuration of SWR122T Switchers

The Audio Precision SWR122T switchers may be set to any one of three possible configurations. These are:

(1) INPUT switcher which selects one of up to 192 different signals for routing to one of the two System One analyzer inputs. This switcher is designed to allow only one or two of the 192 input channels to drive the ANALYZER inputs.

(2) OUTPUT switcher which selects one of up to 192 different signals for routing to one of the two System One generator outputs. This switcher is designed to allow one, two or all of the 192 signals to be driven from one or both of the generator outputs.

(3) PATCH-POINT switcher allows insert patch points of audio systems or mixing consoles to be broken under program control and a signal inserted at that point. They can select one of the patch point receive connections to be driven from one channel of the generator output. Any one of the patch point send connections can be connected to one of the ANALYZER inputs. This version of switcher is essentially one half of an INPUT switcher and one half of an OUTPUT switcher in the same package. Rear panel rocker switches select whether the patch point switcher operates as CHANNEL A or CHANNEL B in the software.

Jumper Selection

Terminal strip switchers may be configured as any one of the above three switchers by setting the internal jumpers. There are four such jumpers on the board when shipped from the factory. They are diagrammed in Figures SWR122.1, SWR122.2, and SWR122.3.

The two jumpers marked I/O are located near the two 25-pin D-subminiature connectors on the rear panel. These select between INPUT and OUTPUT modes of the switcher. The input and output positions are marked above the two jumpers, input being away from the power transformer and output being toward the transformer.

The other two jumpers are located near the six position rocker switch assembly on the rear panel. They select whether the switcher responds to Channel A or Channel B commands. When both jumpers are side by side they bypass the rear panel A and B rocker switches. They must be in this position for the input or output versions of the switcher. This is the position they are shipped in from the factory. If a patch point switcher configuration is desired one of these jumpers must be removed and the other rotated 90 degrees and placed on the pair of pins closest to the 74HCT74 integrated circuit. With the jumper in this position the rear panel A and B rocker switches will select the desired channel for switcher operation.

Input/Output Connections

The connections to and from the device under test are made through the twelve terminal strips located near the front panel of the switcher. The wiring for these connectors is as follows:

1	high signal from device under test
2	low signal from device under test
3	ground
4	high signal to device under test input
5	low signal to device under test input

When used as an INPUT or OUTPUT switcher the corresponding XLR connections are as follows:

1	XLR Pin 2 (signal high)
2	XLR Pin 3 (signal low)
3	XLR Pin 1 (ground)
4	not used
5	not used

When the terminal strip switcher is shipped from the factory, pins 1 and 4 are connected together and pins 2 and 5 are connected together, on the circuit board itself. If the switcher is to be used as a PATCH POINT switcher the appropriate circuit board traces must be cut. Figure SWR122.4 shows how this is done. Once these traces are cut, operation as an INPUT or OUTPUT switcher will require wire jumpers to be inserted in the screw terminals between pins 1 and 4 and pins 2 and 5.

Connections to the System One and to the other switchers in the system are made via the XLR connectors at the rear of the switcher. The Channel A stacking connectors on the rear panel should be connected together on each switcher with the last one of the chain connected to the appropriate System One Channel A connector. The Channel B stacking connectors on the rear panel should be connected together on each switcher with the last one of the chain connected to the appropriate System One Channel B connector.

The PATCH POINT version switcher uses the connectors marked Channel A as the input connections. These should be daisy chained to the other switchers in the system and connected to one channel of the System One generator output. The Channel B connectors are used as the output connectors and should be connected to the same channel of the ANALYZER input. This channel is then selected by setting the corresponding rocker switch, A or B, on the rear of the switcher to the up position.

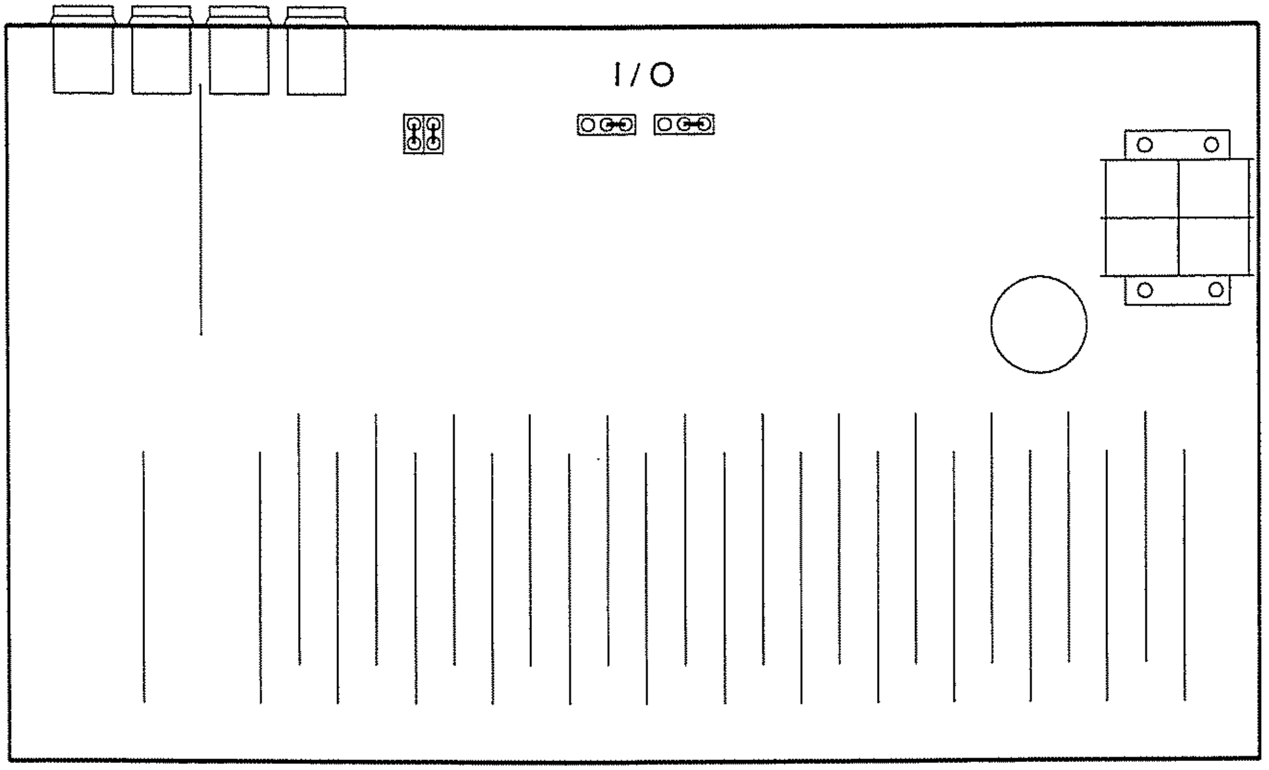


Figure SWR122.1 JUMPER LOCATIONS FOR OUTPUT SWITCHER

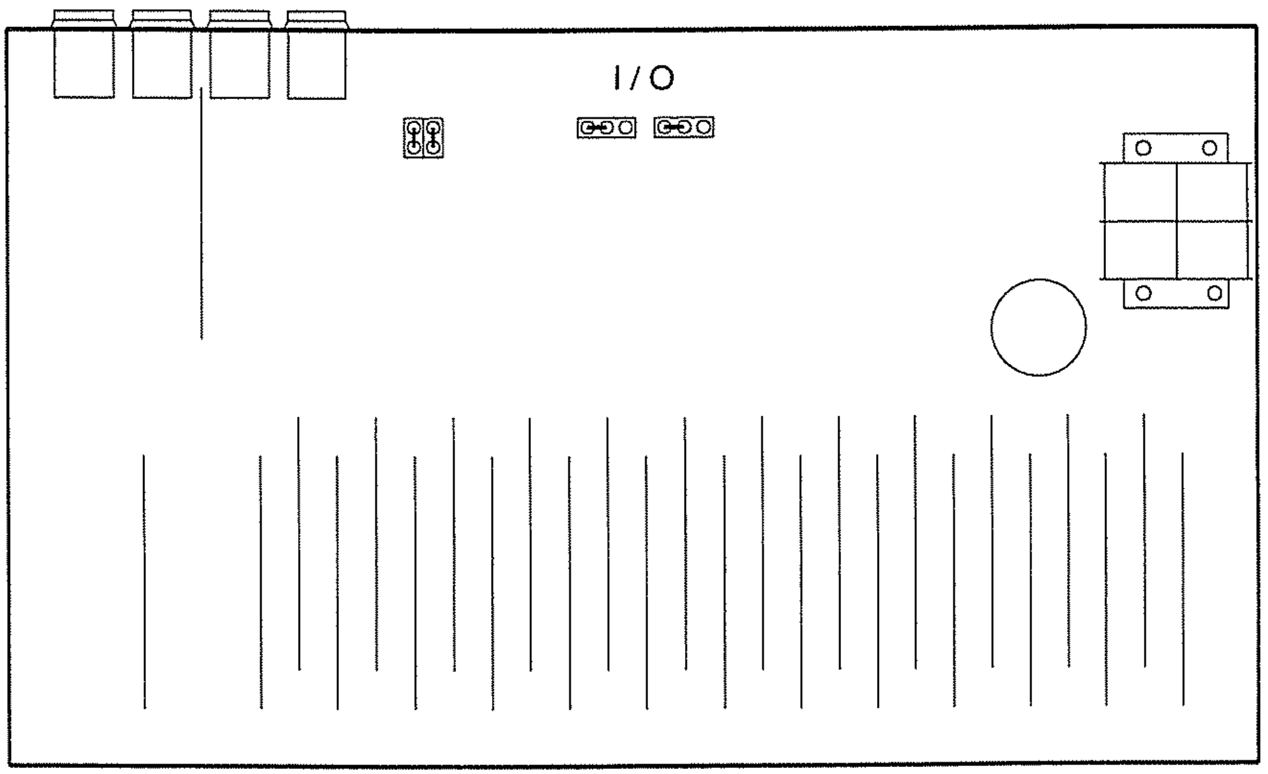


Figure SWR122.2 JUMPER LOCATIONS FOR INPUT SWITCHER

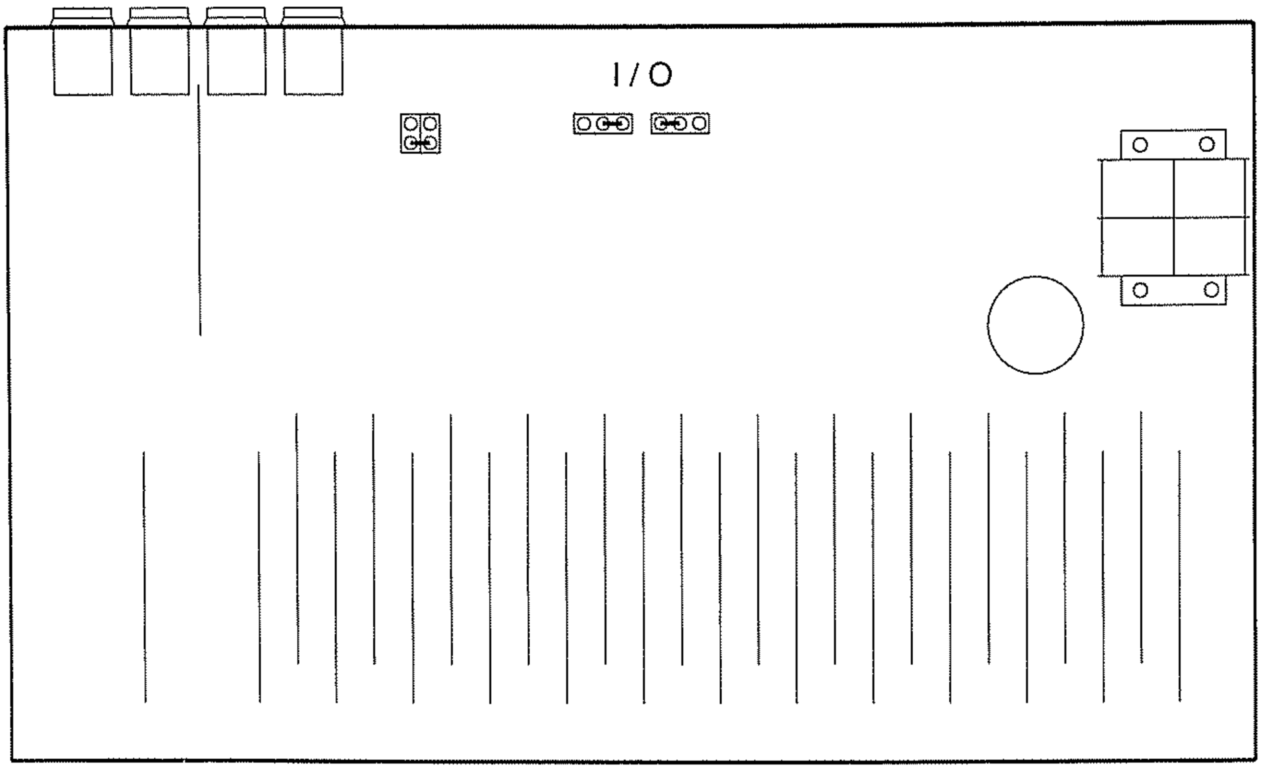


Figure SWR122.3 JUMPER LOCATIONS FOR PATCH POINT SWITCHER

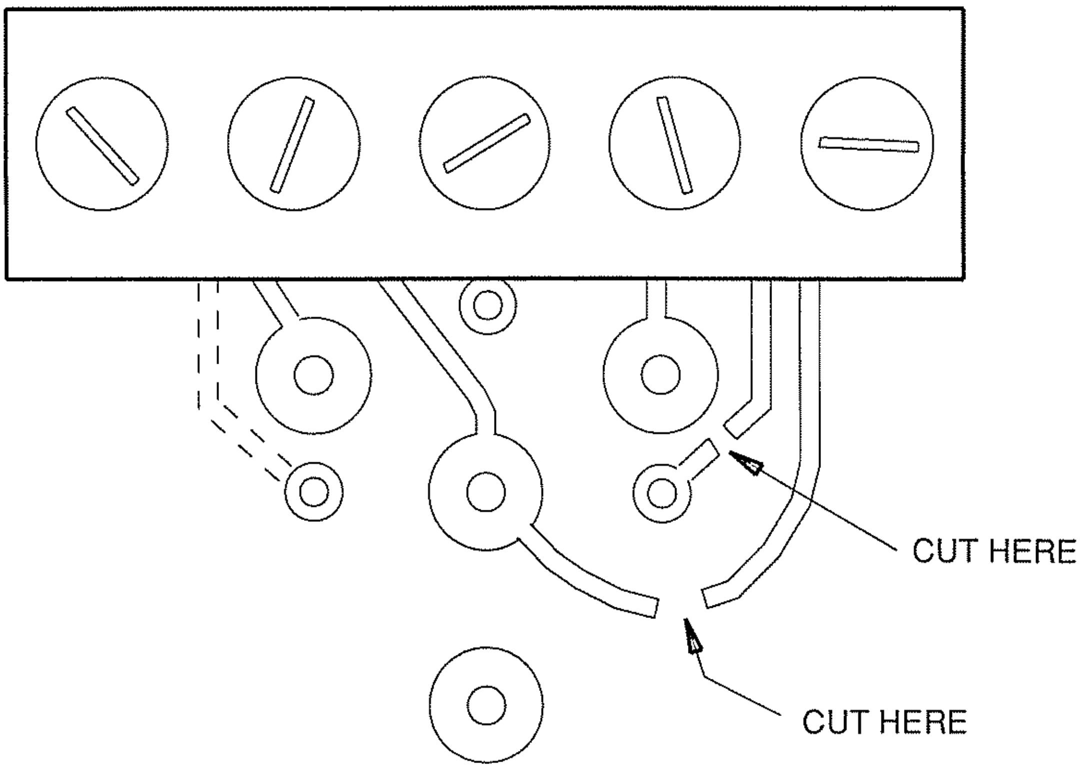
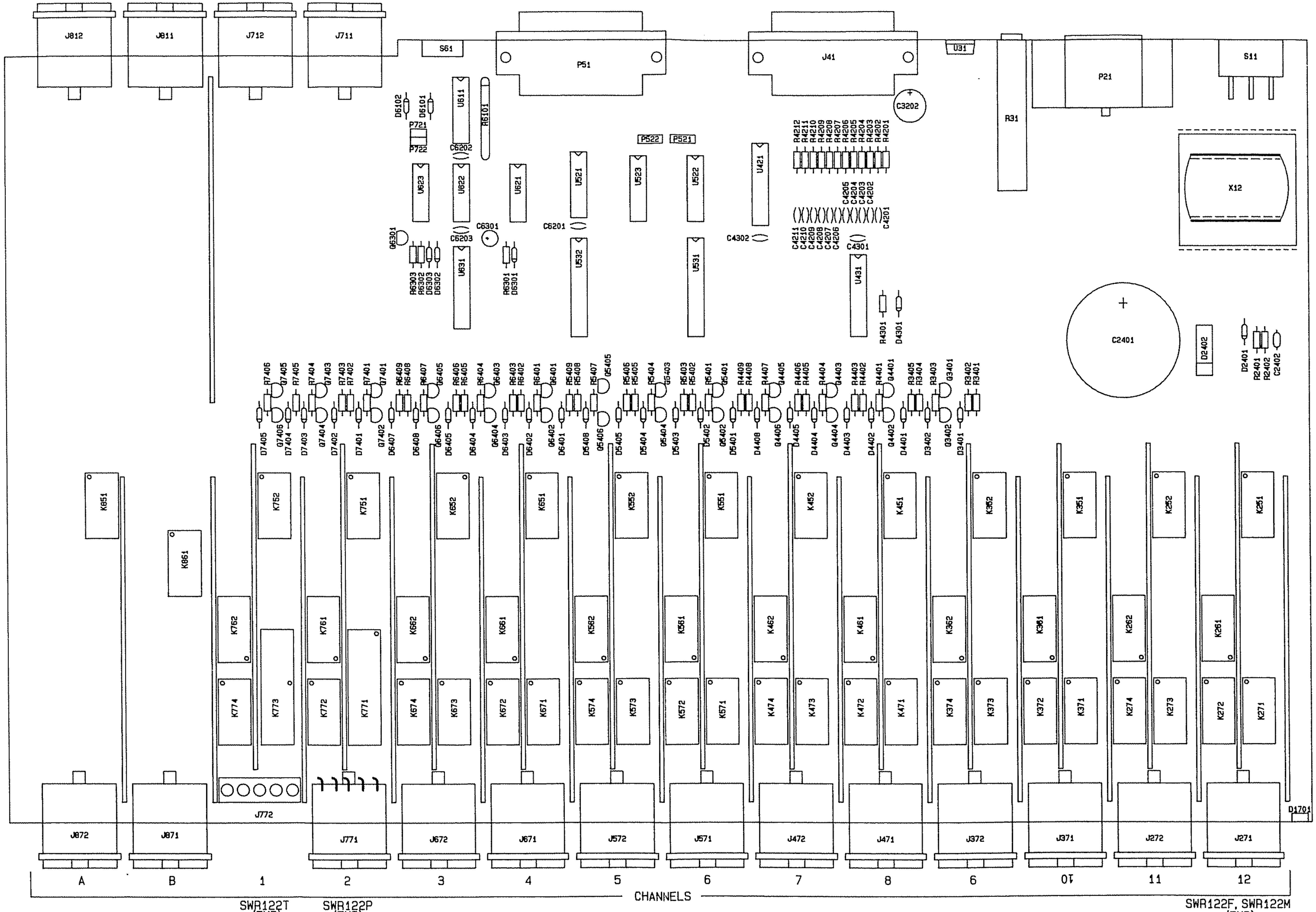
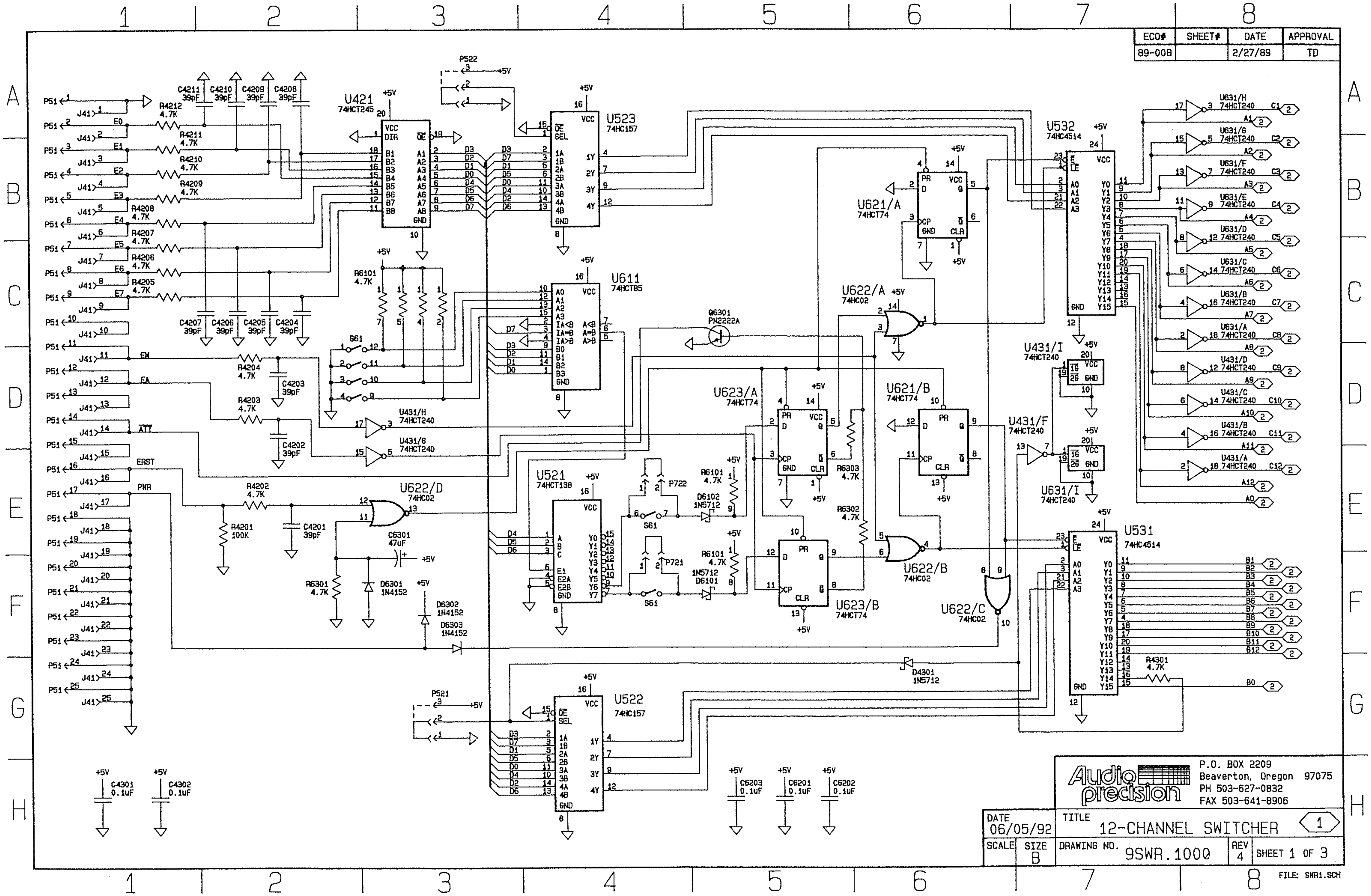
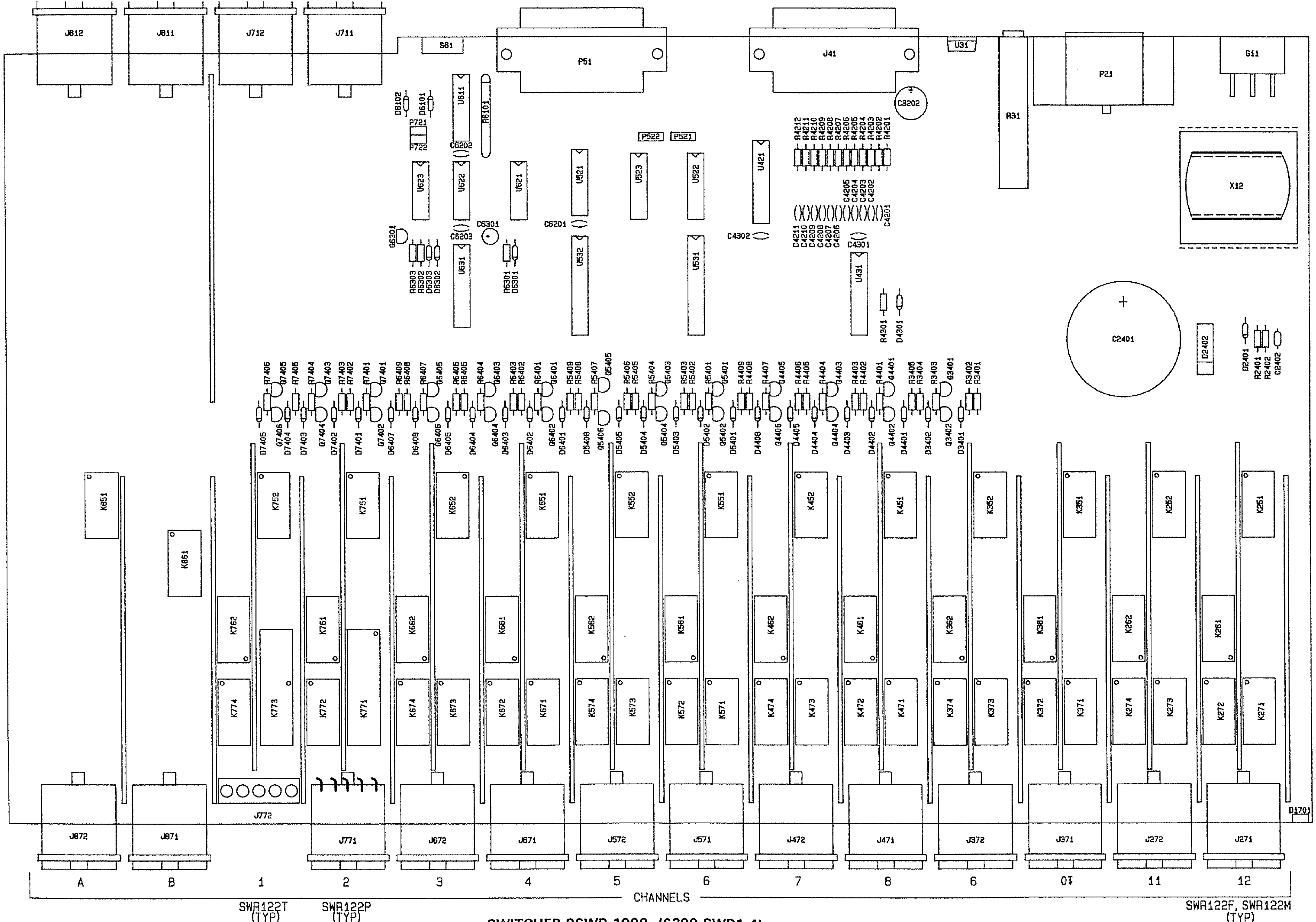


Figure SWR122.4 TRACES TO CUT FOR PATCH POINT SWITCHER

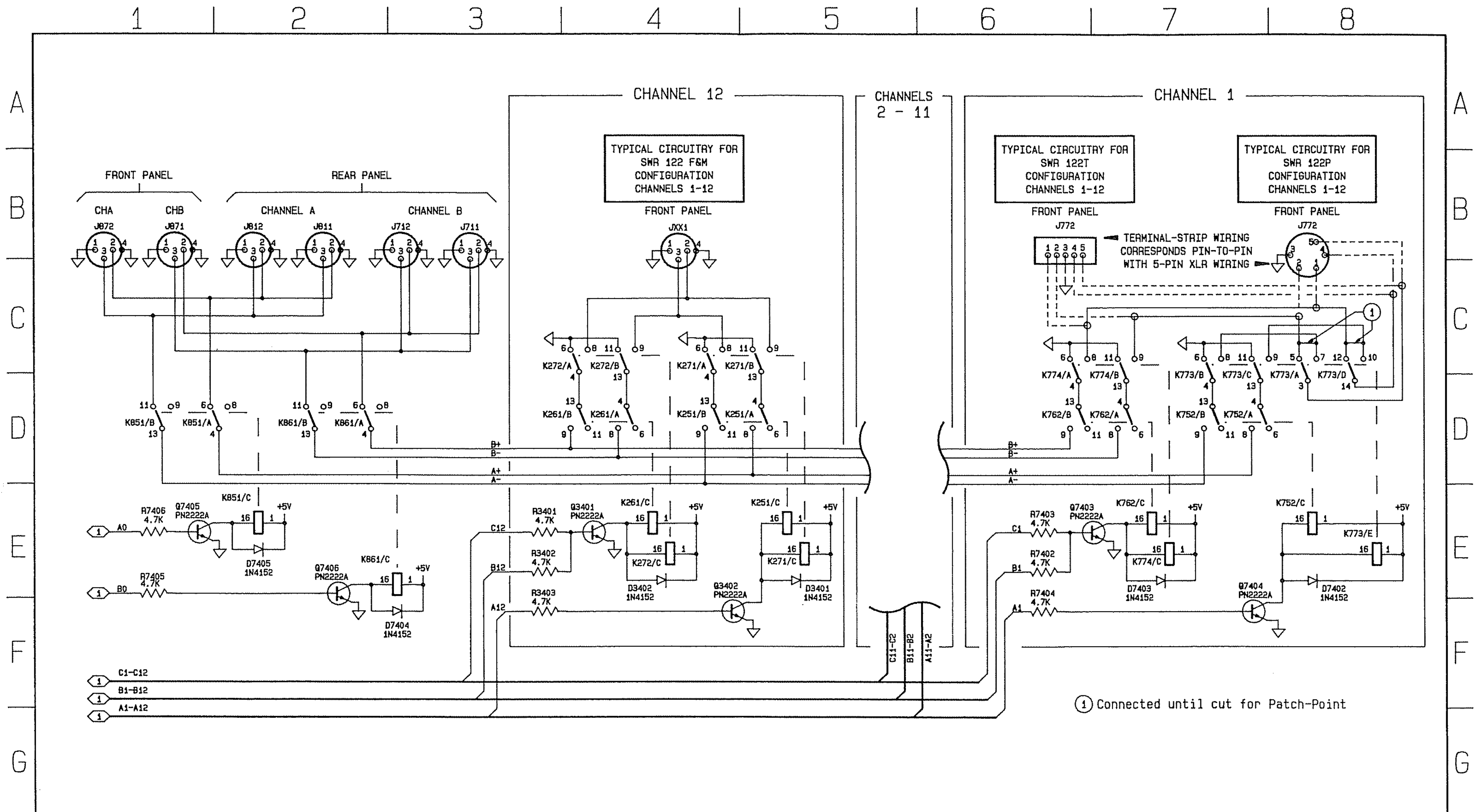


SWITCHER 9SWR.1000 (6200.SWR1.4)


ECO# | SHEET# | DATE | APPROVAL
89-008 | | 2/27/89 | TD
U421 74HCT245
U523 74HC157
U522 74HC157
U611 74HCT85
U521 74HCT138
U532 74HC4514
U531 74HC4514
U621/A 74HCT74
U621/B 74HCT74
U623/A 74HCT74
U623/B 74HCT74
U622/A 74HC02
U622/B 74HC02
U622/C 74HC02
U622/D 74HC02
Q6301 PN2222A
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 06/05/92
TITLE 12-CHANNEL SWITCHER
SCALE
SIZE B
DRAWING NO. 9SWR.1000
REV 4
SHEET 1 OF 3
FILE: SWR1.SCH



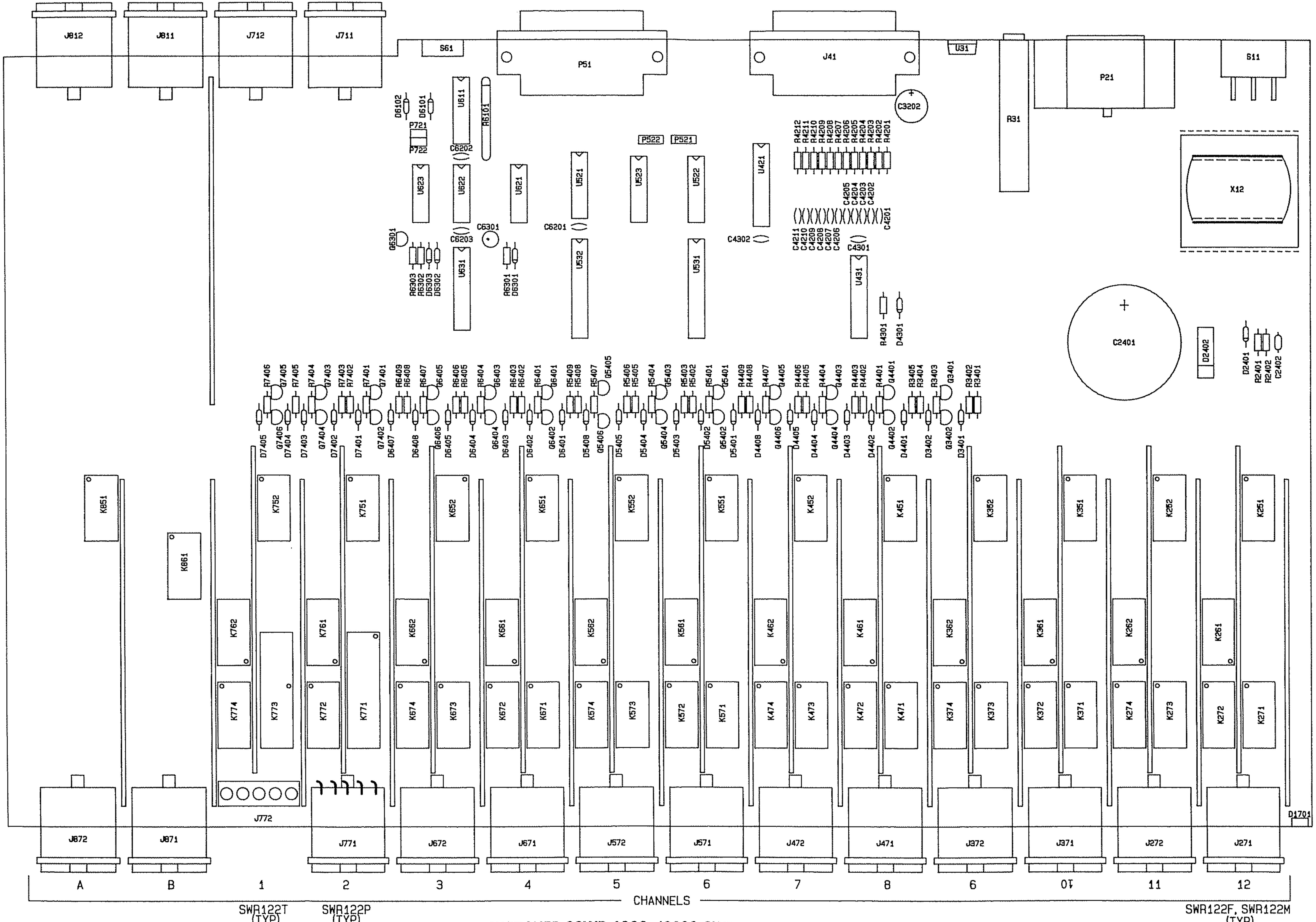
SWITCHER 9SWR.1000 (6200.SWR1.4)



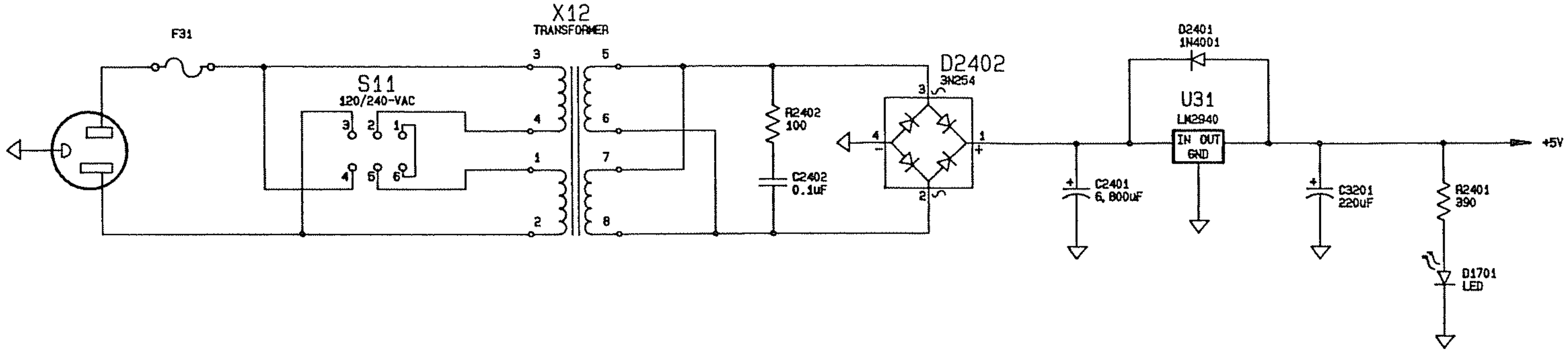
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE 06/05/92
TITLE 12-CHANNEL SWITCHER 2
SCALE
SIZE B
DRAWING NO. 9SWR.1000
REV 4
SHEET 2 OF 3

FILE: SWR2.SCH



SWITCHER 9SWR.1000 (6200.SWR1.4)



Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE		
06/05/92	12-CHANNEL SWITCHER (3)		
SCALE / SIZE B	DRAWING NO. 9SWR.1000	REV 4	SHEET 3 OF 3

FILE: SWR3.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C2401	3C6	2941.0688	CAP AL-EL 35V +80/-20%	6800uF
C2402	3D4	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	3D7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4201	1E2	2172.0330	CAP CERAM 100V 20%	33pF
C4202	1D2	2172.0330	CAP CERAM 100V 20%	33pF
C4203	1D2	2172.0330	CAP CERAM 100V 20%	33pF
C4204	1C2	2172.0330	CAP CERAM 100V 20%	33pF
C4205	C42	2172.0330	CAP CERAM 100V 20%	33pF
C4206	1C2	2172.0330	CAP CERAM 100V 20%	33pF
C4207	1C2	2172.0330	CAP CERAM 100V 20%	33pF
C4208	1A2	2172.0330	CAP CERAM 100V 20%	33pF
C4209	1A2	2172.0330	CAP CERAM 100V 20%	33pF
C4210	1A2	2172.0330	CAP CERAM 100V 20%	33pF
C4211	1A2	2172.0330	CAP CERAM 100V 20%	33pF
C4301	1G6	2172.0104	CAP CERAM 100V 20%	.1uF
C4302	1H1	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	1H5	2172.0104	CAP CERAM 100V 20%	.1uF
C6202	1H5	2172.0104	CAP CERAM 100V 20%	.1uF
C6203	1H5	2172.0104	CAP CERAM 100V 20%	.1uF
C6301	1E3	2932.0476	CAP AL-EL 25V 20%	47uF
D1701	3E7	3610.0004	LED .125 X.22	YELLOW
D2401	3D6	3111.4001	DIODE POWER 1A 50V	4001
D2402	3D5	3140.0254	BRIDGE 2A 100V	3N254
D3401	2E5	3110.4152	DIODE SIGNAL	4152
D3402	2E4	3110.4152	DIODE SIGNAL	4152
D4301	1D8	3120.0000	DIODE SCHOTTKY	1SS97
D4401	---	3110.4152	DIODE SIGNAL	4152
D4402	---	3110.4152	DIODE SIGNAL	4152
D4403	---	3110.4152	DIODE SIGNAL	4152
D4404	---	3110.4152	DIODE SIGNAL	4152
D4405	---	3110.4152	DIODE SIGNAL	4152
D4406	---	3110.4152	DIODE SIGNAL	4152
D5401	---	3110.4152	DIODE SIGNAL	4152
D5402	---	3110.4152	DIODE SIGNAL	4152
D5403	---	3110.4152	DIODE SIGNAL	4152
D5404	---	3110.4152	DIODE SIGNAL	4152
D5405	---	3110.4152	DIODE SIGNAL	4152
D5406	---	3110.4152	DIODE SIGNAL	4152
D6101	1G5	3120.0000	DIODE SCHOTTKY	1SS97
D6102	1F5	3120.0000	DIODE SCHOTTKY	1SS97
D6301	1F3	3110.4152	DIODE SIGNAL	4152
D6302	1F3	3110.4152	DIODE SIGNAL	4152
D6303	1F2	3110.4152	DIODE SIGNAL	4152
D6401	---	3110.4152	DIODE SIGNAL	4152
D6402	---	3110.4152	DIODE SIGNAL	4152
D6403	---	3110.4152	DIODE SIGNAL	4152
D6404	---	3110.4152	DIODE SIGNAL	4152
D6405	---	3110.4152	DIODE SIGNAL	4152
D6406	---	3110.4152	DIODE SIGNAL	4152
D6407	---	3110.4152	DIODE SIGNAL	4152
D7401	---	3110.4152	DIODE SIGNAL	4152
D7402	2E8	3110.4152	DIODE SIGNAL	4152

REPLACEABLE ELECTRICAL PARTS LIST: 9SWR.122X

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
D7403	2E7	3110.4152	DIODE SIGNAL	4152
D7404	2F3	3110.4152	DIODE SIGNAL	4152
D7405	2E2	3110.4152	DIODE SIGNAL	4152
E311	---	4262.0001	FUSE HOLDER PC	UNIVERSAL
E312		4262.0002	FUSE HOLDER INSERT	1/4in
F31	3C2	4620.0020	FUSE SLO-BLO 1/4	.2A
J271	2B4	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J272	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J371	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J372	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J41	1A1-1G1	4225.0025	JACK D-SUB PC 90'	25 PIN
J471	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J472	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J521	---	4220.1002	JACK MINI-JUMPER	2 PIN
J522	---	4220.1002	JACK MINI-JUMPER	2 PIN
J571	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J572	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J671	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J672	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J711	2B3	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J712	2B3	4253.0011	JACK XLR PC MT RT ANGLE	MALE
J721	---	4220.1002	JACK MINI-JUMPER	2 PIN
J722	---	4220.1002	JACK MINI-JUMPER	2 PIN
J771	---	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J772	2B6,2B8	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J811	2B2	4253.0012	JACK XLR PC MT RT ANGLE	FEMALE
J812	2B2	4253.0011	JACK XLR PC MT RT ANGLE	MALE
J871	2B1	4253.0011	JACK XLR PC MT RT ANGLE	MALE
J872	2B1	4253.0011	JACK XLR PC MT RT ANGLE	MALE
K251	2D4,2E5	4530.0002	RELAY PC LOW POWER	DPDT
K252	---	4530.0002	RELAY PC LOW POWER	DPDT
K261	2D4,2E4	4530.0002	RELAY PC LOW POWER	DPDT
K262	---	4530.0002	RELAY PC LOW POWER	DPDT
K271	2C4,2E5	4530.0002	RELAY PC LOW POWER	DPDT
K272	2C4,2E4	4530.0002	RELAY PC LOW POWER	DPDT
K273	---	4530.0002	RELAY PC LOW POWER	DPDT
K274	---	4530.0002	RELAY PC LOW POWER	DPDT
K351	---	4530.0002	RELAY PC LOW POWER	DPDT
K352	---	4530.0002	RELAY PC LOW POWER	DPDT
K361	---	4530.0002	RELAY PC LOW POWER	DPDT
K362	---	4530.0002	RELAY PC LOW POWER	DPDT
K371	---	4530.0002	RELAY PC LOW POWER	DPDT
K372	---	4530.0002	RELAY PC LOW POWER	DPDT
K373	---	4530.0002	RELAY PC LOW POWER	DPDT
K374	---	4530.0002	RELAY PC LOW POWER	DPDT
K451	---	4530.0002	RELAY PC LOW POWER	DPDT
K452	---	4530.0002	RELAY PC LOW POWER	DPDT
K461	---	4530.0002	RELAY PC LOW POWER	DPDT
K462	---	4530.0002	RELAY PC LOW POWER	DPDT
K471	---	4530.0002	RELAY PC LOW POWER	DPDT
K472	---	4530.0002	RELAY PC LOW POWER	DPDT
K473	---	4530.0002	RELAY PC LOW POWER	DPDT

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
K474	---	4530.0002	RELAY PC LOW POWER	DPDT
K551	---	4530.0002	RELAY PC LOW POWER	DPDT
K552	---	4530.0002	RELAY PC LOW POWER	DPDT
K561	---	4530.0002	RELAY PC LOW POWER	DPDT
K562	---	4530.0002	RELAY PC LOW POWER	DPDT
K571	---	4530.0002	RELAY PC LOW POWER	DPDT
K572	---	4530.0002	RELAY PC LOW POWER	DPDT
K573	---	4530.0002	RELAY PC LOW POWER	DPDT
K574	---	4530.0002	RELAY PC LOW POWER	DPDT
K651	---	4530.0002	RELAY PC LOW POWER	DPDT
K652	---	4530.0002	RELAY PC LOW POWER	DPDT
K661	---	4530.0002	RELAY PC LOW POWER	DPDT
K662	---	4530.0002	RELAY PC LOW POWER	DPDT
K671	---	4530.0002	RELAY PC LOW POWER	DPDT
K672	---	4530.0002	RELAY PC LOW POWER	DPDT
K673	---	4530.0002	RELAY PC LOW POWER	DPDT
K674	---	4530.0002	RELAY PC LOW POWER	DPDT
K751	---	4530.0002	RELAY PC LOW POWER	DPDT
K752	2D7,2E8	4530.0002	RELAY PC LOW POWER	DPDT
K761	---	4530.0002	RELAY PC LOW POWER	DPDT
K762	2D6,2D7,2E7	4530.0002	RELAY PC LOW POWER	DPDT
K771	---	4530.0002	RELAY PC LOW POWER	DPDT
K772	---	4530.0002	RELAY PC LOW POWER	DPDT
K773	2C7,2C8,2E8	4530.0002	RELAY PC LOW POWER	DPDT
K774	2C6,2C7,2E7	4530.0002	RELAY PC LOW POWER	DPDT
K851	2D1,2E2	4530.0002	RELAY PC LOW POWER	DPDT
K861	2D2,2E2	4530.0002	RELAY PC LOW POWER	DPDT
P21	3D1	4256.0001	PLUG PC MOUNT 240V	3 COND
P51	1A1-1G1	4225.0125	PLUG D-SUB PC 90'	25 PIN
P521	1G3	4221.0036	PLUG PC .1 X.43	36 PIN
P522	1A3	4221.0036	PLUG PC .1 X.43	36 PIN
P721	1E5	4221.0036	PLUG PC .1 X.43	36 PIN
P722	1E5	4221.0036	PLUG PC .1 X.43	36 PIN
Q3401	2E4	3211.2222	XSTR NPN TO92	PN2222A
Q3402	2F4	3211.2222	XSTR NPN TO92	PN2222A
Q4401	---	3211.2222	XSTR NPN TO92	PN2222A
Q4402	---	3211.2222	XSTR NPN TO92	PN2222A
Q4403	---	3211.2222	XSTR NPN TO92	PN2222A
Q4404	---	3211.2222	XSTR NPN TO92	PN2222A
Q4405	---	3211.2222	XSTR NPN TO92	PN2222A
Q4406	---	3211.2222	XSTR NPN TO92	PN2222A
Q5401	---	3211.2222	XSTR NPN TO92	PN2222A
Q5402	---	3211.2222	XSTR NPN TO92	PN2222A
Q5403	---	3211.2222	XSTR NPN TO92	PN2222A
Q5404	---	3211.2222	XSTR NPN TO92	PN2222A
Q5405	---	3211.2222	XSTR NPN TO92	PN2222A
Q5406	---	3211.2222	XSTR NPN TO92	PN2222A
Q6301	1C5	3211.2222	XSTR NPN TO92	PN2222A
Q6401	---	3211.2222	XSTR NPN TO92	PN2222A
Q6402	---	3211.2222	XSTR NPN TO92	PN2222A
Q6403	---	3211.2222	XSTR NPN TO92	PN2222A
Q6404	---	3211.2222	XSTR NPN TO92	PN2222A

REPLACEABLE ELECTRICAL PARTS LIST: 9SWR.122X

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
Q6405	---	3211.2222	XSTR NPN TO92	PN2222A
Q6406	---	3211.2222	XSTR NPN TO92	PN2222A
Q7401	---	3211.2222	XSTR NPN TO92	PN2222A
Q7402	---	3211.2222	XSTR NPN TO92	PN2222A
Q7403	2E6	3211.2222	XSTR NPN TO92	PN2222A
Q7404	2F7	3211.2222	XSTR NPN TO92	PN2222A
Q7405	2E1	3211.2222	XSTR NPN TO92	PN2222A
Q7406	2E2	3211.2222	XSTR NPN TO92	PN2222A
R2401	3D7	1214.0391	RES 1/4W C FLM 5%	390
R2402	3D4	1214.0101	RES 1/4W C FLM 5%	100
R3401	2E3	1214.0472	RES 1/4W C FLM 5%	4.7K
R3402	2E3	1214.0472	RES 1/4W C FLM 5%	4.7K
R3403	2E3	1214.0472	RES 1/4W C FLM 5%	4.7K
R3404	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R3405	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4201	1E2	1214.0104	RES 1/4W/C/FLM 5%	100K
R4202	1E2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4203	1D2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4204	1D2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4205	1C1	1214.0472	RES 1/4W C FLM 5%	4.7K
R4206	1C1	1214.0472	RES 1/4W C FLM 5%	4.7K
R4207	1B1	1214.0472	RES 1/4W C FLM 5%	4.7K
R4208	1B1	1214.0472	RES 1/4W C FLM 5%	4.7K
R4209	1B2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4210	1B2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4211	1A2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4212	1A1	1214.0472	RES 1/4W C FLM 5%	4.7K
R4301	1G8	1214.0472	RES 1/4W C FLM 5%	4.7K
R4401	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4402	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4403	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4404	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4405	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4406	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4407	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4408	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R4409	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5401	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5402	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5403	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5404	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5405	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5406	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5407	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5408	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R5409	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6101	1C3	1984.9472	RES NET SIP 5% B	9 X 4.7K
R6301	1E6	1214.0472	RES 1/4W C FLM 5%	4.7K
R6302	1G7	1214.0472	RES 1/4W C FLM 5%	4.7K
R6303	1F7	1214.0472	RES 1/4W C FLM 5%	4.7K
R6401	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6402	---	1214.0472	RES 1/4W C FLM 5%	4.7K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R6403	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6404	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6405	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6406	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6407	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6408	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R6409	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R7401	---	1214.0472	RES 1/4W C FLM 5%	4.7K
R7402	2E6	1214.0472	RES 1/4W C FLM 5%	4.7K
R7403	2E6	1214.0472	RES 1/4W C FLM 5%	4.7K
R7404	2F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R7405	2E1	1214.0472	RES 1/4W C FLM 5%	4.7K
R7406	2E1	1214.0472	RES 1/4W C FLM 5%	4.7K
S11	3D3	4340.0001	SWITCH SLIDE 120V-240V	DPDT
S61	1D5	4311.0006	SWITCH DIP 90'	6 POLE
U31	3C5	3430.2940.5	VOLT REG POS 5.0V TO220	LM2940
U421	1A3	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U431	1D8,1E8,1D3	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U521	1E4	3324.0138	DECODER 3LINE/8LINE	74HCT138
U522	1G4	3323.0157	MULTIPLEXER 4 X 2CH	74HC157
U523	1A4	3323.0157	MULTIPLEXER 4 X 2CH	74HC157
U531	1E7	3323.4514	DECODER 4 X 16-LN	74HC4514
U532	1B7	3323.4514	DECODER 4 X 16-LN	74HC4514
U611	1C4	3313.0085	COMPARATOR 4-BIT MAG	74LS85
U621	1C6,1D6	3324.0074	FLIP-FLOP 2X D	74HCT74
U622	1C6,1E6,1F6,1E3	3323.0002	GATE 4X2-IN NAND	74HC02
U623	1D5,1E5	3324.0074	FLIP-FLOP 2X D	74HCT74
U631	1A8-1C8	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
X12	3C4	4523.0001	TRANSFORMER POWER	SWR-1

DCX-127 MULTIFUNCTION ACCESSORY

DCX-127, MULTIFUNCTION ACCESSORY MODULE

Introduction

The Audio Precision DCX-127 provides many functions in one package. These include a 4-1/2 digit voltmeter-ohmmeter, two 20-bit D/A converters, a 22-bit digital input, a 22-bit digital output, four 8-bit digital outputs, an 8-bit digital input which sends commands to the host computer, and several outputs which indicate program flow.

Logic & Interface <1>

The digital information from the host computer is routed through the 25-pin D-subminiature connectors P151 and J151. All signals are looped from one jack to the next, whether or not they are used in the DCX-127.

The data/address input lines are filtered by resistor/capacitor lowpass networks which reduce susceptibility to RFI and intersignal interference. Their outputs are buffered by octal buffer U263. This buffered address and data information drives the address decoding circuitry consisting of U311 and U322. Data leaving the DCX-127 is buffered by octal buffer U262. U432C controls which direction is enabled, U432D inverts this signal to drive the other buffer.

The address strobe line EA is filtered by R2504 and C6304 and buffered/inverted by U533A. The output of this buffer is normally high and strobes low to latch valid address information. This latching is performed by 6-bit latch U322. The Q1 output of U322 will be low when the correct address has been written to the DCX-127. The output of U533D will go high, turning on Q2401, pulling the /ATT line. This tells the host computer that the DCX-127 is present.

When the write strobe EW is pulsed high by the host computer to write data it is filtered by R2502 and C6303. U533C buffers and inverts this signal, driving 1-of-8 decoder U331 and half of dual 1-of-4 decoder U323. Their outputs will go low when a valid write strobe is received.

When power is first applied C3304, D2301 and R2301 provide a power on reset pulse through NOR gate U432B. The host computer may also generate a reset pulse by strobing ERST which drives the other input of the NOR gate. The low going pulse from U432B clears the address latch U322, driving the Q0 output low. This clears flip-flop U313C/U313D and holds the instrument in reset condition until it is initialized by the computer. The output of this flip-flop also drives the front panel RESET line on J941. When U322 is cleared D2401 pulls the PWR line low. This signals the host computer that a power failure has occurred and that data in the DCX-127 is no longer valid.

NAND gate U313B and crystal Y311 form a 20 MHz oscillator. R3101 supplies bias current for the gate input. The output of the oscillator is buffered by U313A to drive counter/divider U321. U321A is a divide-by-5 which supplies 4 MHz to the microprocessor U422. Divide-by-2 counters U321B and U321C deliver a 5 MHz signal to the DMM clock prescaler U232.

Program Control Outputs <1>

The program control output port consists of two types of output. The first is a one shot pulse, the other is a conventional bi-level output. The one shot pulses are triggered by read strobes from 1-of-8 decoder U332. Quad NAND gate U431 and the associated resistors, capacitors and diodes form three 2 msec one shots. Consider the operation of U431A. When pin 9 of U332 goes low the output of NAND gate U431A goes high. This also discharges C4302 through D4301. When the output of U332 returns high C4302 will maintain the output of U431A high until it charges through R4301. The output of U431A drives the front panel connector through R834 which provides current limiting against overload conditions.

The sweep gate and delayed gate signals indicate the status of a sweep in progress. The sweep gate signal comes from bit 5 of U362. It goes high during a sweep and low at all other times. This signal is inverted by U431B to drive the front panel sweep gate output. It also drives the gate input of one counter in an 82C54 triple counter U622 and clears flip-flop U613A. When this line rises at the beginning of a sweep the counter will be triggered. The counter will output a pulse at the end of a time interval programmed by the microprocessor. This pulse clocks the flip-flop low, setting the delayed gate output low. At the end of the sweep the flip-flop is cleared, setting the delayed gate high.

The A/B line comes directly from U362 and is programmed by the host computer to be low when channel A is selected and high when channel B is selected. This output and the sweep gate outputs are isolated by 390 Ohm resistors R834.

Microprocessor <2>

The intelligence for the DCX-127 is provided by a 68705P3 microprocessor. It controls the autoranging of the DMM, reads the output of the A/D converter, sets the gate delay, sets the digital input strobe counter and handles the buffer queue for the program control input.

The processor communicates with the host computer by a bank of dual port RAMs. These are 74LS670 register files U412, U413, U421, U512, U513 and U521. Two are used to send data from the host computer to the microprocessor and four are used to send data to the computer from the microprocessor. The PC0 and PC1 pins on the microprocessor are used for address selection of the RAMs. Chip selects are driven by the PA0-PA7 pins of the microprocessor. The PB0-PB7 pins serve as the external data bus. Resistor network R421 pulls the chip selects high when the microprocessor is held in reset, for example after power up.

Octal latch U531 buffers data from the program control input jack. Resistor network R631 provides current limiting protection against overvoltage and reverse voltage inputs. Resistor network R835 pulls the inputs high. This provides protection against static buildup and allows connection of switch closures to ground.

The processor scans this buffer and queues the data for later reading by the computer. When the computer reads the data from the appropriate RAM location U411B interrupts the processor. This allows the processor to keep track of what the computer has read.

Auxiliary Digital Outputs <3>

Four 8-bit auxiliary digital outputs are provided on the rear of the DCX-127. Three are identical, one includes power supply voltages for driving small amounts of circuitry.

U211, U212, U221 and U231 are octal latches which are programmed by the host computer. They are CMOS output, enabling relatively high load currents. Resistor networks R211, R221, R222 and R231 limit the current under fault conditions to 12 mA per output pin. When power is first applied the SAFETY line drives the output enables high, preventing incorrect data from being sent to the test system. The eight bits of data and ground are available on 9-pin connectors J111, J121 and J131.

The data from U231 appears on a 15-pin connector, J141, along with +5V, -16V, +16V supplies and ground. The supplies are protected against overvoltage by diodes D1301, D1401, and D1402. Capacitors C2103, C2202, C2203, and C2303 reduce susceptibility of the latches to static pulses.

22-Bit Digital Output <4>

The 22-bit digital output sends parallel digital data to a test device. It is designed to output all data simultaneously despite time differences between individual byte writes by the computer. When new data is output the strobe line is pulsed low. The outputs are CMOS and TTL compatible with a 390 Ohm source impedance.

The data from the host computer is sent one byte at a time. To allow simultaneous output of new data the signals are reclocked. All data is written to a single address by the computer. Latch U511 is used as a shift register to provide the strobe signals to each data latch. It starts from the clear condition with all outputs low. When the first byte is written the Q0 output will be clocked high, providing an edge to clock data latch U611. The most significant byte is written first into U611. The next byte is written into U612 as the Q1 output of U511 goes high. When the third byte is written the Q2 output of U511 rises. This latches the data into U712 and at the same time latches the data from U611 and U612 into U711 and U713 respectively. This also drives U621A low to signal new data to the external test device. Shift register U511 is cleared by a read strobe from U332. This sets all of its outputs low again and sets the external strobe high.

U711, U712 and U713 have CMOS outputs, enabling relatively high load currents. Resistor networks R811, R812 and R813 limit the current under fault conditions to about 12 mA per output pin. When power is first applied the SAFETY line drives the output enables high, preventing incorrect data from being sent to the test system.

22-Bit Digital Input <5>

The 22-bit digital input reads parallel digital data from a test device. It is designed to latch all input data simultaneously and allow the host computer to asynchronously read it one byte at a time. The test device presents data to the input pins and pulses the strobe line low. Data is latched on the rising edge of the strobe. The inputs are TTL compatible levels with a 100 kOhm impedance to ground.

The data is latched into three octal data latches U722, U723 and U731. Resistor networks R821, R823 and R832 provide current limiting protection against overvoltage and reverse voltage inputs. Resistor networks R822, R831 and R833 pull the inputs to ground. This provides protection against static buildup and maintains repeatable low levels at unconnected inputs.

NAND gate U621B buffers the external strobe input and combines the internal readings strobe signal. R834, D6202 and D6101 protect the input against reverse and excessive input voltage. R6102 pulls the input high when no external strobe is connected. The output of U621B is coupled through C6202 to R6201, D6203 and U621D. These form a one shot which drives the clock inputs of the latches. The one shot output also drives the interrupt line of the Audio Precision interface bus through Q2501. This signals the host computer that a reading is ready.

The second input of U621B is driven by the output of one section of triple counter U622. This will strobe the input at a rate selectable from 4 to 32 readings per second. This value is programmed through the microprocessor. The output of the counter will strobe low at the programmed rate.

The outputs of the octal latches are tied to the internal data bus. They are normally tri-stated, the outputs are enabled when the appropriate output enable line is pulled low. The output enables are driven by the 1-of-8 decoder U332. When a reading strobe occurs the IRQ line increments eight bit counter U732. The outputs are tri-state and are enabled by a read strobe from U332. When the read strobe goes low NAND gate U621C drives the counter RCLK input high to latch the count into the internal output latches. The computer reads this count to see when new readings are ready.

D/A Converters <6>

The two 20-bit D/A converters are implemented with a pulse width conversion technique. The two D/A converters are identical, so only one will be described here. A precision dc voltage is chopped into pulses by a digital counter. After lowpass filtering the output voltage may be controlled by adjusting the pulse width. The converter is constructed with a separate coarse and fine counters to allow keep the update rate of each counter fast enough for the desired settling time. To improve the linearity and reduce ripple the coarse voltage adjustment is accomplished with two 12-bit counters operating in a push pull fashion. The counters are allowed to be one count off from each other, giving a resolution of 13 bits. The remaining seven bits are obtained from a third counter.

The three counters required for one converter are contained in an 82C54, U261. The counters are each 16-bit with independent clock, gate and output pins. Only the lower 12 bits of each are used. Binary counter U232 divides the 5 MHz clock by 4096 to 1.22 kHz (819 usec period) which is used to trigger the counters. The counters are clocked at 5 MHz, causing their outputs to go low for a time equal to the programmed count divided by 5 MHz. Since the counters are triggered every 819 usec the output will have a duty cycle of the programmed count divided by 4096.

The outputs drive flip-flops U341 and U342. The flip-flops remove any time skew and jitter in the outputs. They also provide a low impedance differential output which can drive the inputs of the differential amplifiers which follow. To further reduce the output impedance each flip-flop consists of two flip-flops wired in parallel.

Each flip-flop output drives the differential input summing amplifier consisting of U441 and U442. U441 sums the Q output of U341A, the /Q output of U341B and the Q output of U342A. This results in an output voltage which goes from 0 to -5 V as the counters are programmed from 1 to 4095. This voltage is summed with the /Q output of U341A, the Q output of U341B and the /Q output of U342A in U442. The output voltage of U442 therefore swings $\pm$10 V.

Counter 1 and counter 2 operate with complementary pulse widths, when one is set to a large count the other is set low. This gives first order rejection of ripple in the output of U442. The use of both the Q and /Q flip-flop outputs results in cancellation of nonlinearities due to differing high state and low state output impedances of the flip-flops. The resistor network R341 insures that the flip-flops used for the 13 MSBs are summed with equal gain and also provides the gain setting resistors for U441 and U442. The lower seven bits are summed through R3403 and R3402 to give a 1/128 weighting to their output. R3401 equalizes the load on the these flip-flops with that on the higher bits, reducing the effect of the finite output impedance on linearity.

C4401 and C4403 filter the voltage to reduce the slew rate requirements of the op-amps U441 and U442. C3401 and C4402 absorb the fast changes in voltage which would otherwise exceed the capability of the amplifiers. R5403 adjusts the offset by feeding a current into either U441 or U442. R5404 adjusts the gain of U442 and sets the full scale value from the converter. R4401 increases the output voltage slightly, giving a full scale voltage of $\pm$10.500 Vdc.

Since the voltage out of the D/A converters depends upon the flip-flop supply voltage they are powered from a separate +5V regulator. U352 is a pretrimmed precision reference which includes an output buffer amplifier. R3504 reduces the required output current, reducing output impedance effects on voltage. D2501 and D2502 prevent the flip-flop inputs from being reverse biased in the event of a +15V supply failure.

U232 generates a 1.25 MHz clock for driving the DMM circuitry and a 4.88 kHz clock for the gate delay and digital input strobe counters. Data selector U333 feeds either the 5 MHz clock or the 1.25 MHz clock to divide-by-5 counter U321D. It outputs either a 1 MHz or 250 kHz clock, depending on the state of the speed line.

2-to-4 line decoder U411A senses when any write operation occurs to the counters U261 or U361. The output will pulse low, incrementing 8-bit counter U721. The host computer uses this count to guard against unauthorized writes to the dc output counters. Such writes would create problems because the counters are byte serial with an internal high byte / low byte flip-flop. If sync between the host computer and the flip-flop were lost incorrect data would be programmed.

DC Output Filters & Buffers <7>

The dc voltage from each 20-bit D/A is filtered and buffered to drive the front panel output jacks. The filter removes the ripple generated by the pulse width conversion D/A technique. The buffer provides an electronically floating output which rejects ground potential differences between the DCX-127 and the device under test. Since the circuits are identical for the two outputs, only one will be described here.

The dc voltage from the output of op-amp U442 is applied to an active filter comprised of U742 and its associated components. The filter is a 100 Hz 3-pole, 2-zero quasi-elliptic lowpass. The zeros are introduced by R5406 and C6402 which create a notch in the response at 1.22 kHz, the frequency of the major ripple component in the output. R6405 protects the op-amp input against excessive differential voltage during power down and fault conditions.

The output of the active filter U742 drives the ground sensing output buffer stage. This consists of low offset amplifier U741 and high current driver U753A. The amplifiers are wired in cascade with dc feedback around the pair. C6404 provides ac feedback around U741 to reduce its bandwidth and insure stability of the op-amp pair. R741A and R741B provide dc feedback and set the gain of the stage. R741C and R741D sense the voltage at the low output terminal to allow rejection of signals present there with respect to ground. R8402 allows adjustment of the resistor ratio to maximize common mode rejection of the output.

Positive temperature coefficient resistors R8403 and R8404 guard against excessive voltage applied to the terminals. Under normal conditions their resistance is low, dropping less than 1 V across each resistor at the 10 mA full rated output current. When a fault occurs they will heat up, increasing their resistance and reducing the power dissipated in them. D7501A and D7501B clamp the voltage at U753A's output, preventing excessive current flow through its output transistors. C8401 maintains a low output impedance at high frequencies where the gain of the op-amp is dropping. K741 disconnects the output when desired. Its drive signal comes from U362 and is buffered by Q3601.

DMM Interface <8>

The DMM circuitry is completely floating and isolated from ground. The converter circuitry interfaces serially to the microprocessor by sending a pulse stream to be counted which represents the reading obtained. This is isolated with optoisolators for the CLOCK, BUSY (or COUNT ENABLE), POLARITY, and RUN/HOLD signals. The CLOCK signal is sent from the logic circuits to the DMM and controls timing of all conversion activity. The RUN/HOLD signal tells the DMM to start a new conversion or stop after the one currently in progress. The BUSY signal indicates when the converter is in the autozero mode or when it is integrating the signal or reference.

The DMM clock is either 250 kHz or 1 MHz, depending on the reading rate selected (6 rdg/sec or 25 rdg/sec). This is buffered by Q3603 and drives optoisolator U121 located on the DMM board. The polarity indication from the DMM is buffered by Q1102 and drives optoisolator U571. Resistor R5702 draws charge from the phototransistor base to speed its turnoff. This signal is read by the microprocessor through tristate buffer U533.

BUSY is low during conversion and high during the autozero cycle. The BUSY signal is read by the microprocessor as a status indicator and is used to gate the clock signal to the counter U622. BUSY is also used to clock the run/hold flip-flop U613A. The computer presets flip-flop U613B to start a conversion. When the BUSY line transitions high at the end of a conversion the flip-flop will be clocked low, preventing the next conversion. The computer holds the preset input low when continuous conversion is desired. The output of the run/hold flip-flop drives optoisolator U122 which drives the converter.

Octal latch U532 drives the ranging relays on the DMM board. The ranges are set by the microprocessor based on fixed range information sent from the host computer or from the microprocessor's internal autoranging algorithm.

The lower four bits of octal latch U362 controls mode lines on the DMM board and the run hold flip-flop U613B. The upper four bits are used to control the on/off relays of the dc outputs and the A/B and sweep status lines. The inputs to U362 come from the D bus which receives data from the host computer.

DMM Voltmeter <9,10>

The four front panel DMM inputs are directly connected to the circuit board through short jumper wires to minimize thermocouple effects. Relays K451 and K432 provide on-off selection to totally isolate the DMM and ohmmeter circuitry from the device-under-test if a DMM measurement is not requested. The GUARD input is connected to the shield enclosing the DMM board and a large conductive plain on the main circuit board through R9802. C5602 and R5602 prevent static build-up and high frequency noise from interfering with the DMM measurement. C4603 and C4604 provide balanced decoupling of high frequency interference to the guard.

Relays K152, K151, and K142 select the input attenuation factor for the 2-20-200-500 Volt ranges. Relay K152 is energized for both 2 Volt and 200 mV ranges. Relay K151 is on for the 20 Volt range and relay K142 is on for the 200 Volt range. The default state with relays K152, K151, and K142 off provides the 500 Volt range. This connects the DMM input to the lowest tap point which could theoretically support readings up to 2 kVolts. However, component breakdown ratings limit the maximum input voltage to ±500 Vpeak.

R251 is a precision 10 MegOhm thick-film decade divider resistor network. R2503, R2501, and R2405 provide adjustment of the divider ratios for exact calibration. R3502, R3503, C3503, C3504, and C3502 function as a lowpass filter to remove the ac components of the input signal and prevent slew-rate limiting errors in the subsequent buffer stage, U342.

U342 buffers the input to maintain a high input impedance in all ranges. R2407 trims the op-amp offset to zero. The gain of U342 is switched from unity to x10 by K141 to obtain the most sensitive 200 mV range. K141 is off for the 2-20-200-500 Volt ranges, and on for the 200 mVolt range. The precision thin film resistor network R231 and related components determine the x10 gain value when K141 is energized. U341B acts as a unity gain buffer to drive guard traces on the circuit board to minimize leakage currents at the input to U342. U341A and related components comprise a 3-pole low-pass filter to improve normal mode rejection and noise immunity.

The basic dc voltage measurement is performed by A/D converter, U221. It uses the dual-slope integration technique with an auto-zero cycle. U221 also contains polarity switching, auto-zero, and control logic. The input sensitivity at pin 10 is nominally 2 Volts, determined by the +1V reference voltage at pin 2. R2202 and C2101 are the integrator components. C2101 is a polypropylene capacitor with very low dissipation factor for good A/D conversion linearity. C2202 stores the reference voltage during the de-integration phase of the conversion. C2201 stores the offset voltage accumulated during the autozero phase. The digital signals are coupled to the ground-referenced logic and microprocessor through the opto-isolators located on schematic <8>.

The +1V reference for all dc voltage measurements is generated by U311 on schematic <10>. Bandgap diodes D3101 and D3102 each generate a stable reference of about 1.23 V. These are averaged and attenuated to approximately +0.98 V by precision thin-film resistor network R411. The two diodes are averaged to obtain a statistical reduction in their temperature drift and aging characteristics. R2101, R3101, and one section of R411 provide an adjustable amount of positive offset to precisely calibrate the reference voltage to +1.000 V. R3102 and C3102 form a lowpass filter to remove any noise present in diodes D3101 and D3102.

> *NOTE: Do not use solders with water-soluble flux when making repairs to the DMM circuit board. Very small leakage currents at pins 5, 7, and 8 of U221 or pins 2 and 3 of U342 can seriously degrade accuracy. Also allow sufficient time for temperature gradients caused by soldering to stabilize before testing or calibrating the DMM.*

Ohms Current Source <10>

The ohmmeter function is obtained by measuring the dc voltage drop across the unknown resistance in response to a calibrated dc current. Figures DCX127.1 and DCX127.2 show simplified schematics of both two terminal and four terminal operation. "I_{ref}" is the test current, "Rx" is the unknown resistance being measured, "I_{comp}" is a compensation current source, and "r_w" is the test lead resistance. I_{comp} does not flow through the unknown resistor and serves only to cancel the low-side lead resistance error term in a four terminal measurement. R9701 and R9702 automatically connect the current sources to the voltmeter input terminals when using the two-terminal configuration. With the four terminal configuration R9701 and R9702 have negligible effect provided $r_W \leq 1.5$ Ohms.

The +1V reference scales both the test current source and the dc voltage measurement and has virtually no effect on ohmmeter accuracy. Accuracy and stability are determined by the current setting resistors only. The effect of the constant 10 Meg input resistance is mathematically corrected for and raises the maximum measurable resistance on the 2 Meg range to 2.5 Meg.

The I_{ref} current source is composed of U343, U331, and a switched reference resistor. The voltage at the +INPUT node is buffered through U343, summed with the +1V reference and amplified through U331. The gain around the loop is unity so that the voltage drop across the current setting resistor (for example R3305-R4301) is 1.000 Volts regardless of the value of the voltage at +INPUT. K421, K422, and K431 switch the current setting resistors to obtain the various ranges of the ohmmeter.

TABLE DCX127.1
OHMS CURRENT SOURCE SWITCHING LOGIC

RANGE	CURRENT	K421	K422	K431
200 Ohm	1 mA	On	On	Off
2 kOhm	1 mA	On	On	Off
20 kOhm	100 uA	Off	Off	On
200 kOhm	10 uA	Off	On	Off
2 MOhm	1 uA	Off	Off	Off

The I_{comp} current source is composed of U321 and related resistors and operates in a similar bootstrap fashion. Because I_{comp} is connected across a low impedance (R9702), it is not necessary to buffer its input. I_{comp} is active only for the three lowest resistance ranges because lead resistance (r_W) becomes a negligible error factor when Rx $\geq$20 kOhms.

Incandescent lamps I451, I452 and clamping network Q4401, Q4402, D3401 provide overload protection to at least 100 Volts. JFETs are used as diodes because of their low gate leakage characteristic. U321B is inherently protected by R3201 or R3202.

Power Supplies <11>

The DCX-127 contains 5 different power supplies. The +5V power supply is conventional in design, consisting of bridge rectifier D3701 and filter capacitor C2701. Regulator U171 is a 3-terminal device with internal series pass darlington for low dropout voltage and current limiting at approximately 1.5 A. The other half of D3701 is used as part of the ±16V supplies.

The ±16V supplies are obtained from voltage triplers. D2701 clamps the voltage on C2702 so that it may never go more positive than the voltage on C2701. Since C2701 has charged to +10 V, positive power peaks cause C2702 to reach +30 V. This voltage is passed through D3702 and stored on C3701. It is then regulated by U471 to the final desired +16 V. R3703 and R3701 set the output voltage. D4701 and D3704 provide fault protection.

D3703 clamps the voltage on C3704 so that it may never go more positive than the voltage on C3703. Since C3703 has charged to -10 Vdc, negative power peaks cause C3704 to reach -30 V. This voltage is passed through D4703 and stored on C3702. It is then regulated by U472 to the final desired -16 V. R3704 and R3702 set the output voltage. D4702 and D3705 provide fault protection.

The floating power supplies are obtained from a second power transformer X171, operating with a 1:1.1 step-up ratio. X171 is connected to the secondary of X381 and contains Faraday shielding to isolate power line related interference from the floating DMM circuitry, and the circuit under test. The supplies consist of a pair of full wave center tapped rectifiers and filter capacitors. These drive 3-terminal regulators identical to those for the ±16V supplies but with different voltage setting resistors.

DCX-127 INPUT/OUTPUT CONNECTOR PIN ASSIGNMENTS

22 BIT DIGITAL INPUT/OUTPUT

1	Ground
2	Bit 0 (LSB)
3	Bit 1
4	Bit 2
5	Bit 3
6	Bit 4
7	Bit 5
8	Bit 6
9	Bit 7
10	Bit 8
11	Bit 9
12	Bit 10
13	Ground
14	Bit 11
15	Bit 12
16	Bit 13
17	Bit 14
18	Bit 15
19	Bit 16
20	Bit 17
21	Bit 18
22	Bit 19
23	Bit 20 (MSB)
24	Sign
25	Strobe

PROGRAM CONTROL INPUT

1	Bit 7 (MSB)
2	Bit 6
3	Bit 5
4	Bit 4
5	Bit 3
6	Bit 2
7	Bit 1
8	Bit 0 (LSB)
9	Ground

PROGRAM CONTROL OUTPUT

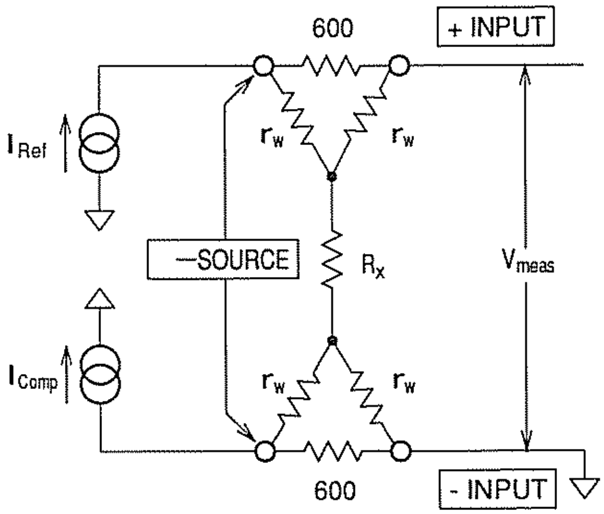
1	Delayed sweep gate
2	Reset
3	Data acquired
4	Trigger
5	Undefined
6	Sweep Gate
7	Channel A/B
8	Ground
9	Ground

8 BIT AUXILIARY PORTS

1	Bit 7 (MSB)
2	Bit 6
3	Bit 5
4	Bit 4
5	Bit 3
6	Bit 2
7	Bit 1
8	Bit 0 (LSB)
9	Ground

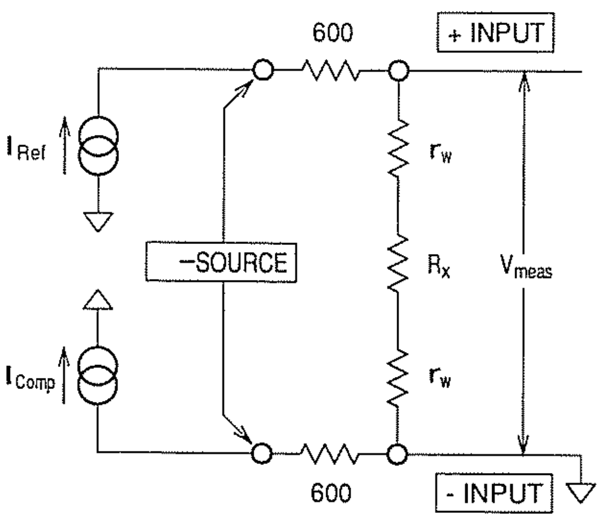
CONNECTOR J141

1	Ground
2	Bit 7 (MSB)
3	Bit 6
4	Bit 5
5	Bit 4
6	Bit 3
7	Bit 2
8	Bit 1
9	Bit 0 (LSB)
10	+5V
11	+5V
12	+15V
13	-15V
14-15	Ground



$$R_{meas} = R_x + 2r_w$$

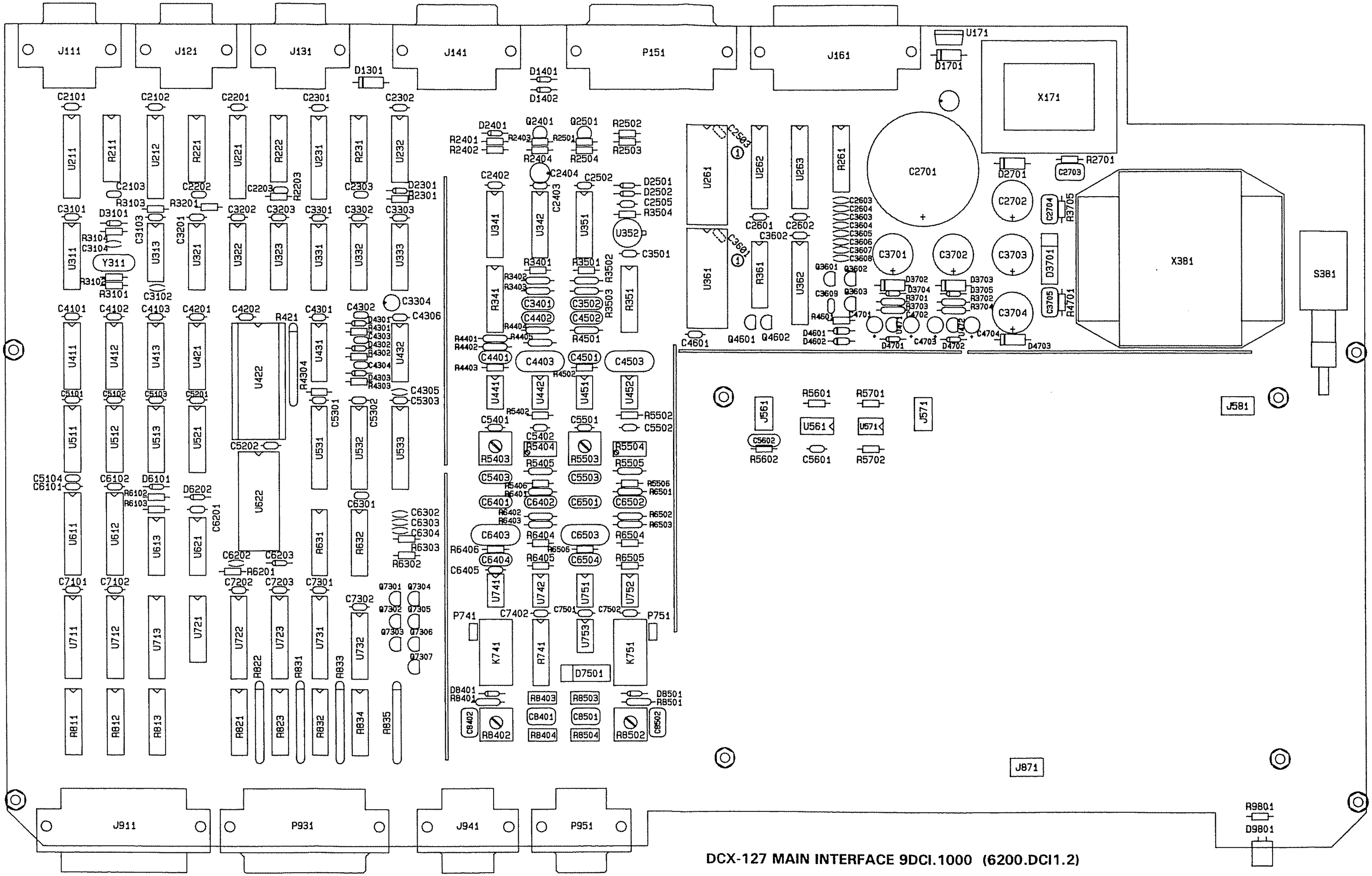
Figure DCX127.1 SIMPLIFIED DIAGRAM OF 2-WIRE OHMMETER OPERATION



$$R_{meas} = R_x \pm 0.02\Omega$$

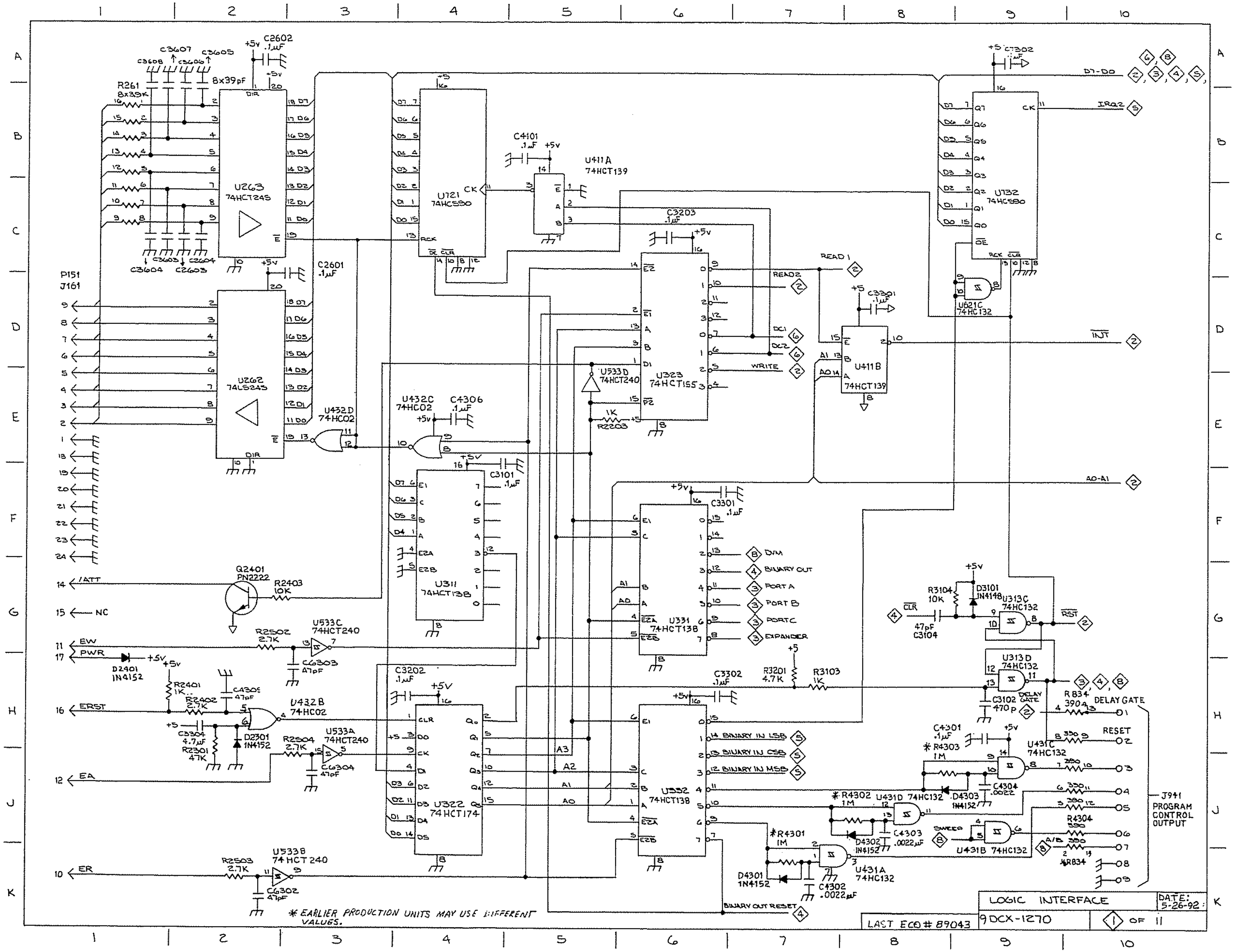
(if $r_W \leq 1.5\Omega$)

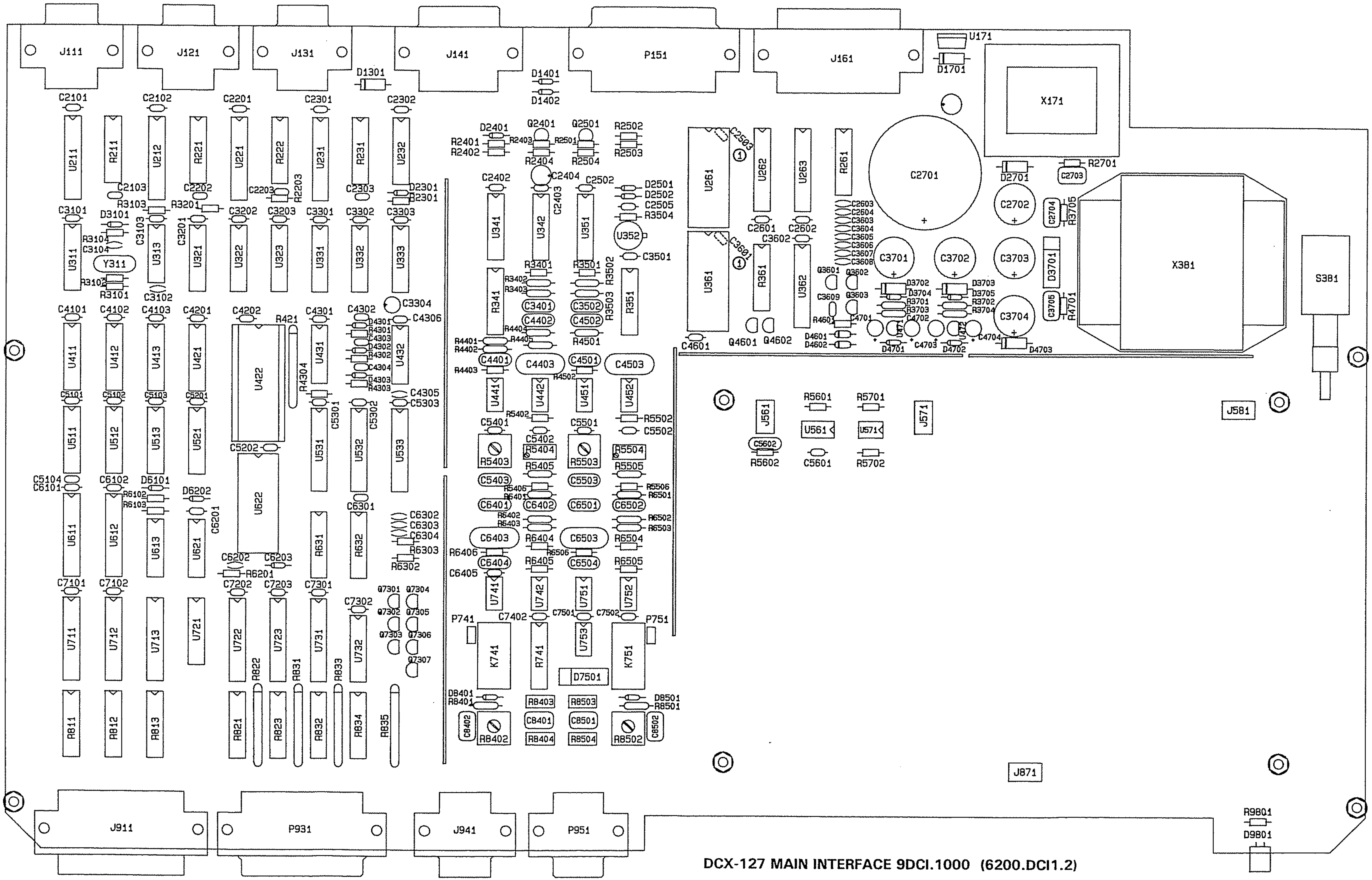
Figure DCX127.2 SIMPLIFIED DIAGRAM OF 4-WIRE OHMMETER OPERATION



DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

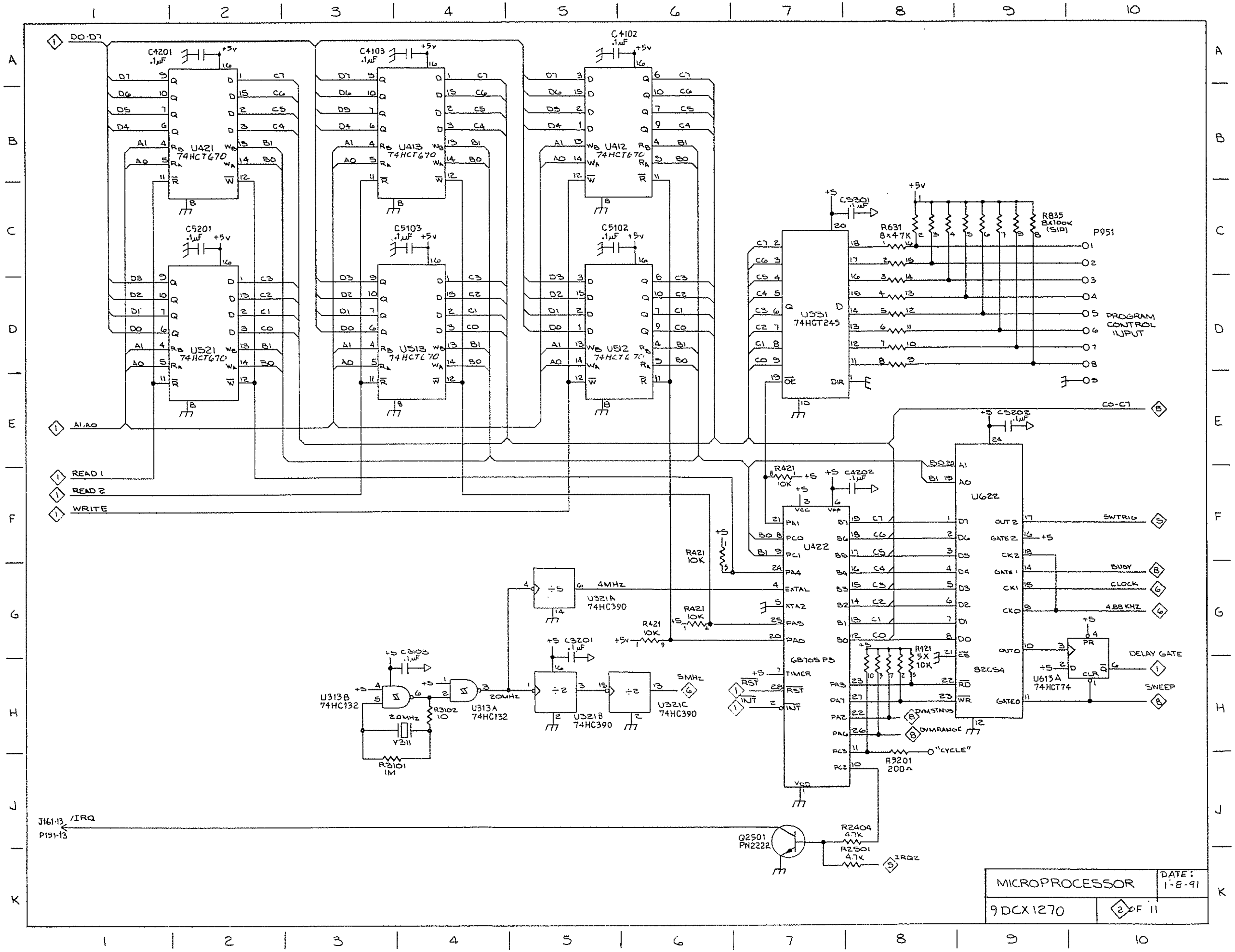
① Parts on solder side.


LOGIC INTERFACE
DATE: 5-26-92
9DCX-1270
1 OF 11
LAST ECO # 89043
* EARLIER PRODUCTION UNITS MAY USE DIFFERENT VALUES.
U263 74HCT245
U262 74LS245
U721 74HC590
U411A 74HCT139
U411B 74HCT139
U323 74HCT155
U132 74HC590
U621C 74HC132
U432C 74HC02
U432D 74HC02
U432B 74HC02
U311 74HCT138
U331 74HCT138
U332 74HCT138
U322 74HCT174
U533D 74HCT240
U533C 74HCT240
U533A 74HCT240
U533B 74HCT240
U313C 74HC132
U313D 74HC132
U431A 74HC132
U431B 74HC132
U431C 74HC132
U431D 74HC132
Q2401 PN2222
P151 J161
D7-D0
IRQ2
READ 1
READ2
WRITE
INT
A0-A1
RST
DELAY GATE
RESET
SWEEP
A/B
BINARY OUT RESET
BINARY IN LSB
BINARY IN CSB
BINARY IN MSB
D/M
BINARY OUT
PORT A
PORT B
PORT C
EXPANDER
J941 PROGRAM CONTROL OUTPUT
ATT
NC
EW
PWR
ERST
EA
ER

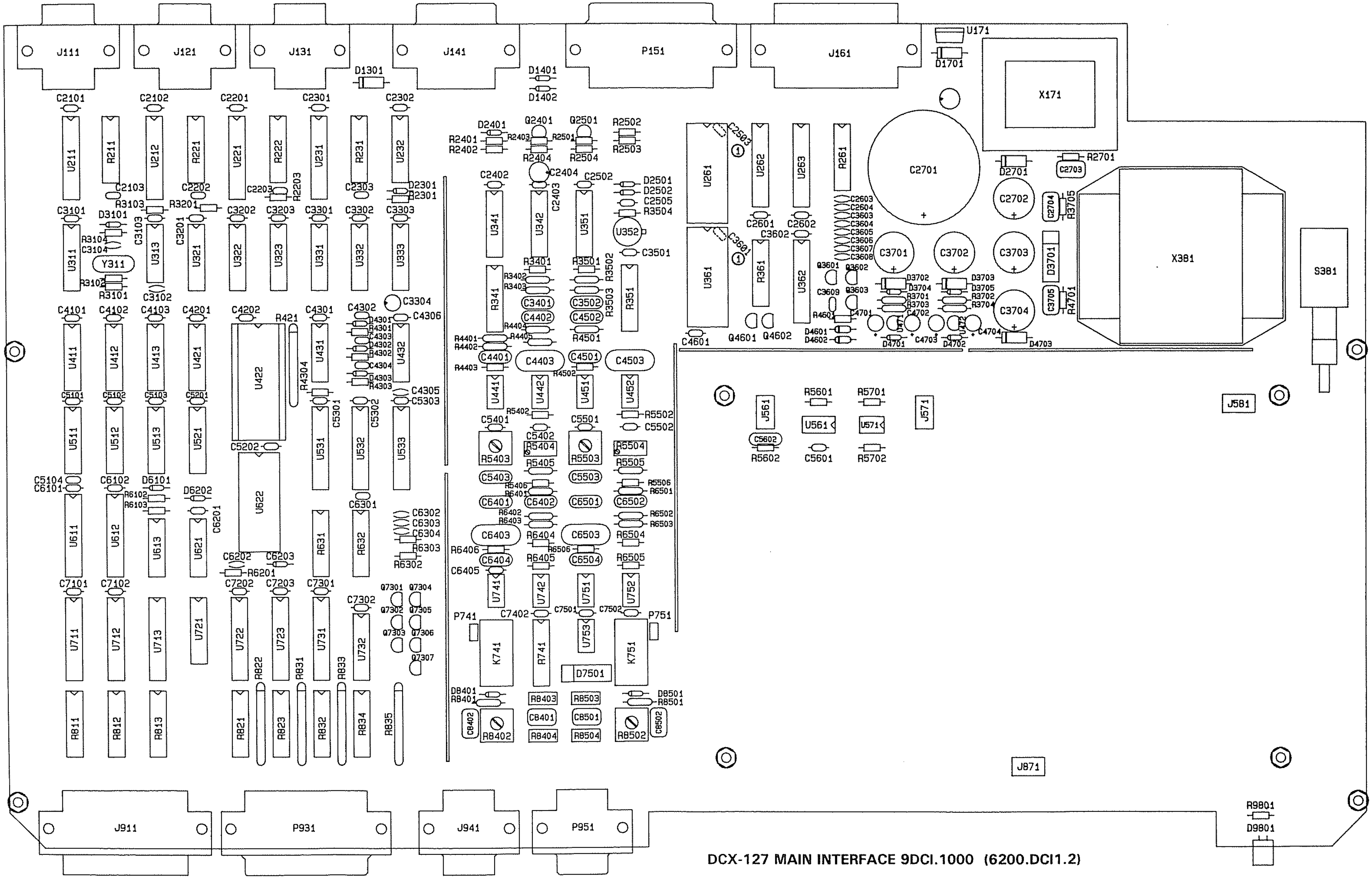


DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

① Parts on solder side.

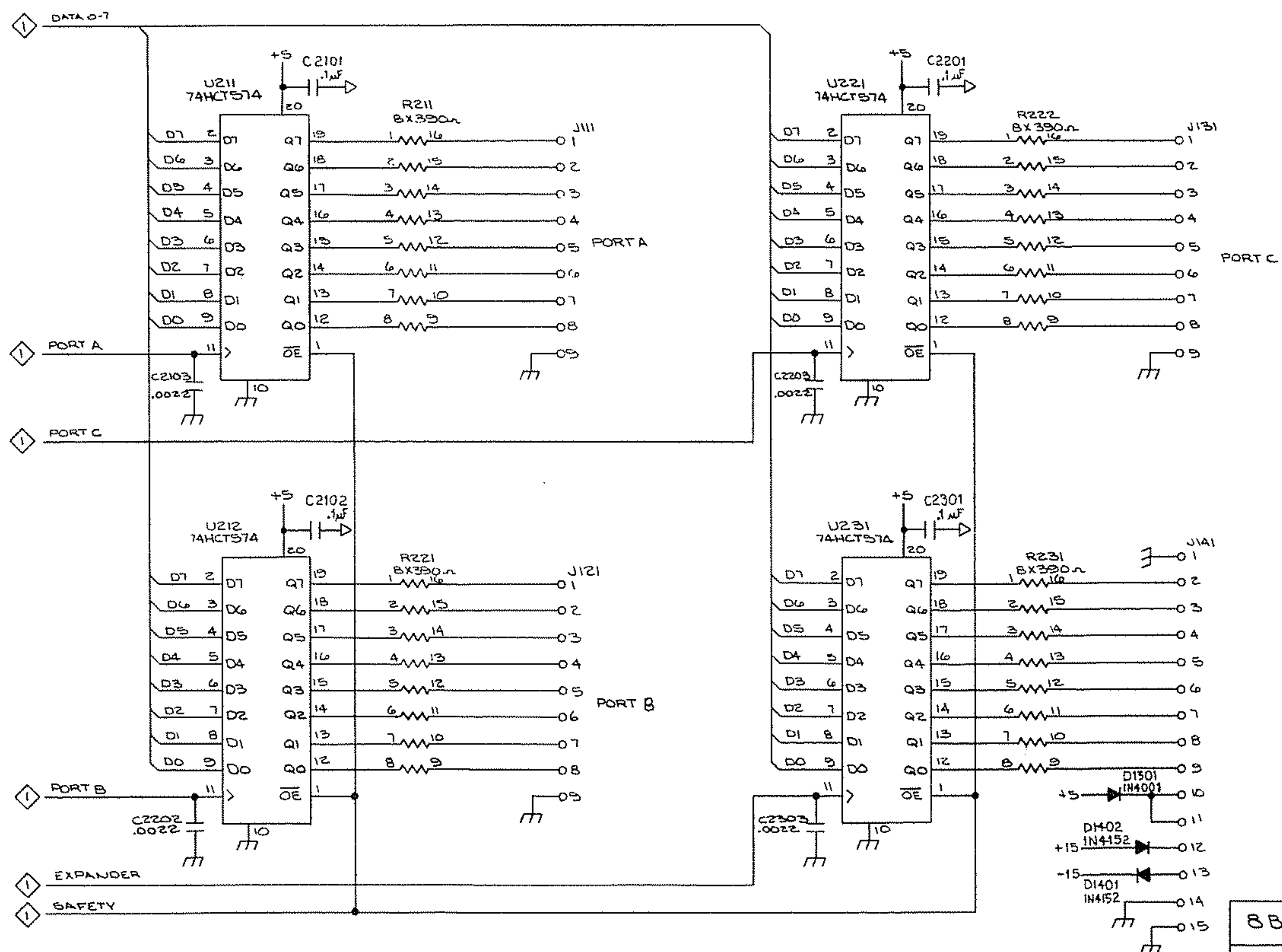


D0-D7
A1,A0
READ 1
READ 2
WRITE
U421 74HCT670
U521 74HCT670
U413 74HCT670
U513 74HCT670
U412 74HCT670
U512 74HCT670
C4201 .1µF
C5201 .1µF
C4103 .1µF
C5103 .1µF
C4102 .1µF
C5102 .1µF
U331 74HCT245
R631 8x4.7K
R835 8x100K (SIP)
P951
PROGRAM CONTROL INPUT
C0-C7
U622
82C54
SWTRIG
BUSY
CLOCK
4.88 KHZ
DELAY GATE
SWEEP
U613A 74HCT74
U422
68705P3
U321A 74HC390
4MHz
U321B 74HC390
U321C 74HC390
5MHz
U313B 74HC132
U313A 74HC132
20MHz
Y311
R3101 1M
R3102 10
DVMSTATUS
DVMRANGE
"CYCLE"
R9201 200Ω
J161-13 /IRQ
P151-13
Q2501 PN2222
R2404 4.7K
R2501 4.7K
IRQ2
MICROPROCESSOR
DATE: 1-8-91
9DCX1270
2 OF 11



DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

① Parts on solder side.

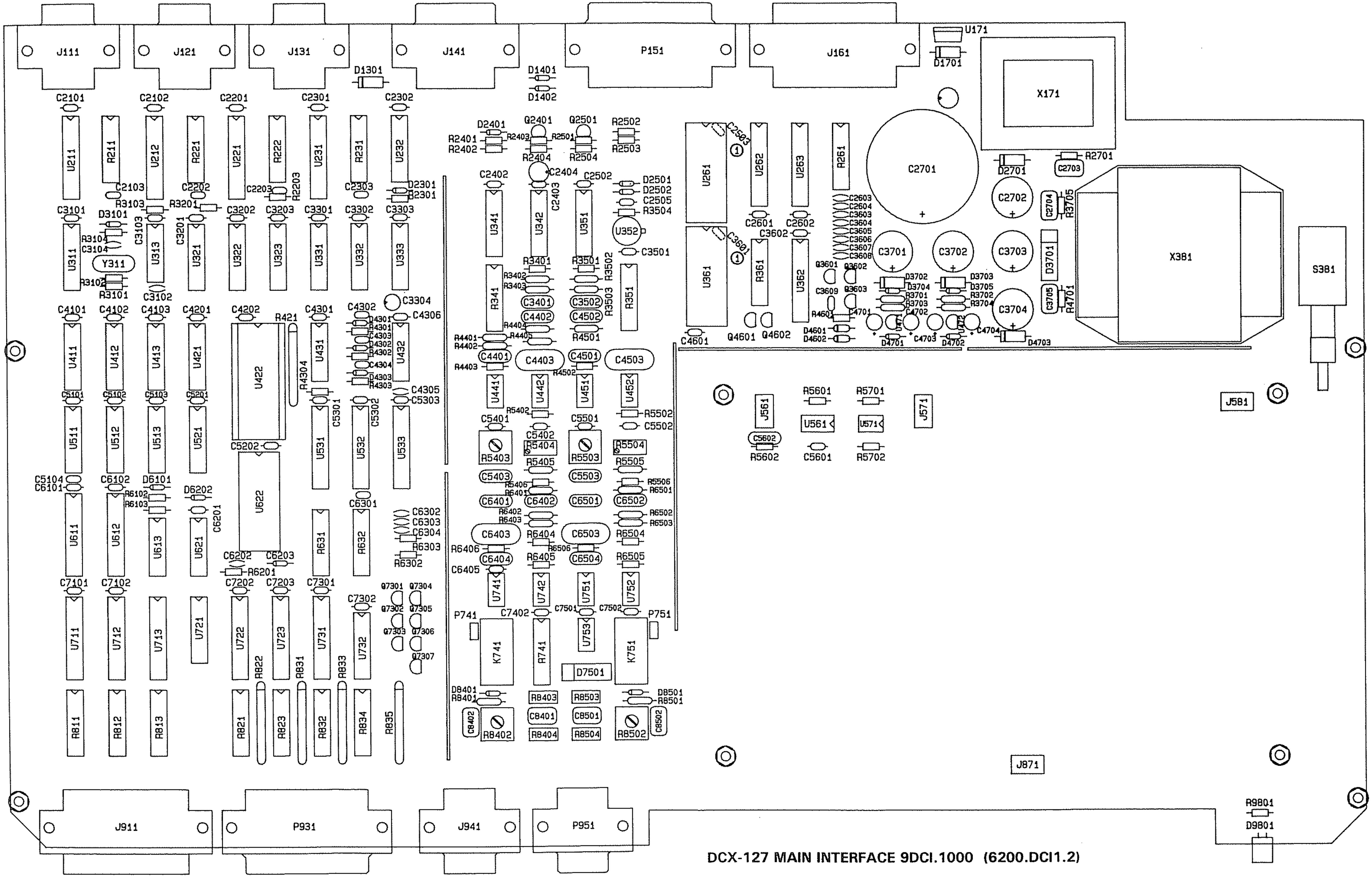


8 BIT OUTPUT PORTS

DATE: 1-8-91

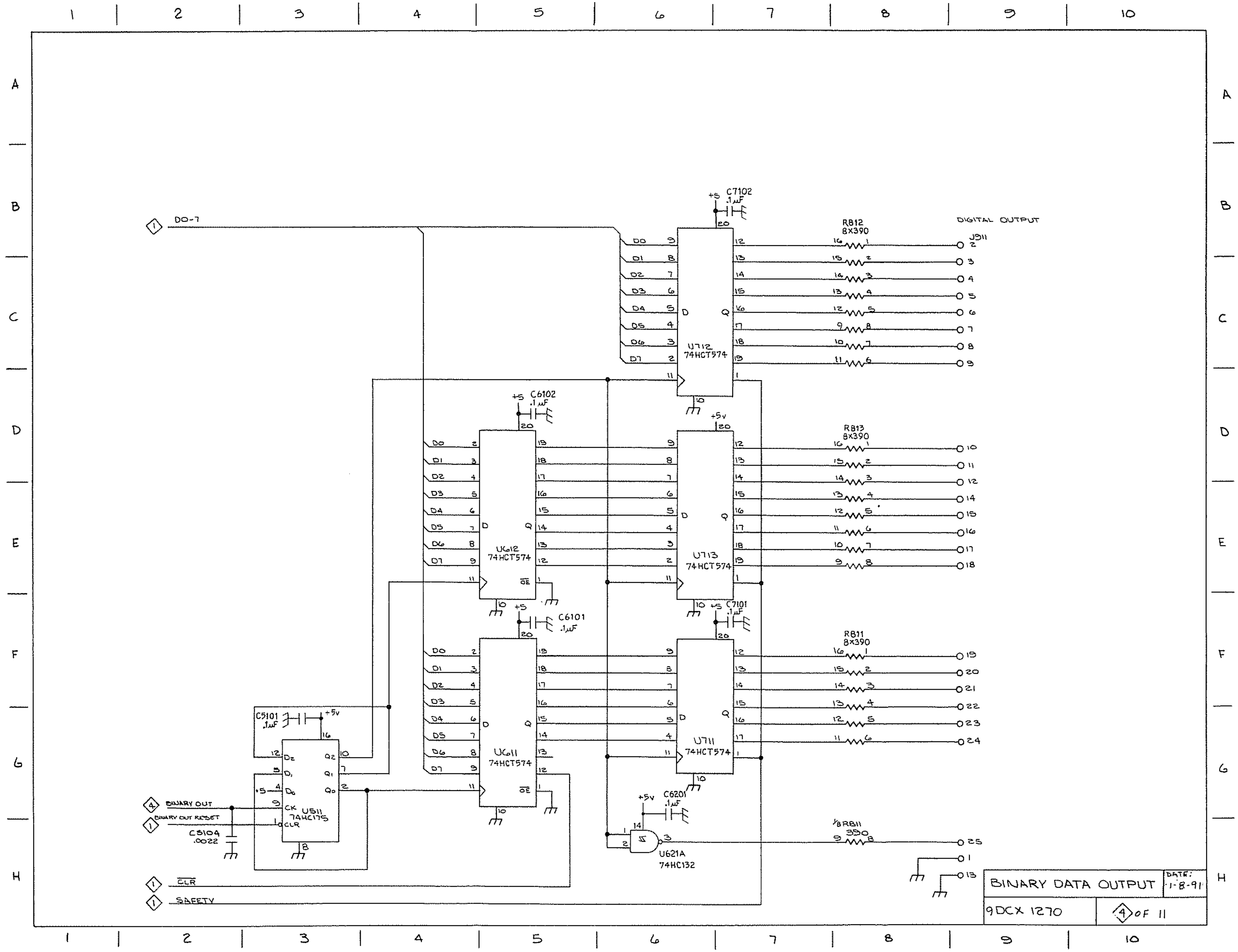
9DCX1270

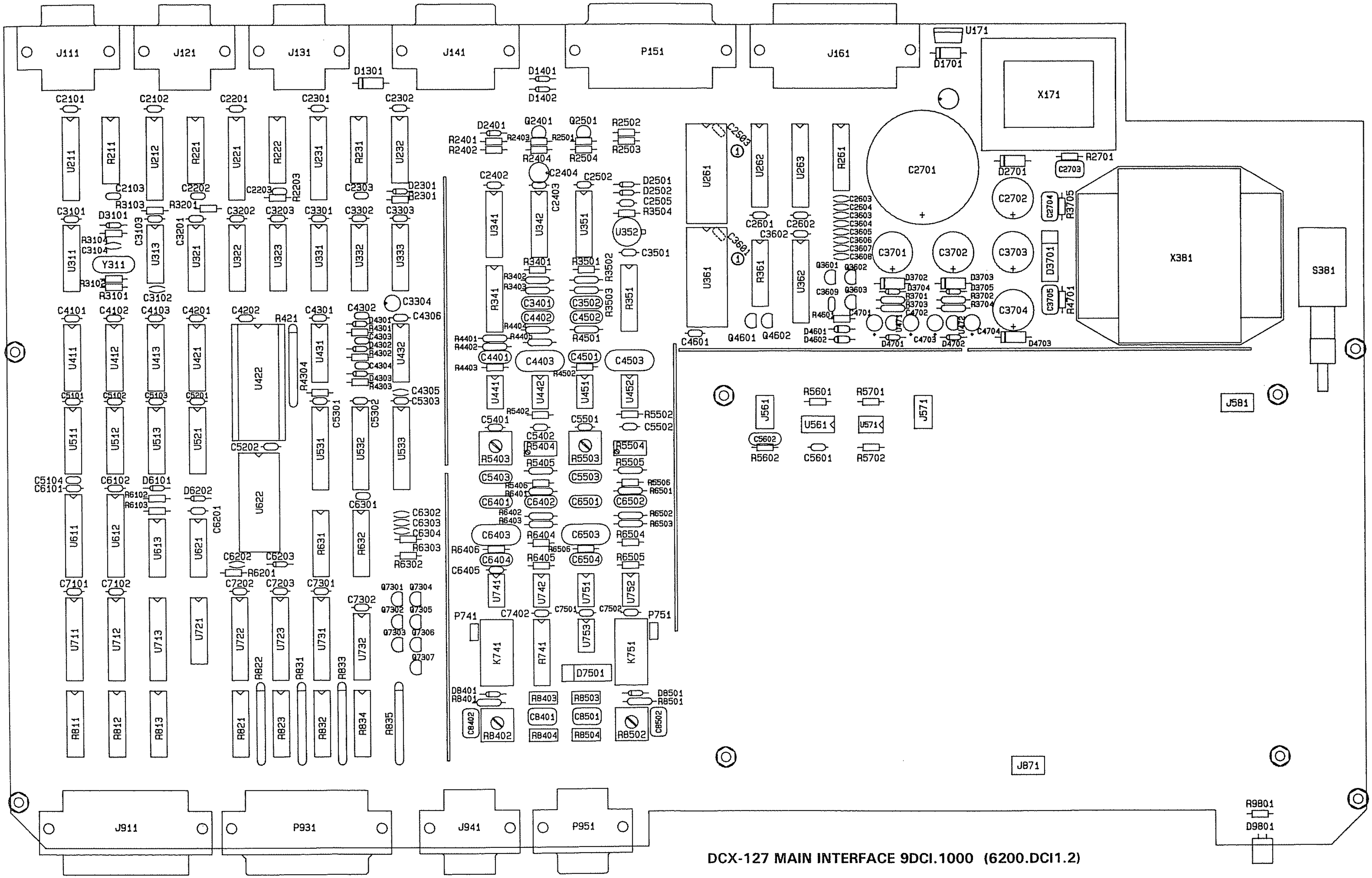
3 OF 11



DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

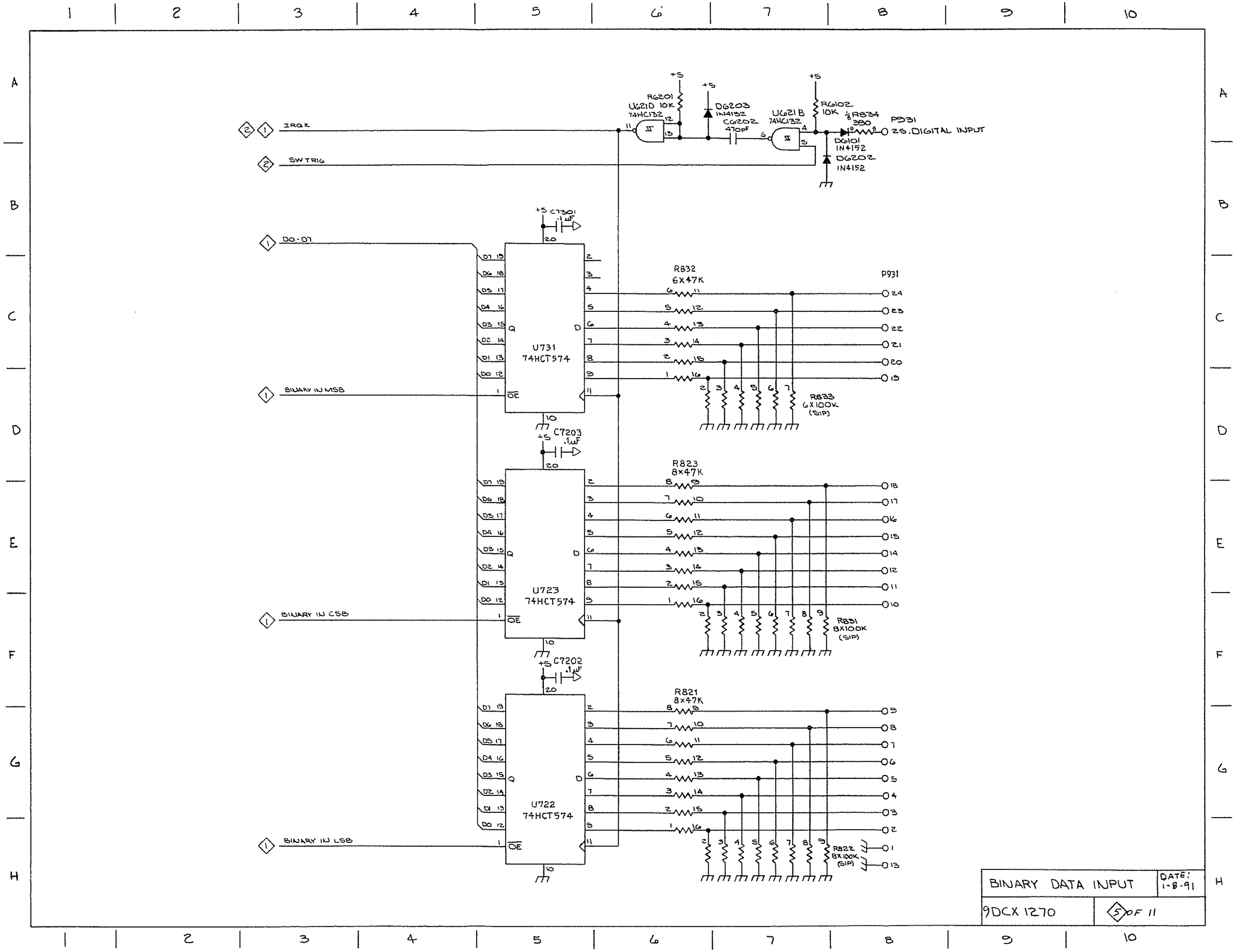
① Parts on solder side.


DO-7
DIGITAL OUTPUT
J511
RB12 8X390
RB13 8X390
RB11 8X390
C7102 .1µF
C6102 .1µF
C6101 .1µF
C7101 .1µF
C5101 .1µF
C6201 .1µF
C5104 .0022
U712 74HCT574
U612 74HCT574
U713 74HCT574
U611 74HCT574
U711 74HCT574
U511 74HC175
U621A 74HC132
BINARY OUT
BINARY OUT RESET
CLR
SAFETY
BINARY DATA OUTPUT
DATE: 1-8-91
9DCX 1270
4 OF 11

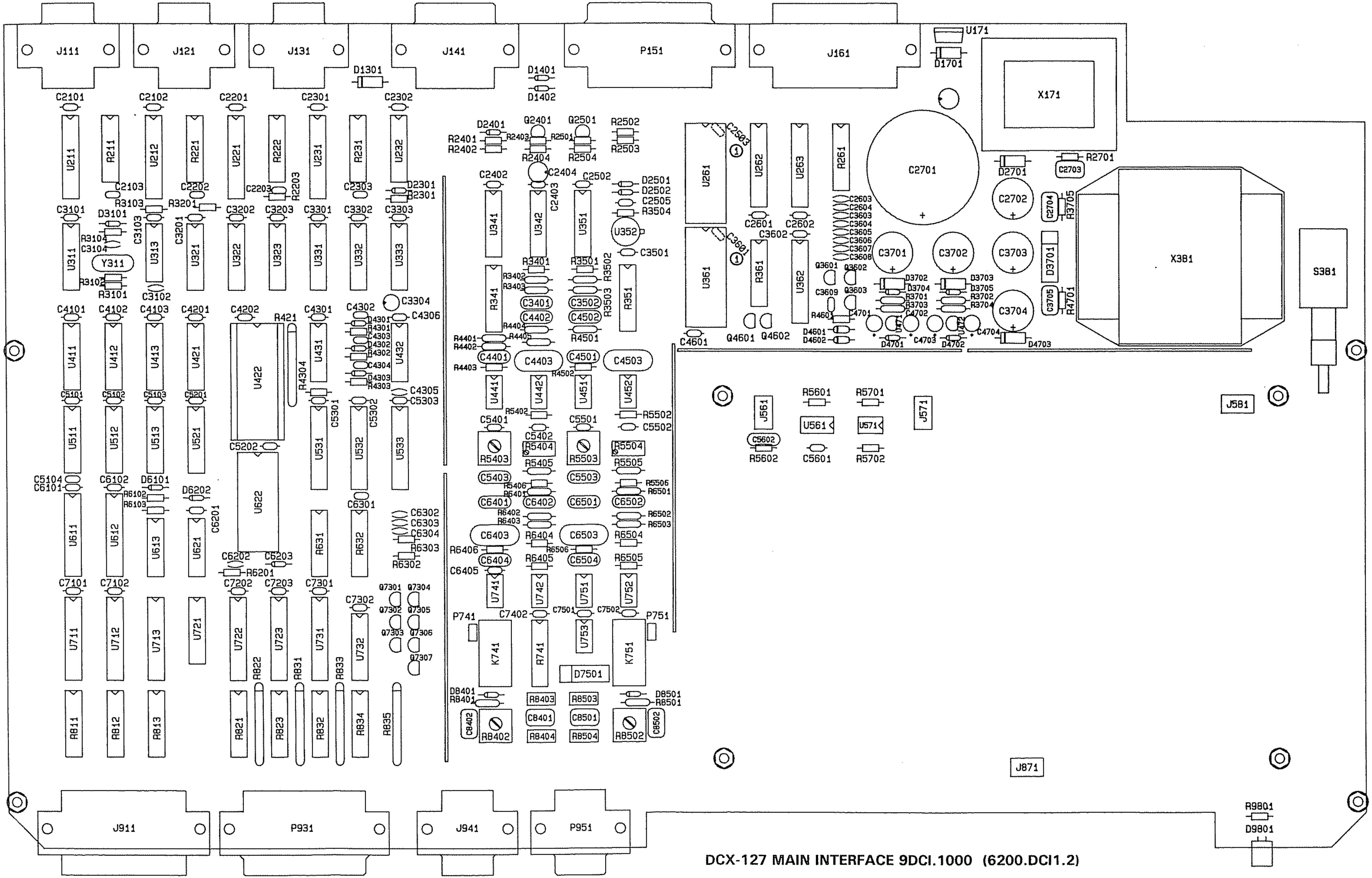


DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

① Parts on solder side.

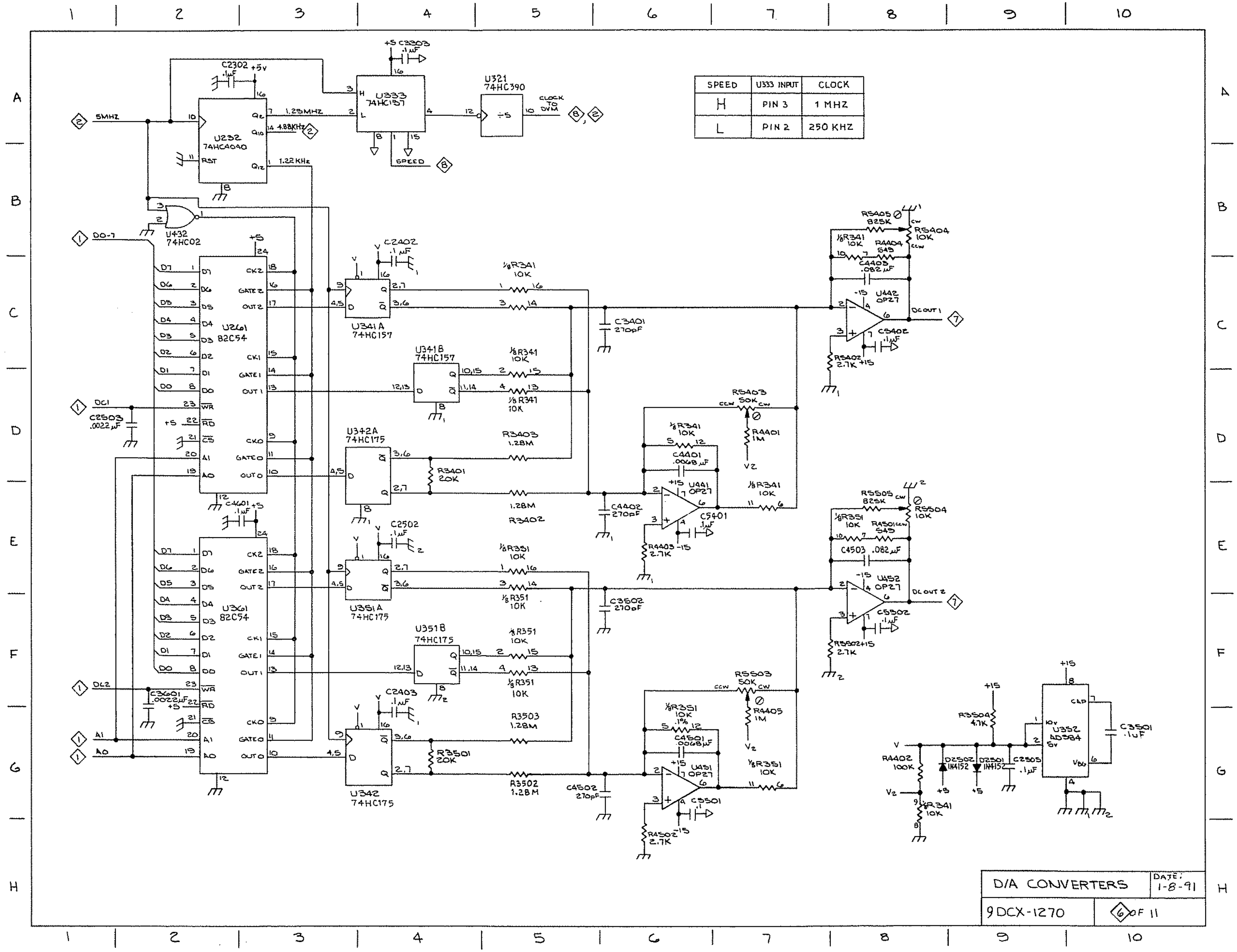


BINARY DATA INPUT	DATE: 1-8-91
9DCX 1270	5 OF 11



DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

① Parts on solder side.



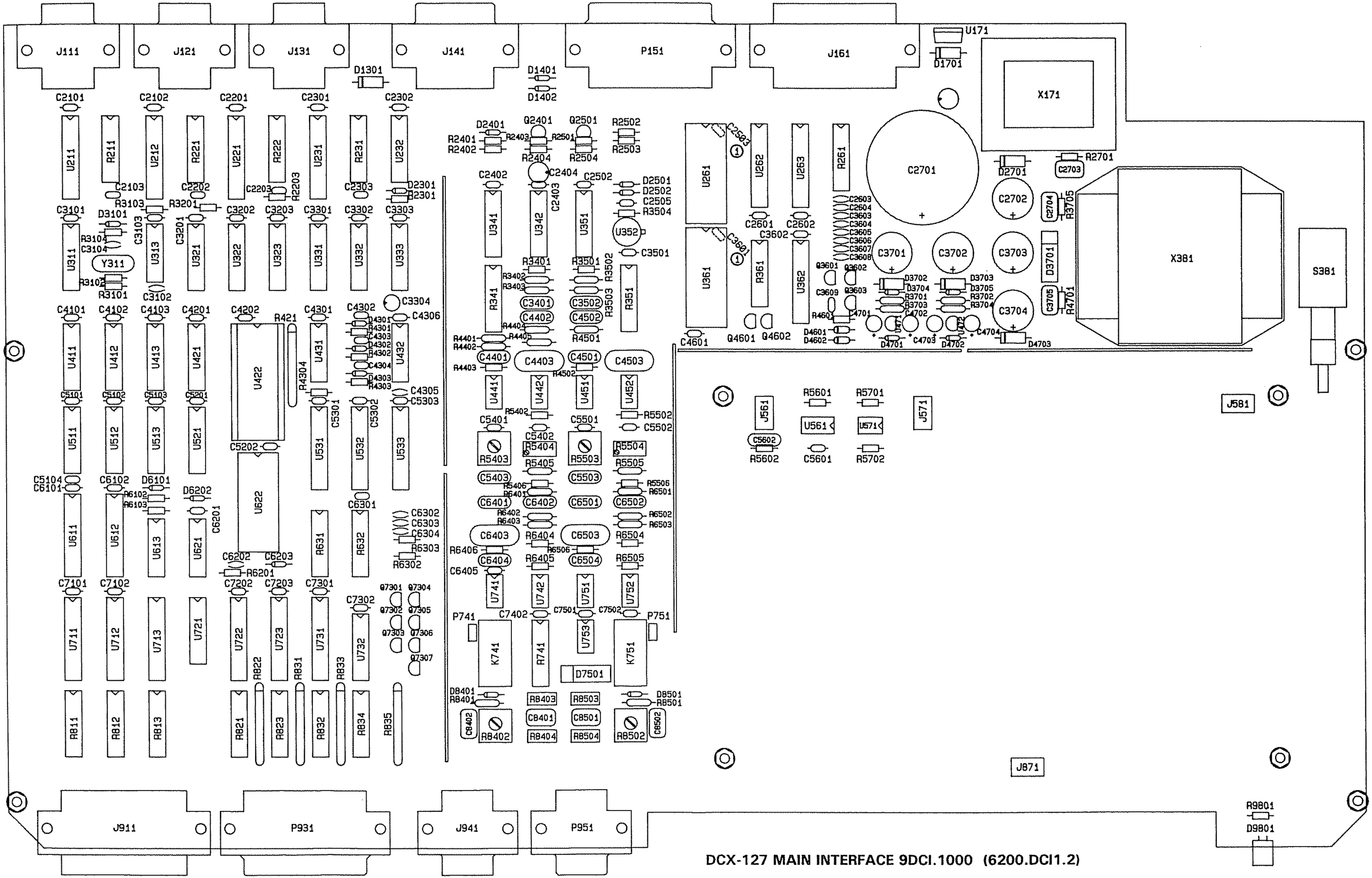
SPEED	U333 INPUT	CLOCK
H	PIN 3	1 MHZ
L	PIN 2	250 KHZ

D/A CONVERTERS

DATE: 1-8-91

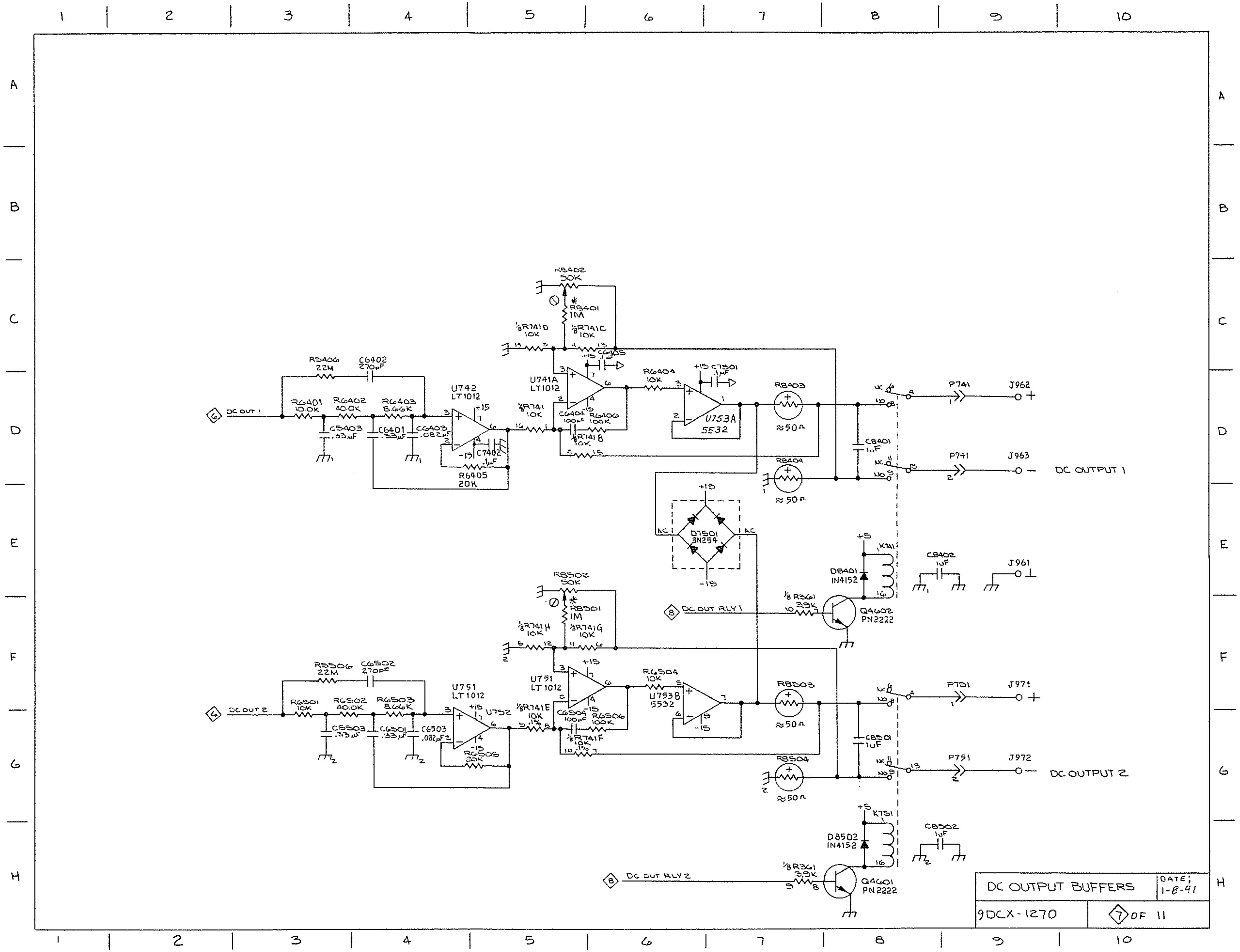
9DCX-1270

6 OF 11

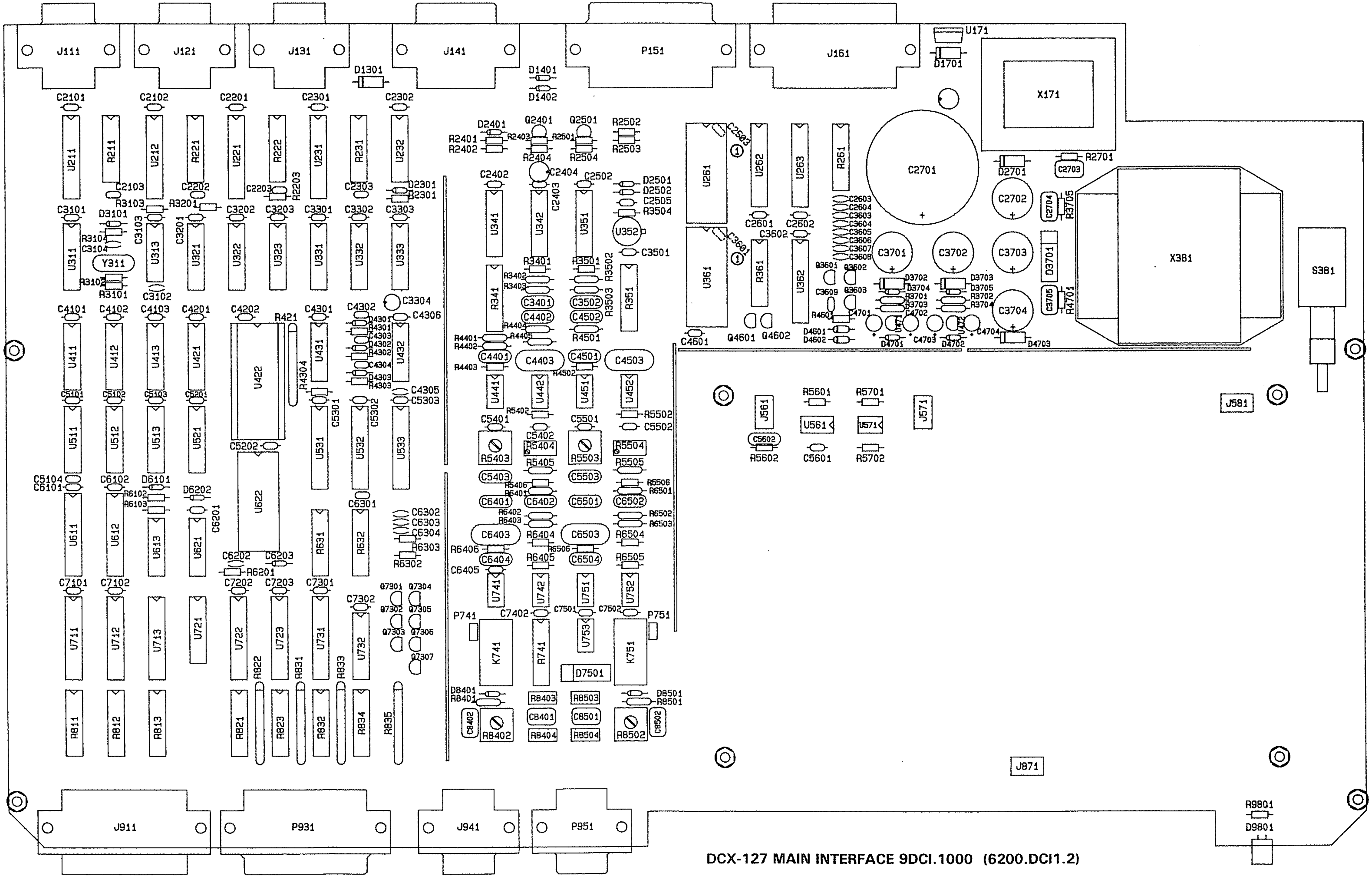


DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

① Parts on solder side.

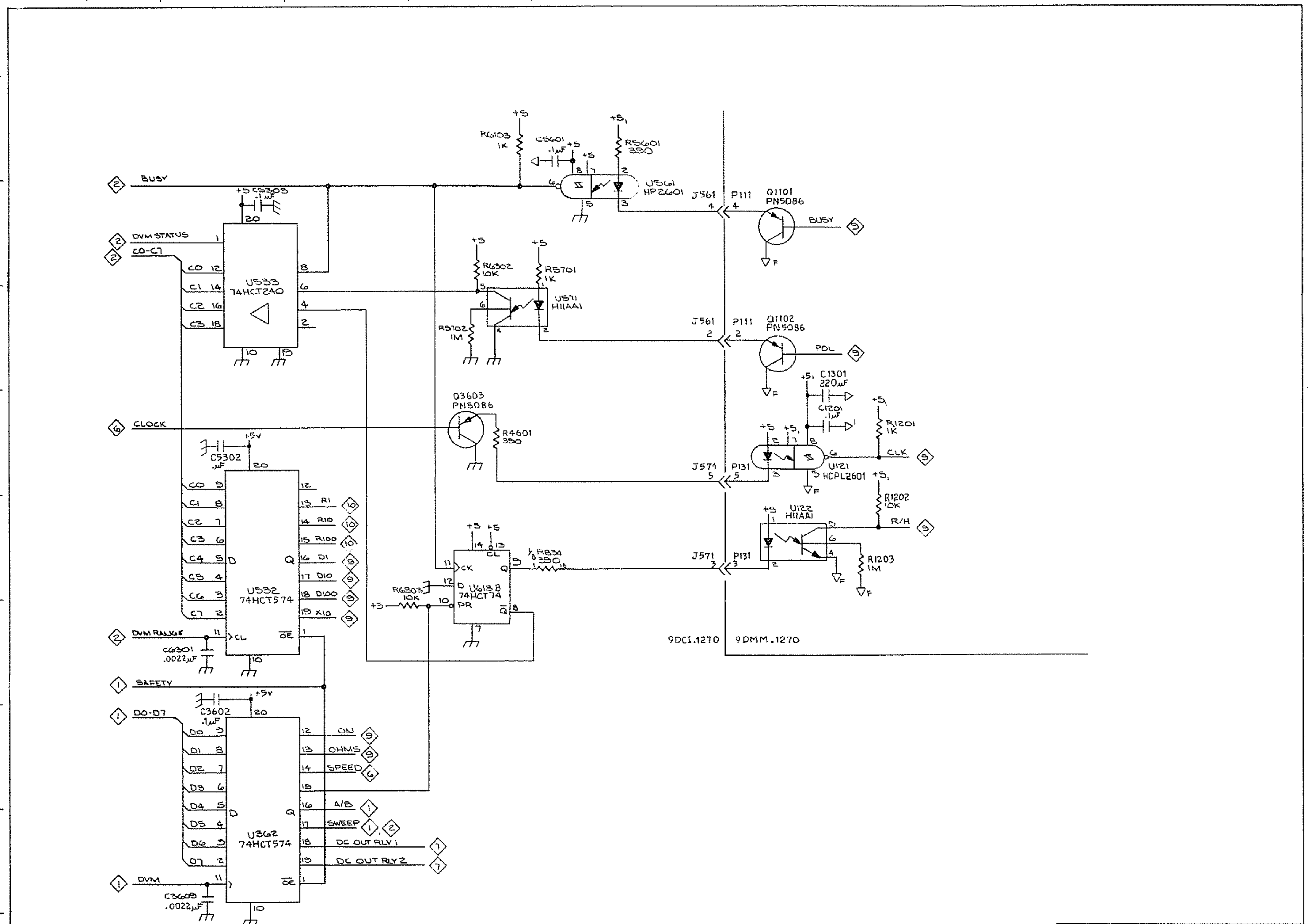


DC OUT 1
R5406 22M
C6402 270pF
R6401 10.0K
R6402 40.0K
R6403 8.66K
C5403 .33uF
C6401 .33uF
C6403 .082uF
U742 LT1012
C7402 .1uF
R6405 20K
R8402 50K
R8401 1M
1/8 R741D 10K
1/8 R741C 10K
U741A LT1012
C6405 .1uF
1/8 R741 10K
C6404 100pF
R6406 100K
1/8 R741B 10K
R6404 10K
C7501 .1uF
U753A 5532
R8403 ≈50Ω
R8404 ≈50Ω
C8401 1uF
P741
J962 +
J963 −
DC OUTPUT 1
D7501 3N254
AC
+15
−15
+5
K741
D8401 1N4152
1/8 R361 3.9K
Q4602 PN2222
DC OUT RLY 1
C8402 1uF
J961
R8502 50K
R8501 1M
1/8 R741H 10K
1/8 R741G 10K
DC OUT 2
R5506 22M
C6502 270pF
R6501 10K
R6502 40.0K
R6503 8.66K
C5503 .33uF
C6501 .33uF
C6503 .082uF
U751 LT1012
U752
R6505 35K
1/8 R741E 10K
U751 LT1012
C6504 100pF
R6506 100K
1/8 R741F 10K
R6504 10K
U753B 5532
R8503 ≈50Ω
R8504 ≈50Ω
C8501 1uF
P751
J971 +
J972 −
DC OUTPUT 2
K751
D8502 1N4152
1/8 R361 3.9K
Q4601 PN2222
DC OUT RLY 2
C8502 1uF
DC OUTPUT BUFFERS
DATE: 1-8-91
9DCX-1270
7 OF 11

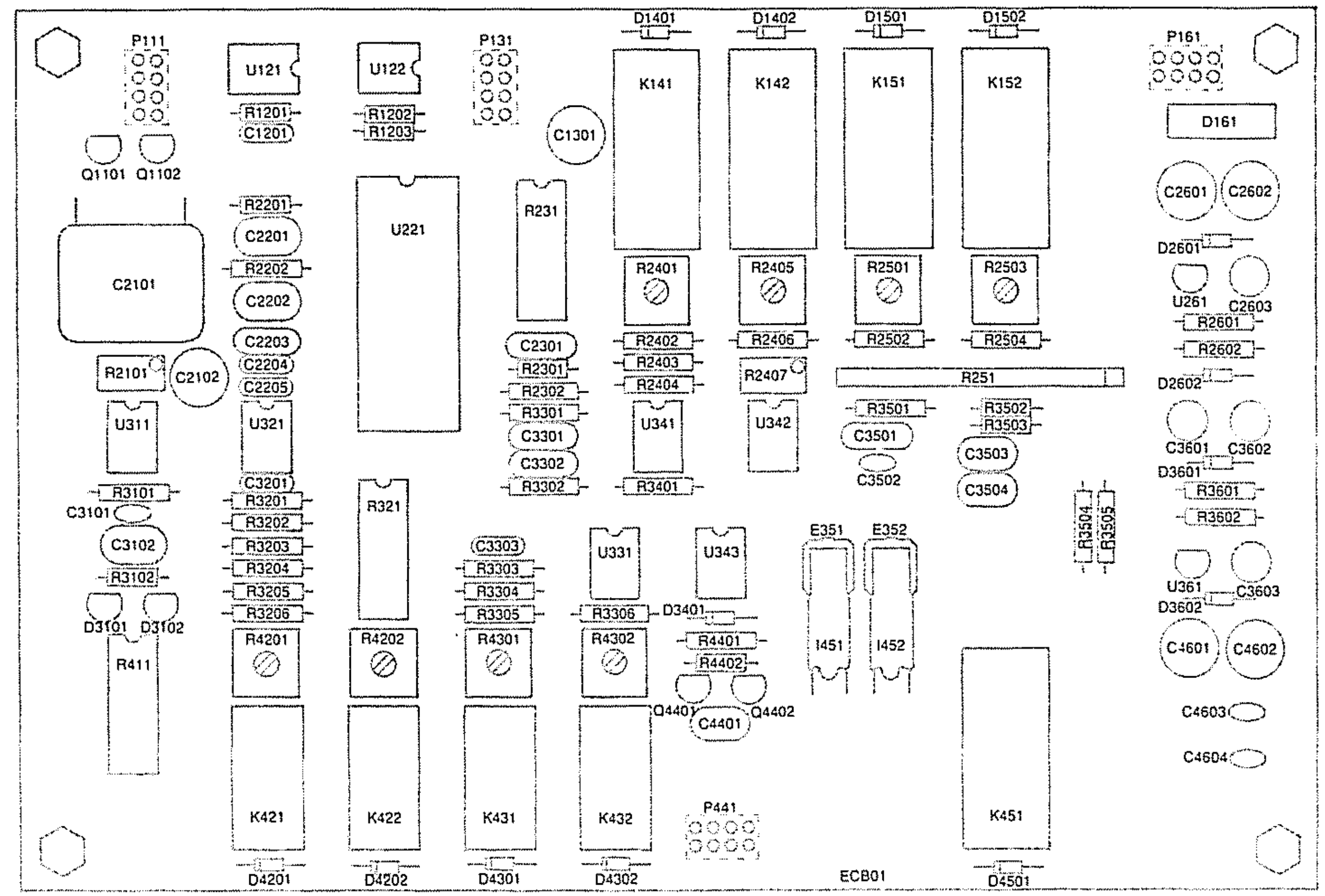


DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

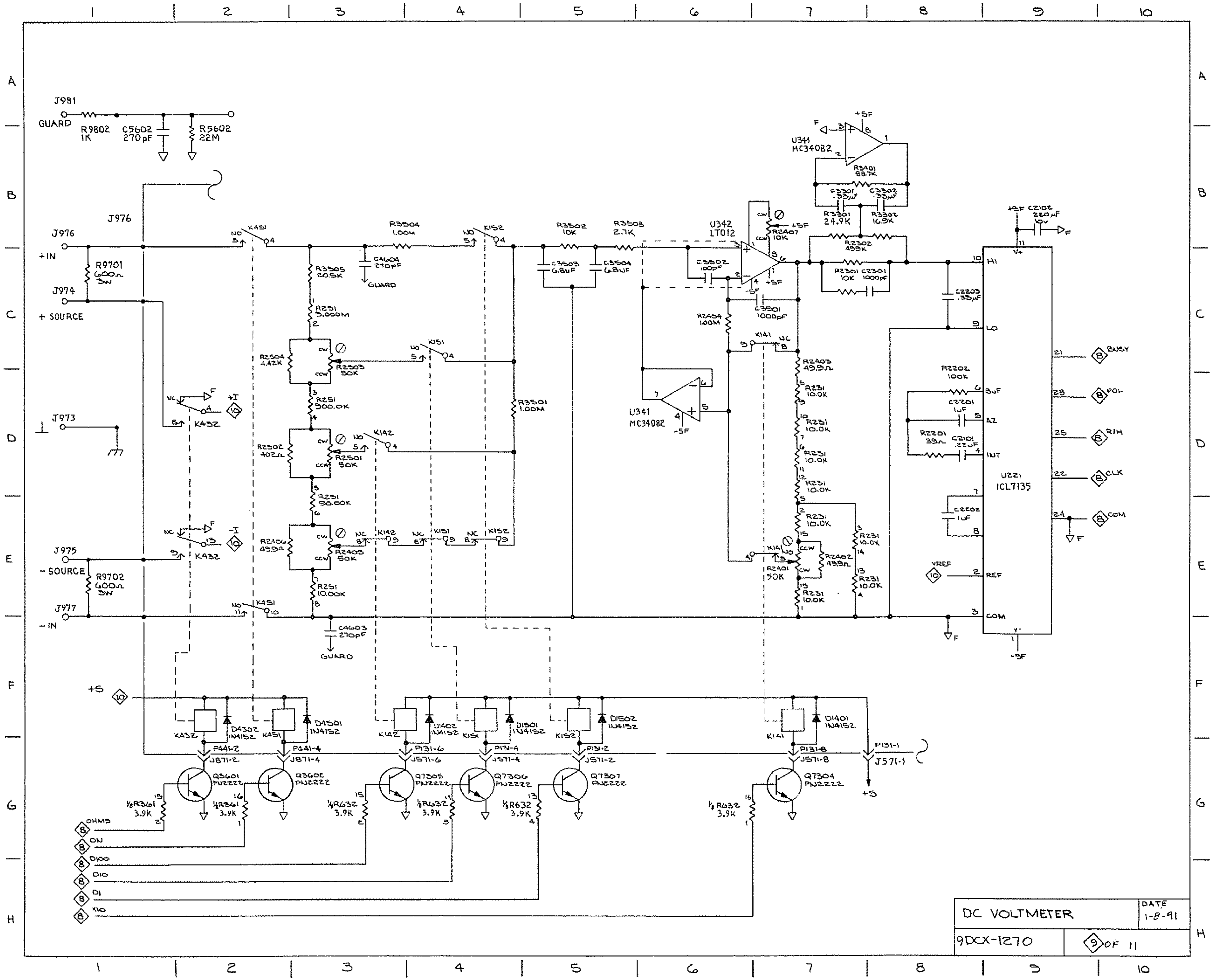
① Parts on solder side.

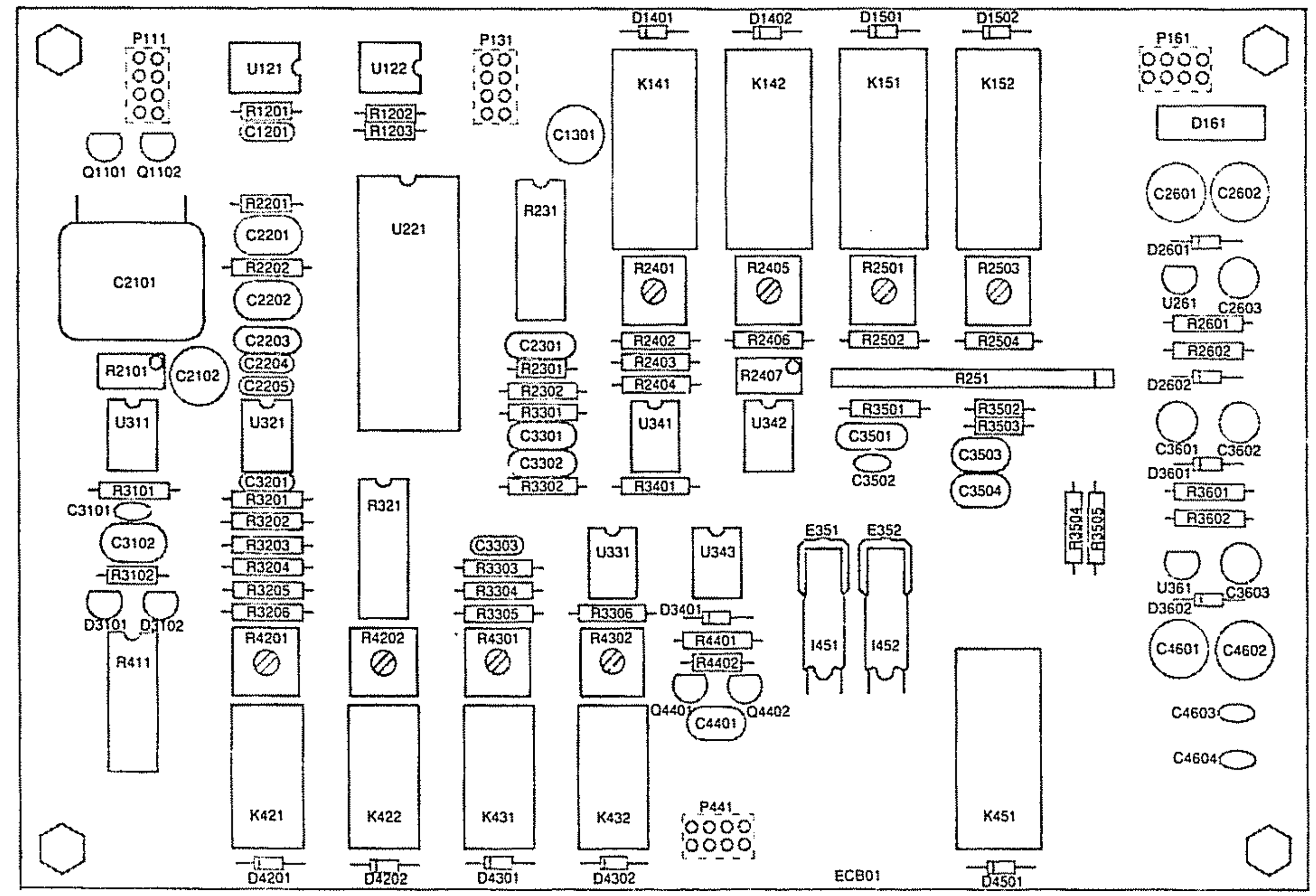


DVM INTERFACE	DATE: 1-8-91
9DCX-1270	8 OF 11

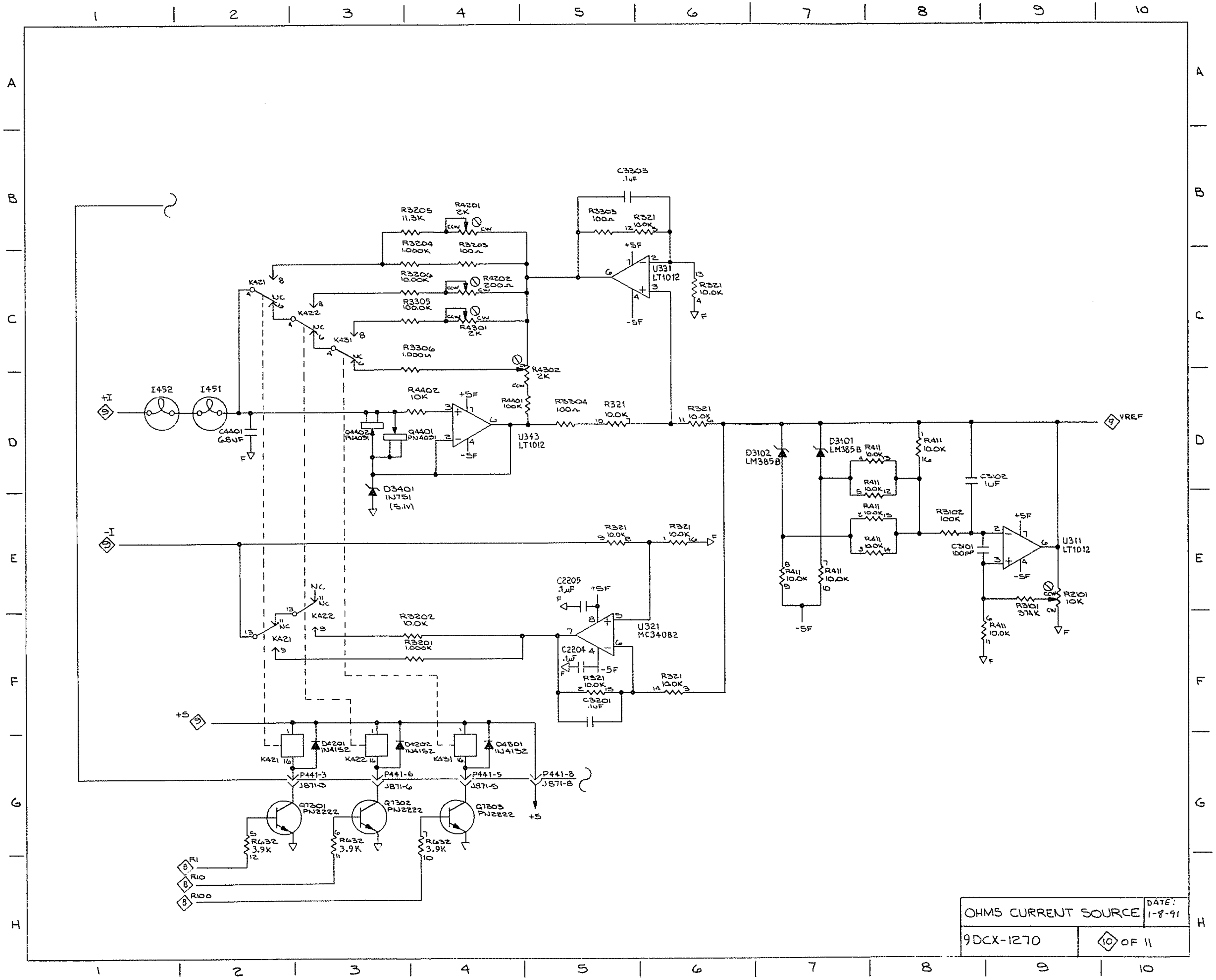


DCX-127 DIGITAL MULTIMETER (9DMM.1270)

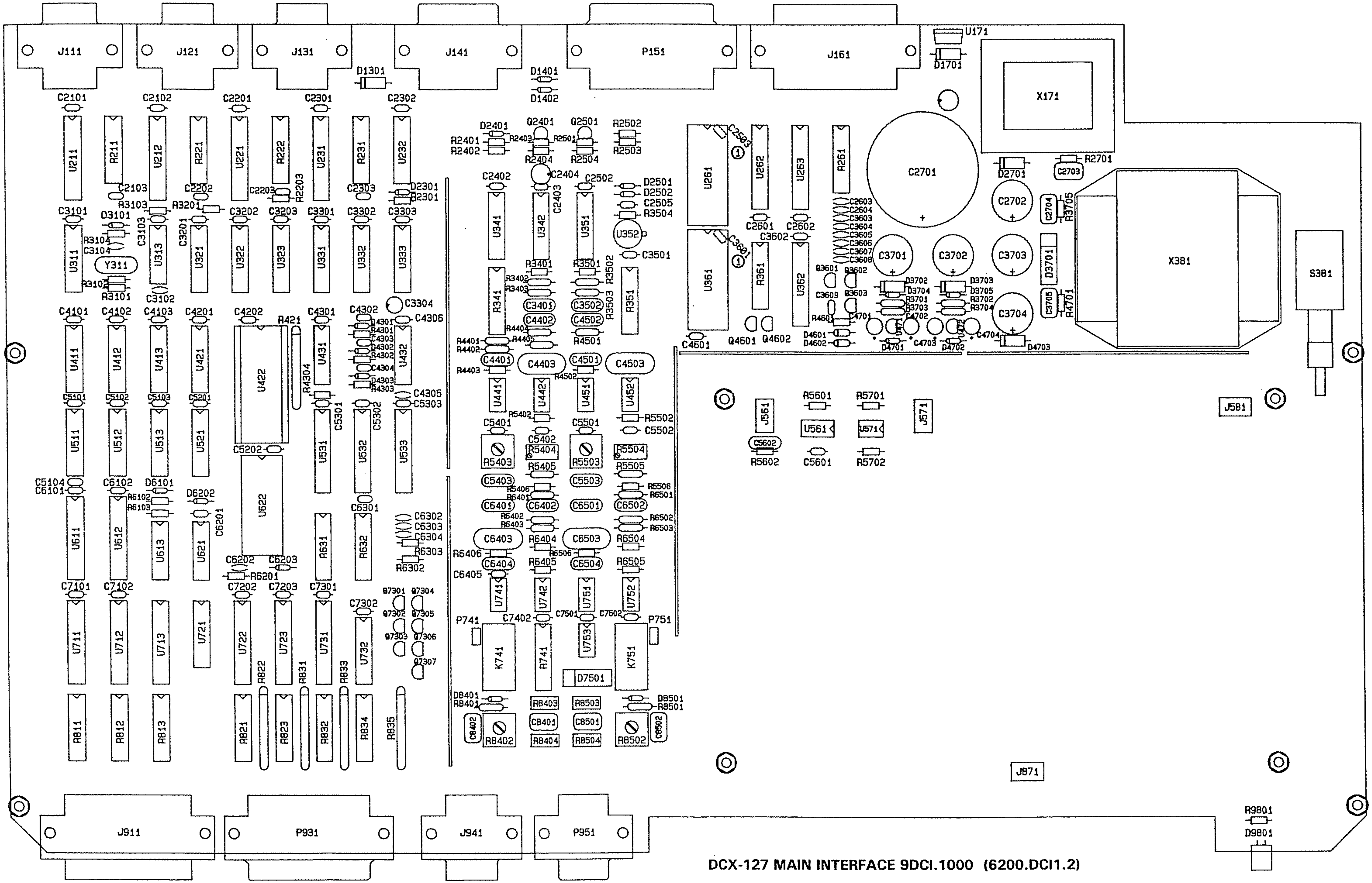

J981
GUARD
R9802 1K
C5602 270pF
R5602 22M
J976
+IN
R9701 600Ω 3W
J974
+ SOURCE
J973
J975
- SOURCE
R9702 600Ω 3W
J977
- IN
K451
K432
K142
K151
K152
K141
R3504 1.00M
R3505 20.5K
C4604 270pF
C4603 270pF
R251 9.000M
R2504 4.42K
R2503 50K
R251 900.0K
R2502 402Ω
R2501 50K
R251 90.00K
R2404 49.9Ω
R2405 50K
R251 10.00K
R3501 1.00M
R3502 10K
R3503 2.7K
C3503 6.8μF
C3504 6.8μF
U342 LT012
R2407 10K
C3502 100pF
C3501 1000pF
R2404 1.00M
U341 MC34082
R3401 88.7K
C3301 .33μF
C3302 .33μF
R3301 24.9K
R3302 16.9K
R2302 499K
R2301 10K
C2301 1000pF
R2403 49.9Ω
R231 10.0K
R2402 49.9Ω
R2401 50K
+5F
-5F
C2102 220μF 10v
C2203 .33μF
R2202 100K
C2201 1μF
R2201 39Ω
C2101 .22μF
C2202 1μF
U221 ICL7135
HI
LO
BUF
AZ
INT
REF
COM
V+
V-
VREF
BUSY
POL
R/H
CLK
COM
+5
D4302 1N4152
D4501 1N4152
D1402 1N4152
D1501 1N4152
D1502 1N4152
D1401 1N4152
P441-2
P441-4
P131-6
P131-4
P131-2
P131-8
P131-1
J871-2
J871-4
J571-6
J571-4
J571-2
J571-8
J571-1
Q3601 PN2222
Q3602 PN2222
Q7305 PN2222
Q7306 PN2222
Q7307 PN2222
Q7304 PN2222
1/8 R3601 3.9K
1/8 R632 3.9K
OHMS
ON
D100
D10
D1
X10
DC VOLTMETER
DATE 1-8-91
9DCX-1270
9 OF 11



DCX-127 DIGITAL MULTIMETER (9DMM.1270)

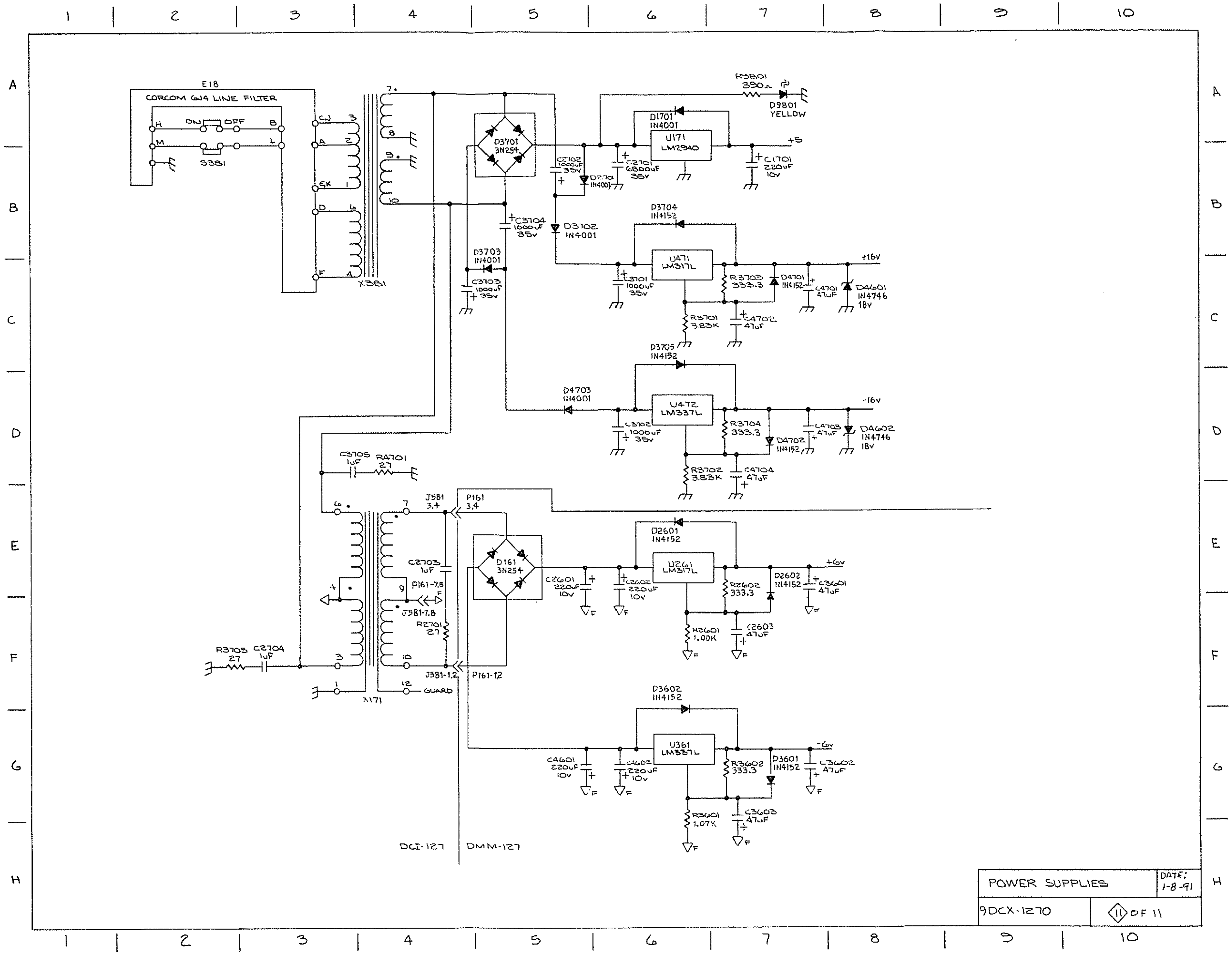


OHMS CURRENT SOURCE
DATE: 1-8-91
9DCX-1270
10 OF 11
+I
-I
VREF
+5
R1
R10
R100
I452
I451
C4401 6.8UF
K421
K422
K431
R3205 11.3K
R4201 2K
R3204 1.000K
R3203 100Ω
R3206 10.00K
R4202 200Ω
R3305 100.0K
R4301 2K
R3306 1.000M
R4302 2K
R4402 10K
R4401 100K
Q4402 PN4091
Q4401 PN4091
D3401 1N751 (5.1V)
U343 LT1012
R3304 100Ω
R321 10.0K
C3303 .1uF
R3303 100Ω
U331 LT1012
D3102 LM385B
D3101 LM385B
R411 10.0K
C3102 1uF
R3102 100K
C3101 100PF
U311 LT1012
R3101 374K
R2101 10K
C2205 .1uF
U321 MC34082
C2204 .1uF
R3202 10.0K
R3201 1.000K
C3201 .1uF
D4201 1N4152
D4202 1N4152
D4301 1N4152
P441-3 J871-3
P441-6 J871-6
P441-5 J871-5
P441-8 J871-8
Q7301 PN2222
Q7302 PN2222
Q7303 PN2222
R632 3.9K
+5F
-5F



DCX-127 MAIN INTERFACE 9DCI.1000 (6200.DCI1.2)

① Parts on solder side.


E18
CORCOM 6J4 LINE FILTER
ON
OFF
S381
X381
D3701
3N254
U171
LM2940
+5
D9801
YELLOW
R3801
390
D1701
IN4001
C2701
6800uF
35v
C1701
220uF
10v
C3704
1000uF
35v
D3702
IN4001
D3703
IN4001
C3703
1000uF
35v
D3704
IN4152
U471
LM317L
+16v
C3701
1000uF
35v
R3703
333.3
D4701
IN4152
C4701
47uF
D4601
IN4746
18v
R3701
3.83K
C4702
47uF
D3705
IN4152
D4703
IN4001
U472
LM337L
-16v
C3702
1000uF
35v
R3704
333.3
D4702
IN4152
C4703
47uF
D4602
IN4746
18v
R3702
3.83K
C4704
47uF
C3705
1uF
R4701
27
J581
3,4
P161
3,4
D161
3N254
D2601
IN4152
U261
LM317L
+6v
C2703
1uF
P161-7,8
J581-7,8
R2701
27
C2601
220uF
10v
C2602
220uF
10v
R2602
333.3
D2602
IN4152
C3601
47uF
R2601
1.00K
C2603
47uF
R3705
27
C2704
1uF
X171
J581-1,2
P161-1,2
GUARD
D3602
IN4152
U361
LM337L
-6v
C4601
220uF
10v
C4602
220uF
10v
R3602
333.3
D3601
IN4152
C3602
47uF
R3601
1.07K
C3603
47uF
DCI-127
DMM-127
POWER SUPPLIES
DATE: 1-8-91
9DCX-1270
11 OF 11

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1201	8E7	2172.0104	CAP CERAM 100V 20%	.1uF
C1301	8E7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2101	9D8	2555.0224	CAP POLYP 50V 2%	.22uF
C2102	9B9	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2201	9D8	2454.0105	CAP POLYE 50V 5%	1uF
C2202	9E8	2454.0105	CAP POLYE 50V 5%	1uF
C2203	9C8	2454.0334	CAP POLYE 50V 5%	.33uF
C2204	10F5	2172.0104	CAP CERAM 100V 20%	.1uF
C2205	10E5	2172.0104	CAP CERAM 100V 20%	.1uF
C2301	9C7	2276.0102	CAP MICA 100V 1%	.001uF
C2601	11F5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2602	11F6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2603	11F7	2932.0476	CAP AL-EL 25V 20%	47uF
C3101	10E8	2296.0101	CAP MICA 500V 1%	100pF
C3102	10D8	2454.0105	CAP POLYE 50V 5%	1uF
C3201	9F5	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	9B7	2454.0334	CAP POLYE 50V 5%	.33uF
C3302	9B8	2454.0334	CAP POLYE 50V 5%	.33uF
C3303	10B5	2172.0104	CAP CERAM 100V 20%	.1uF
C3501	9C7	2276.0102	CAP MICA 100V 1%	.001uF
C3502	9C6	2296.0101	CAP MICA 500V 1%	100pF
C3503	9C5	2555.0682	CAP POLYP 50V 2%	.0068uF
C3504	9C5	2555.0682	CAP POLYP 50V 2%	.0068uF
C3601	11E7	2932.0476	CAP AL-EL 25V 20%	47uF
C3602	11G7	2932.0476	CAP AL-EL 25V 20%	47uF
C3603	11H7	2932.0476	CAP AL-EL 25V 20%	47uF
C4401	10D2	2555.0682	CAP POLYP 50V 2%	.0068uF
C4601	11G5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4602	11G6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4603	9F3	2296.0271	CAP MICA 500V 1%	270pF
C4604	9C3	2296.0271	CAP MICA 500V 1%	270pF
D1401	9G7	3110.4152	DIODE SIGNAL	4152
D1402	9G4	3110.4152	DIODE SIGNAL	4152
D1501	9F4	3110.4152	DIODE SIGNAL	4152
D1502	9F5	3110.4152	DIODE SIGNAL	4152
D161	11E4	3140.0254	BRIDGE 2A 100V	3N254
D2601	11E6	3110.4152	DIODE SIGNAL	4152
D2602	11F7	3110.4152	DIODE SIGNAL	4152
D3101	10D7	3132.0385	DIODE PREC REF BG 1.2V	LM385B
D3102	10D7	3132.0385	DIODE PREC REF BG 1.2V	LM385B
D3401	10D3	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D3601	11G7	3110.4152	DIODE SIGNAL	4152
D3602	11G6	3110.4152	DIODE SIGNAL	4152
D4201	10F3	3110.4152	DIODE SIGNAL	4152
D4202	10F3	3110.4152	DIODE SIGNAL	4152
D4301	10F4	3110.4152	DIODE SIGNAL	4152
D4302	9F2	3110.4152	DIODE SIGNAL	4152
D4501	9F3	3110.4152	DIODE SIGNAL	4152
E351		4261.0001	FUSE CLIP PC	
E352		4261.0001	FUSE CLIP PC	

REPLACEABLE ELECTRICAL PARTS LIST: 9DMM.127

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
I451	10D2	4700.4840	LAMP INCANDESCENT	48V 40mA
I452	10D1	4700.4840	LAMP INCANDESCENT	48V 40mA
K141	9F7,9E7,9C7	4531.0001	RELAY PC LOW EMF	4POLE
K142	9F3,9E3,9D3	4531.0001	RELAY PC LOW EMF	4POLE
K151	9F4,9E4,9C4	4531.0001	RELAY PC LOW EMF	4POLE
K152	9F5,9E4,9B4	4531.0001	RELAY PC LOW EMF	4POLE
K421	10C2,10F2,10G2	4530.0002	RELAY PC LOW POWER	DPDT
K422	10C3,10E3,10F3	4530.0002	RELAY PC LOW POWER	DPDT
K431	10C3,10F4	4530.0002	RELAY PC LOW POWER	DPDT
K432	9D2,9E2,9F2	4530.0002	RELAY PC LOW POWER	DPDT
K451	9B2,9E2,9F2	4531.0001	RELAY PC LOW EMF	4POLE
P111	8C6,8D6	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P131	9G4,9G5,9G7	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P161	11E4,11F4	4221.0072	PLUG PC 2X.1 X.43	72 PIN
P441	8G2	4221.0072	PLUG PC 2X.1 X.43	72 PIN
Q1101	8C7	3211.5086	XSTR PNP TO92	PN5086
Q1102	8D7	3211.5086	XSTR PNP TO92	PN5086
Q4401	10D3	3214.4091	XSTR FET TO92	PN4091
Q4402	10D3	3214.4091	XSTR FET TO92	PN4091
R1201	8E7	1214.0102	RES 1/4W C FLM 5%	1K
R1202	8F7	1214.0103	RES 1/4W C FLM 5%	10K
R1203	8F7	1214.0105	RES 1/4W C FLM 5%	1M
R2101	10E9	4413.0103	POT TRIM PC 10 TURN	10K
R2201	9D8	1214.0390	RES 1/4W C FLM 5%	39
R2202	9D8	1136.1003	RES 1/8W M FLM 1%	100K
R2301	9C7	1214.0103	RES 1/4W C FLM 5%	10K
R2302	9C7	1136.4993	RES 1/8W M FLM 1%	499K
R231	9D7,9E7,10D5	1999.1002	RES NET DIP .1%	8 X 10K
R2401	9E7	4412.0503	POT TRIM PC ENC	50K
R2402	9E7	1136.4999	RES 1/8W M FLM 1%	49.9
R2403	9C7	1136.4999	RES 1/8W M FLM 1%	49.9
R2404	9C6	1136.1004	RES 1/8W M FLM 1%	1.00M
R2405	9E3	4412.0503	POT TRIM PC ENC	50K
R2406	9E2	1136.4999	RES 1/8W M FLM 1%	49.9
R2407	9B7	4413.0103	POT TRIM PC 10 TURN	10K
R2501	9D3	4412.0503	POT TRIM PC ENC	50K
R2502	9D3	1136.4020	RES 1/8W M FLM 1%	402
R2503	9C3	4412.0503	POT TRIM PC ENC	50K
R2504	9C3	1136.4421	RES 1/8W M FLM 1%	4.42K
R251	9C3,9D3,9E3	1980.1005	RES NET SIP .5% DIVIDER	10M
R2601	11F6	1139.1001	RES 1/8W M FLM .1%	1.00K
R2602	11E7	1139.3330	RES 1/8W M FLM .1%	333.3
R3101	10E9	1136.3743	RES 1/8W M FLM 1%	374K
R3102	10E8	1214.0104	RES 1/4W/C/FLM 5%	100K
R3201	11F3	1130.1001	RES 1/8W M FLM .1% T13	1.000K
R3202	10F3	1136.1002	RES 1/8W M FLM 1%	10.0K
R3203	10C4	1136.1000	RES 1/8W M FLM 1%	100
R3204	10C4	1130.1001	RES 1/8W M FLM .1% T13	1.000K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R3205	10B4	1136.1132	RES 1/8W M FLM 1%	11.3K
R3206	10C4	1130.1002	RES 1/8W M FLM .1% T13	10.00K
R321	10E-F5,10B-F6,	1999.1002	RES NET DIP .1%	8 X 10K
R3301	9B7	1136.2492	RES 1/8W M FLM 1%	24.9K
R3302	9B8	1136.1692	RES 1/8W M FLM 1%	16.9K
R3303	10B5	1136.1000	RES 1/8W M FLM 1%	100
R3304	10D5	1136.1000	RES 1/8W M FLM 1%	100
R3305	10C4	1130.1003	RES 1/8W M FLM .1% T13	100.0K
R3306	10C4	1139.1004	RES 1/8W M FLM .1%	1.00M
R3401	9B7	1136.8872	RES 1/8W M FLM 1%	88.7K
R3501	9D4	1136.1004	RES 1/8W M FLM 1%	1.00M
R3502	9B5	1214.0103	RES 1/4W C FLM 5%	10K
R3503	9B5	1214.0272	RES 1/4W C FLM 5%	2.7K
R3504	9B3	1136.1004	RES 1/8W M FLM 1%	1.00M
R3505	9C3	1136.2052	RES 1/8W M FLM 1%	20.5K
R3601	11H6	1136.1071	RES 1/8W M FLM 1%	1.07K
R3602	11G7	1139.3330	RES 1/8W M FLM .1%	333.3
R411	10D7,10E7,10D8,10F9	1999.1002	RES NET DIP .1%	8 X 10K
R4201	10B4	4412.0202	POT TRIM PC ENC	2K
R4202	10C4	4412.0201	POT TRIM PC ENC	200
R4301	10C4	4412.0202	POT TRIM PC ENC	2K
R4302	10C5	4412.0202	POT TRIM PC ENC	2K
R4401	10D5	1136.1003	RES 1/8W M FLM 1%	100K
R4402	10D4	1214.0103	RES 1/4W C FLM 5%	10K
U121	8E6	3630.2601	OPTOCOUPLER GATE	HCPL2601
U122	8F6	3630.0001	OPTO-ISOLATOR	H11AA1
U221	9C9,9D9,9F9	3441.7135	CONVERTER A/4.5DIGIT	ICL7135
U261	11E6	3430.1317	VOLT REG POS VAR TO92	LM317L
U311	10E9	3411.1012	OP AMP SINGLE	LT1012
U321	10F5	3412.0082	OP AMP DUAL	MC34082
U331	10C6	3411.1012	OP AMP SINGLE	LT1012
U341	9D6	3412.0082	OP AMP DUAL	MC34082
U342	9C6	3411.1012	OP AMP SINGLE	LT1012
U343	10D4	3411.1012	OP AMP SINGLE	LT1012
U361	11G6	3431.1337	VOLT REG NEG VAR TO92	LM337L

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C1701	11A7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2101	3C4	2172.0104	CAP CERAM 100V 20%	.1uF
C2102	3F4	2172.0104	CAP CERAM 100V 20%	.1uF
C2103	3E3	2172.0222	CAP CERAM 100V 20%	.0022uF
C2201	3C7	2172.0104	CAP CERAM 100V 20%	.1uF
C2202	3G3	2172.0222	CAP CERAM 100V 20%	.0022uF
C2203	3E7	2172.0222	CAP CERAM 100V 20%	.0022uF
C2301	3F7	2172.0104	CAP CERAM 100V 20%	.1uF
C2302	6A3	2172.0104	CAP CERAM 100V 20%	.1uF
C2303	3G6	2172.0222	CAP CERAM 100V 20%	.0022uF
C2402	6C4	2172.0104	CAP CERAM 100V 20%	.1uF
C2403	6F4	2172.0104	CAP CERAM 100V 20%	.1uF
C2404	6F4	2172.0104	CAP CERAM 100V 20%	.1uF
C2502	6E4	2172.0104	CAP CERAM 100V 20%	.1uF
C2503	6D2	2172.0222	CAP CERAM 100V 20%	.0022uF
C2505	6G9	2172.0104	CAP CERAM 100V 20%	.1uF
C2601	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C2602	1A2	2172.0104	CAP CERAM 100V 20%	.1uF
C2603	1C2	2172.0390	CAP CERAM 100V 20%	39pF
C2604	1C2	2172.0390	CAP CERAM 100V 20%	39pF
C2701	11A6	2941.0688	CAP AL-EL 35V +80/-20%	6800uF
C2702	11A5	2941.0108	CAP AL-EL 35V +80/-20%	1000uF
C2703	11E4	2454.0105	CAP POLYE 50V 5%	1uF
C2704	11F3	2454.0105	CAP POLYE 50V 5%	1uF
C3101	1E4	2172.0104	CAP CERAM 100V 20%	.1uF
C3102	1H9	2172.0471	CAP CERAM 100V 20%	470pF
C3103	2G4	2172.0104	CAP CERAM 100V 20%	.1uF
C3104	1G8	2172.0470	CAP CERAM 100V 20%	47pF
C3201	2G5	2172.0104	CAP CERAM 100V 20%	.1uF
C3202	1H4	2172.0104	CAP CERAM 100V 20%	.1uF
C3203	1C6	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	1F6	2172.0104	CAP CERAM 100V 20%	.1uF
C3302	1H6	2172.0104	CAP CERAM 100V 20%	.1uF
C3303	6A4	2172.0104	CAP CERAM 100V 20%	.1uF
C3304	1H2	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3401	6C6	2296.0271	CAP MICA 500V 1%	270pF
C3501	6G10	2172.0104	CAP CERAM 100V 20%	.1uF
C3502	6F6	2296.0271	CAP MICA 500V 1%	270pF
C3601	6G2	2172.0222	CAP CERAM 100V 20%	.0022uF
C3602	8H2	2172.0104	CAP CERAM 100V 20%	.1uF
C3603	1C1	2172.0390	CAP CERAM 100V 20%	39pF
C3604	1C1	2172.0390	CAP CERAM 100V 20%	39pF
C3605	1A2	2172.0390	CAP CERAM 100V 20%	39pF
C3606	1A2	2172.0390	CAP CERAM 100V 20%	39pF
C3607	1A1	2172.0390	CAP CERAM 100V 20%	39pF
C3608	1A1	2172.0390	CAP CERAM 100V 20%	39pF
C3609	8J2	2172.0222	CAP CERAM 100V 20%	.0022uF
C3701	11C6	2941.0108	CAP AL-EL 35V +80/-20%	1000uF
C3702	11D6	2941.0108	CAP AL-EL 35V +80/-20%	1000uF
C3703	11C4	2941.0108	CAP AL-EL 35V +80/-20%	1000uF
C3704	11B5	2941.0108	CAP AL-EL 35V +80/-20%	1000uF
C3705	11D4	2454.0105	CAP POLYE 50V 5%	1uF

REPLACEABLE ELECTRICAL PARTS LIST: 9DCI.1270

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C4101	1B5	2172.0104	CAP CERAM 100V 20%	.1uF
C4102	2A5	2172.0104	CAP CERAM 100V 20%	.1uF
C4103	2A4	2172.0104	CAP CERAM 100V 20%	.1uF
C4201	2A2	2172.0104	CAP CERAM 100V 20%	.1uF
C4202	2F7	2172.0104	CAP CERAM 100V 20%	.1uF
C4301	1H9	2172.0104	CAP CERAM 100V 20%	.1uF
C4302	1K7	2172.0222	CAP CERAM 100V 20%	.0022uF
C4303	1J8	2172.0222	CAP CERAM 100V 20%	.0022uF
C4304	1J9	2172.0222	CAP CERAM 100V 20%	.0022uF
C4305	1H2	2172.0470	CAP CERAM 100V 20%	47pF
C4306	1E4	2172.0104	CAP CERAM 100V 20%	.1uF
C4401	6D6	2555.0682	CAP POLYP 50V 2%	.0068uF
C4402	6E6	2296.0271	CAP MICA 500V 1%	270pF
C4403	6B8	2555.0823	CAP POLYP 50V 2%	.082uF
C4501	6G6	2555.0682	CAP POLYP 50V 2%	.0068uF
C4502	6G6	2296.0271	CAP MICA 500V 1%	270pF
C4503	6E8	2555.0823	CAP POLYP 50V 2%	.082uF
C4601	6E2	2172.0104	CAP CERAM 100V 20%	.1uF
C4701	11C7	2932.0476	CAP AL-EL 25V 20%	47uF
C4702	11C7	2932.0476	CAP AL-EL 25V 20%	47uF
C4703	11D7	2932.0476	CAP AL-EL 25V 20%	47uF
C4704	11D7	2932.0476	CAP AL-EL 25V 20%	47uF
C5101	11G3	2172.0104	CAP CERAM 100V 20%	.1uF
C5102	2C5	2172.0104	CAP CERAM 100V 20%	.1uF
C5103	2C4	2172.0104	CAP CERAM 100V 20%	.1uF
C5104	4H2	2172.0222	CAP CERAM 100V 20%	.0022uF
C5201	2C2	2172.0104	CAP CERAM 100V 20%	.1uF
C5202	2E9	2172.0104	CAP CERAM 100V 20%	.1uF
C5301	2C8	2172.0104	CAP CERAM 100V 20%	.1uF
C5302	8E2	2172.0104	CAP CERAM 100V 20%	.1uF
C5303	8C2	2172.0104	CAP CERAM 100V 20%	.1uF
C5401	6E6	2172.0104	CAP CERAM 100V 20%	.1uF
C5402	6C8	2172.0104	CAP CERAM 100V 20%	.1uF
C5403	7D3	2454.0334	CAP POLYE 50V 5%	.33uF
C5501	6H6	2172.0104	CAP CERAM 100V 20%	.1uF
C5502	6F8	2172.0104	CAP CERAM 100V 20%	.1uF
C5503	7G3	2454.0334	CAP POLYE 50V 5%	.33uF
C5601	8B5	2172.0104	CAP CERAM 100V 20%	.1uF
C5602	9A1	2296.0271	CAP MICA 500V 1%	270pF
C6101	4F5	2172.0104	CAP CERAM 100V 20%	.1uF
C6102	4D5	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	4G6	2172.0104	CAP CERAM 100V 20%	.1uF
C6202	5A7	2172.0471	CAP CERAM 100V 20%	470pF
C6301	8G2	2172.0222	CAP CERAM 100V 20%	.0022uF
C6302	1K2	2172.0470	CAP CERAM 100V 20%	47pF
C6303	1H2	2172.0470	CAP CERAM 100V 20%	47pF
C6304	1J3	2172.0470	CAP CERAM 100V 20%	47pF
C6401	7D4	2454.0334	CAP POLYE 50V 5%	.33uF
C6402	7C4	2296.0271	CAP MICA 500V 1%	270pF
C6403	7D4	2555.0823	CAP POLYP 50V 2%	.082uF
C6404	7D5	2296.0101	CAP MICA 500V 1%	100pF
C6405	7C6	2172.0104	CAP CERAM 100V 20%	.1uF

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C6501	7G4	2454.0334	CAP POLYE 50V 5%	.33uF
C6502	7F4	2296.0271	CAP MICA 500V 1%	270pF
C6503	7G4	2555.0823	CAP POLYP 50V 2%	.082uF
C6504	7G5	2296.0101	CAP MICA 500V 1%	100pF
C7101	4F7	2172.0104	CAP CERAM 100V 20%	.1uF
C7102	4B7	2172.0104	CAP CERAM 100V 20%	.1uF
C7202	5F5	2172.0104	CAP CERAM 100V 20%	.1uF
C7203	5D5	2172.0104	CAP CERAM 100V 20%	.1uF
C7301	5B5	2172.0104	CAP CERAM 100V 20%	.1uF
C7302	1A9	2172.0104	CAP CERAM 100V 20%	.1uF
C7402	1D5	2172.0104	CAP CERAM 100V 20%	.1uF
C7501	7D7	2172.0104	CAP CERAM 100V 20%	.1uF
C7502	1A9	2172.0104	CAP CERAM 100V 20%	.1uF
C8401	7D8	2454.0105	CAP POLYE 50V 5%	1uF
C8402	7E8	2454.0105	CAP POLYE 50V 5%	1uF
C8501	7G8	2454.0105	CAP POLYE 50V 5%	1uF
C8502	7H9	2454.0105	CAP POLYE 50V 5%	1uF
D1301	3G8	3111.4001	DIODE POWER 1A 50V	4001
D1401	3H8	3110.4152	DIODE SIGNAL	4152
D1402	3H8	3110.4152	DIODE SIGNAL	4152
D1701	11A6	3111.4001	DIODE POWER 1A 50V	4001
D2301	1H2	3110.4152	DIODE SIGNAL	4152
D2401	1H4	3110.4152	DIODE SIGNAL	4152
D2501	6G9	3110.4152	DIODE SIGNAL	4152
D2502	6G8	3110.4152	DIODE SIGNAL	4152
D2701	11B5	3111.4001	DIODE POWER 1A 50V	4001
D3101	1G9	3110.4152	DIODE SIGNAL	4152
D3701	11A5	3140.0254	BRIDGE 2A 100V	3N254
D3702	11B5	3111.4001	DIODE POWER 1A 50V	4001
D3703	11B5	3111.4001	DIODE POWER 1A 50V	4001
D3704	11B6	3110.4152	DIODE SIGNAL	4152
D3705	11D6	3110.4152	DIODE SIGNAL	4152
D4301	1K7	3110.4152	DIODE SIGNAL	4152
D4302	1J7	3110.4152	DIODE SIGNAL	4152
D4303	1J8	3110.4152	DIODE SIGNAL	4152
D4601	11C8	3131.0180	DIODE ZEN 1W 5% 18V	1N4746
D4602	11D8	3131.0180	DIODE ZEN 1W 5% 18V	1N4746
D4701	11C7	3110.4152	DIODE SIGNAL	4152
D4702	11D7	3110.4152	DIODE SIGNAL	4152
D4703	11D5	3111.4001	DIODE POWER 1A 50V	4001
D6101	5A8	3110.4152	DIODE SIGNAL	4152
D6202	5B8	3110.4152	DIODE SIGNAL	4152
D6203	5A6	3110.4152	DIODE SIGNAL	4152
D7501	7E7	3140.0254	BRIDGE 2A 100V	3N254
D8401	7E8	3110.4152	DIODE SIGNAL	4152
D8501	7H8	3110.4152	DIODE SIGNAL	4152
D9801	11A7	3610.0004	LED .125 X.22	YELLOW
E18	11A3	4540.0001	RFI	FILT, V SEL, FUSE&LINE CO
F18		4620.0020	FUSE SLO-BLO 1/4	.2A

REPLACEABLE ELECTRICAL PARTS LIST: 9DCI.1270

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
J111	3D5,3E5	4225.0009	JACK D-SUB PC 90°	9 PIN
J121	3F5,3G5	4225.0009	JACK D-SUB PC 90°	9 PIN
J131	3D9,3E9	4225.0009	JACK D-SUB PC 90°	9 PIN
J141	3F9,3G9	4225.0015	JACK D-SUB PC 90'	15 PIN
J161	1D1,1E1,1F1,1G1,1H1,			
	1I1,1J1,1K1	4225.0025	JACK D-SUB PC 90'	25 PIN
J561	8C6,8D6	4221.1008	JACK PC 2 X .1	8 PIN
J571	8E6,8F6,9G4,9G5,9G7	4221.1008	JACK PC 2 X .1	8 PIN
J581	11E4,11F4	4221.1008	JACK PC 2 X .1	8 PIN
J871	9G2,9G3	4221.1008	JACK PC 2 X .1	8 PIN
J911	4B9,4C9,4D9,4E9,4F9,4G9,4H9	4225.0025	JACK D-SUB PC 90'	25 PIN
J941	1H10,1I10,1J10,1K10	4225.0009	JACK D-SUB PC 90°	9 PIN
J961	7E9	4255.0002	JACK BANANA GNDED	KNURLED
J962	7D9	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J963	7D9	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J971	7F9	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J972	7G9	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J973	9D1	4255.0002	JACK BANANA GNDED	KNURLED
J974	9C1	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J975	9E1	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J976	9B1	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J977	9E1	4255.0001	JACK BANANA INSUL W/HDWR	BLK
J981	9A1	4255.0001	JACK BANANA INSUL W/HDWR	BLK
K741	7D8,7E8	4530.0002	RELAY PC LOW POWER	DPDT
K751	7F8,7G8,7H8	4530.0002	RELAY PC LOW POWER	DPDT
P151	1D1,1E1,1F1,1G1,1H1,			
	1I1,1J1,2J1	4225.0125	PLUG D-SUB PC 90'	25 PIN
P741	7D9	4221.0036	PLUG PC .1 X.43	36 PIN
P751	7G9	4221.0036	PLUG PC .1 X.43	36 PIN
P931	5A-H8	4225.0125	PLUG D-SUB PC 90'	25 PIN
P951	2C10,2D10	4225.0109	PLUG D-SUB PC 90'	9 PIN
Q2401	1G2	3211.2222	XSTR NPN TO92	PN2222A
Q2501	2J7	3211.2222	XSTR NPN TO92	PN2222A
Q3601	9G2	3211.2222	XSTR NPN TO92	PN2222A
Q3602	9G2	3211.2222	XSTR NPN TO92	PN2222A
Q3603	7E4	3211.5086	XSTR PNP TO92	PN5086
Q4601	7H8	3211.2222	XSTR NPN TO92	PN2222A
Q4602	7F8	3211.2222	XSTR NPN TO92	PN2222A
Q7301	10G2	3211.2222	XSTR NPN TO92	PN2222A
Q7302	10G3	3211.2222	XSTR NPN TO92	PN2222A
Q7303	10G4	3211.2222	XSTR NPN TO92	PN2222A
Q7304	9G7	3211.2222	XSTR NPN TO92	PN2222A
Q7305	9G3	3211.2222	XSTR NPN TO92	PN2222A
Q7306	9G4	3211.2222	XSTR NPN TO92	PN2222A
Q7307	9G5	3211.2222	XSTR NPN TO92	PN2222A
R211	3D4,3E4	1994.8391	RES NET DIP 5%	8 X 390
R2203	1E5	1214.0102	RES 1/4W C FLM 5%	1K
R221	3F4,3G4	1994.8391	RES NET DIP 5%	8 X 390
R222	3D8,3E8	1994.8391	RES NET DIP 5%	8 X 390
R2301	1H2	1214.0473	RES 1/4W C FLM 5%	47K
R231	3F8,3G8	1994.8391	RES NET DIP 5%	8 X 390

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R2401	1H1	1214.0102	RES 1/4W C FLM 5%	1K
R2402	1H2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2403	1G2	1214.0103	RES 1/4W C FLM 5%	10K
R2404	2J7	1214.0472	RES 1/4W C FLM 5%	4.7K
R2501	2K7	1214.0472	RES 1/4W C FLM 5%	4.7K
R2502	1G2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2503	1K2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2504	1H2	1214.0272	RES 1/4W C FLM 5%	2.7K
R261	1A1,1B1,1C1	1994.8392	RES NET DIP 5%	8 X 3.9K
R2701	11F4	1214.0270	RES 1/4W C FLM 5%	27
R3101	2H4	1214.0105	RES 1/4W C FLM 5%	1M
R3102	2H4	1214.0100	RES 1/4W C FLM 5%	10
R3103	1H7	1214.0102	RES 1/4W C FLM 5%	1K
R3104	1G9	1214.0103	RES 1/4W C FLM 5%	10K
R3201	1H7	1214.0472	RES 1/4W C FLM 5%	4.7K
R3401	6D4	1214.0203	RES 1/4W C FLM 5%	20K
R3402	6E5	1139.1284	RES 1/8W M FLM .1%	1.28M
R3403	6D5	1139.1284	RES 1/8W M FLM .1%	1.28M
R341	6C5,6D5,6C8,6D6,6E7,6G8	1999.1002	RES NET DIP .1%	8 X 10K
R3501	6G4	1214.0203	RES 1/4W C FLM 5%	20K
R3502	6G5	1139.1284	RES 1/8W M FLM .1%	1.28M
R3503	6G5	1139.1284	RES 1/8W M FLM .1%	1.28M
R3504	6F9	1214.0472	RES 1/4W C FLM 5%	4.7K
R351	6E5,6F5,6F6,6G7,6E8	1999.1002	RES NET DIP .1%	8 X 10K
R361	7F7,7H7,9G1,9G2	1994.8392	RES NET DIP 5%	8 X 3.9K
R3701	11C6	1136.3831	RES 1/8W M FLM 1%	3.83K
R3702	11D6	1136.3831	RES 1/8W M FLM 1%	3.83K
R3703	11C7	1139.3330	RES 1/8W M FLM .1%	333.3
R3704	11D7	1139.3330	RES 1/8W M FLM .1%	333.3
R3705	11F2	1214.0270	RES 1/4W C FLM 5%	27
R421	2F7,2F6,2G6,2G7,2G8	1984.9103	RES NET SIP 5% B	9 X 10K
R4301	1J7	1214.0105	RES 1/4W C FLM 5%	1M
R4302	1J7	1214.0105	RES 1/4W C FLM 5%	1M
R4303	1J8	1214.0105	RES 1/4W C FLM 5%	1M
R4304	1J10	1214.0391	RES 1/4W C FLM 5%	390
R4401	6D7	1136.1004	RES 1/8W M FLM 1%	1.00M
R4402	6G8	1136.1003	RES 1/8W M FLM 1%	100K
R4403	6E6	1214.0272	RES 1/4W C FLM 5%	2.7K
R4404	6B8	1136.5490	RES 1/8W M FLM 1%	549
R4405	6G7	1136.1004	RES 1/8W M FLM 1%	1.00M
R4501	6E8	1136.5490	RES 1/8W M FLM 1%	549
R4502	6H6	1214.0272	RES 1/4W C FLM 5%	2.7K
R4601	8E4	1214.0391	RES 1/4W C FLM 5%	390
R4701	11D4	1214.0270	RES 1/4W C FLM 5%	27
R5201	2J8	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R5402	6C8	1214.0272	RES 1/4W C FLM 5%	2.7K
R5403	6D7	4412.0503	POT TRIM PC ENC	50K
R5404	6B8	4413.0103	POT TRIM PC 10 TURN	10K
R5405	6B8	1136.8253	RES 1/8W M FLM 1%	825K
R5406	7C3	1214.0226	RES 1/4W C FLM 5%	22M
R5502	6F8	1214.0272	RES 1/4W C FLM 5%	2.7K
R5503	6F7	4412.0503	POT TRIM PC ENC	50K

REPLACEABLE ELECTRICAL PARTS LIST: 9DCI.1270

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R5504	6E8	4413.0103	POT TRIM PC 10 TURN	10K
R5505	6E8	1136.8253	RES 1/8W M FLM 1%	825K
R5506	7F3	1214.0226	RES 1/4W C FLM 5%	22M
R5601	8B5	1214.0391	RES 1/4W C FLM 5%	390
R5602	9A1	1214.0226	RES 1/4W C FLM 5%	22M
R5701	8C5	1214.0102	RES 1/4W C FLM 5%	1K
R5702	8D4	1214.0105	RES 1/4W C FLM 5%	1M
R6102	5A7	1214.0103	RES 1/4W C FLM 5%	10K
R6103	8B4	1214.0102	RES 1/4W C FLM 5%	1K
R6201	5A6	1214.0103	RES 1/4W C FLM 5%	10K
R6302	8C4	1214.0103	RES 1/4W C FLM 5%	10K
R6303	8F3	1214.0103	RES 1/4W C FLM 5%	10K
R631	2C8	1994.8473	RES NET DIP 5%	8 X 47K
R632	9G3,9G4,9G6,10G2	1994.8392	RES NET DIP 5%	8 X 3.9K
R6401	7D3	1136.1002	RES 1/8W M FLM 1%	10.0K
R6402	7D4	1139.4002	RES 1/8W M FLM .1%	40.0K
R6403	7D4	1136.8661	RES 1/8W M FLM 1%	8.66K
R6404	7D6	1214.0103	RES 1/4W C FLM 5%	10K
R6405	7D5	1214.0203	RES 1/4W C FLM 5%	20K
R6406	7D6	1214.0104	RES 1/4W/C/FLM 5%	100K
R6501	7F3	1136.1002	RES 1/8W M FLM 1%	10.0K
R6502	7F3	1139.4002	RES 1/8W M FLM .1%	40.0K
R6503	7F4	1136.8661	RES 1/8W M FLM 1%	8.66K
R6504	7F6	1214.0103	RES 1/4W C FLM 5%	10K
R6505	7G5	1214.0203	RES 1/4W C FLM 5%	20K
R6506	7G6	1214.0104	RES 1/4W/C/FLM 5%	100K
R741	7D5,7D6,7C5,7C6,7G5,7F5,7F6	1999.1002	RES NET DIP .1%	8 X 10K
R811	4F8,4G8	1994.8391	RES NET DIP 5%	8 X 390
R812	4B8,4C8	1994.8391	RES NET DIP 5%	8 X 390
R813	4D8,4E8	1994.8391	RES NET DIP 5%	8 X 390
R821	5G6,5H6	1994.8473	RES NET DIP 5%	8 X 47K
R822	5H7	1984.9104	RES NET SIP 5%	B 9 X 100K
R823	5E6,5F6	1994.8473	RES NET DIP 5%	8 X 47K
R831	5F7	1984.9104	RES NET SIP 5%	B 9 X 100K
R832	5C6,5D6	1994.8473	RES NET DIP 5%	8 X 47K
R833	5D6,5D7	1984.9104	RES NET SIP 5%	B 9 X 100K
R834	1H10,1J10,1K10	1994.8391	RES NET DIP 5%	8 X 390
R835	2C8,2C9	1984.9104	RES NET SIP 5%	B 9 X 100K
R8401	7C5	1136.1004	RES 1/8W M FLM 1%	1.00M
R8402	7C5	4412.0503	POT TRIM PC ENC	50K
R8403	7D7	1065.0060	RES PTC CERAM 150V	60mA
R8404	7D7	1065.0060	RES PTC CERAM 150V	60mA
R8501	7F6	1136.1004	RES 1/8W M FLM 1%	1.00M
R8502	7F6	4412.0503	POT TRIM PC ENC	50K
R8503	7G7	1065.0060	RES PTC CERAM 150V	60mA
R8504	7G7	1065.0060	RES PTC CERAM 150V	60mA
R9701	9C1	1656.6000	RES 3W W WND 1%	600
R9702	9E1	1656.6000	RES 3W W WND 1%	600
R9801	11A7	1214.0391	RES 1/4W C FLM 5%	390
R9802	9A1	1214.0102	RES 1/4W C FLM 5%	1K
S381	11B2	4321.0002	SWITCH PUSH POWER	DPDT

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U171	3D3	3430.2940.5	VOLT REG POS 5.0V TO220	LM2940
U211	3D4	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U212	3G4	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U221	3C7	3324.0574	FLIP-FLO 8X D TRI-ST	74HCT574
U231	3G7	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U232	6A2	3323.4040	COUNTER 12-STAGE	74HC4040
U261	6C2	3332.8254	TIMER INTERVAL PROG	82C54
U262	1D2	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U263	1B2	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U311	1F4	3324.0138	DECODER 3LINE/8LINE	74HCT138
U313	1G9,2H4	3323.0132	GATE 4X2-IN NAND SCHMT	74HC132
U321	2G5,2H5,2H6,6A5	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U322	1J4	3313.0174	FLIP-FLOP 6X D W/CLR	74HCT174
U323	1D6	3313.0155	DECODER 2 X 2-LN/4-LN	74HCT155
U331	1G6	3324.0138	DECODER 3LINE/8LINE	74HCT138
U332	1J6	3324.0138	DECODER 3LINE/8LINE	74HCT138
U333	6A4	3323.0157	MULTIPLEXER 4 X 2CH	74HC157
U341	6C4,6D4	3323.0175	FLIP-FLOP 6X D	74HC175
U342	6D4	3323.0175	FLIP-FLOP 6X D	74HC175
U351	6E4,6F4	3323.0175	FLIP-FLOP 6X D	74HC175
U352	6G10	3442.0584	PRECISION VOLTAGE REF	AD584
U361	6F2	3332.8254	TIMER INTERVAL PROG	82C54
U362	8H2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U411	1B5	3324.0139	DECODER 2 X 2-LN/4-LN	74HCT139
U412	2B5	3313.0670	REGISTER FILE 4X4	74HCT670
U413	2B4	3313.0670	REGISTER FILE 4X4	74HCT670
U421	2B2	3313.0670	REGISTER FILE 4X4	74HCT670
U422	2F7	3331.6805	uPROCESSOR EPROM	68705P3
U431	1H9,1J7,1J8,1J9	3323.0132	GATE 4X2-IN NAND SCHMT	74HC132
U432	1D3,1E4,1H2,6B2	3323.0002	GATE 4X2-IN NAND	74HC02
U441	6E6	3411.0027	OP AMP SINGLE	OP27
U442	6C8	3411.0027	OP AMP SINGLE	OP27
U451	6G6	3411.0027	OP AMP SINGLE	OP27
U452	6E8	3411.0027	OP AMP SINGLE	OP27
U471	11B6	3430.1317	VOLT REG POS VAR TO92	LM317L
U472	11D6	3431.1337	VOLT REG NEG VAR TO92	LM337L
U511	4G3	3323.0175	FLIP-FLOP 6X D	74HC175
U512	2D5	3313.0670	REGISTER FILE 4X4	74HCT670
U513	2D4	3313.0670	REGISTER FILE 4X4	74HCT670
U521	2D2	3313.0670	REGISTER FILE 4X4	74HCT670
U531	2D7	3324.0245	TRANSCVR 8X TRI-ST	74HCT245
U532	8F2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U533	1G3,1J3,1K2,1D5	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U561	8C5	3630.2601	OPTOCOUPLER GATE	HCPL2601
U571	8D4	3630.0001	OPTO-ISOLATOR	H11AA1
U611	4F5	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U612	4E5	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U613	2G10,8F4	3324.0074	FLIP-FLOP 2X D	74HCT74
U621	4H6,5A6,5A7	3323.0132	GATE 4X2-IN NAND SCHMT	74HC132
U622	2F9	3332.8254	TIMER INTERVAL PROG	82C54
U711	4G6	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574

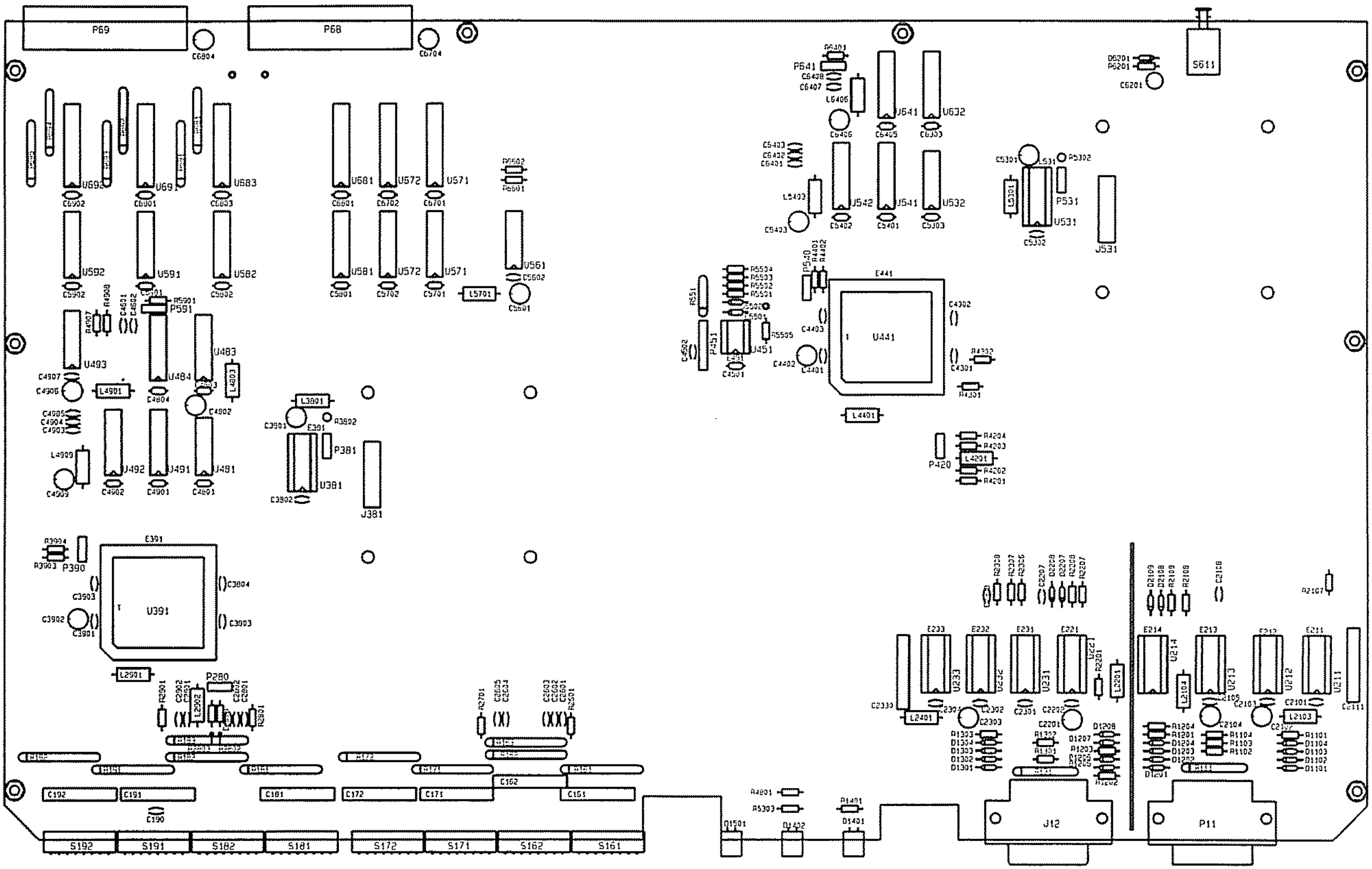
REPLACEABLE ELECTRICAL PARTS LIST: 9DCI.1270

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
U712	4C6	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U713	4E6	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U721	1B4	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U722	5G5	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U723	5E5	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U731	5C5	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U732	1B9	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U741	7D5	3411.1012	OP AMP SINGLE	LT1012
U742	7D4	3411.1012	OP AMP SINGLE	LT1012
U751	7F5	3411.1012	OP AMP SINGLE	LT1012
U752	7G4	3411.1012	OP AMP SINGLE	LT1012
U753	7D6,7G6	3412.5532	OP AMP DUAL	5532
W2801		4121.0002.0	WIRE 22Ga C&S UL1015 2.5"	BLK
W2802		4121.0002.9	WIRE 22Ga C&S UL1015 2.5"	WHT
W2803		4121.0002.0	WIRE 22Ga C&S UL1015 2.5"	BLK
W2804		4121.0002.9	WIRE 22Ga C&S UL1015 2.5"	WHT
W2805		4121.0002.0	WIRE 22Ga C&S UL1015 2.5"	BLK
W2806		4121.0002.9	WIRE 22Ga C&S UL1015 2.5"	WHT
W2807		4121.0002.0	WIRE 22Ga C&S UL1015 2.5"	BLK
W2808		4121.0002.9	WIRE 22Ga C&S UL1015 2.5"	WHT
W491		4122.0001	WIRE 18Ga C&S	3
W971		4151.6002	CABLE ASSY .1 RBN 6	2 COND
W972		4151.6002	CABLE ASSY .1 RBN 6	2 COND
W973		4121.0002.0	WIRE 22Ga C&S UL1015 2.5"	BLK
W974		4121.0002.9	WIRE 22Ga C&S UL1015 2.5"	WHT
W975		4121.0002.0	WIRE 22Ga C&S UL1015 2.5"	BLK
W976		4121.0002.9	WIRE 22Ga C&S UL1015 2.5"	WHT
X171	11E4	4524.0001	TRANSFORMER LO POWER	DCX
X381	11A4	4523.0002	TRANSFORMER POWER	DCX/SWR
Y311	2H4	3900.0020	CRYSTAL	20MHz

→

SIA-322

SERIAL INTERFACE ADAPTER



SIA-322 SERIAL INTERFACE ADAPTER 9SIA.1000 (6200.SIA1.5)

SIA-322, SERIAL INTERFACE ADAPTER

Introduction

The SIA-322 Serial Interface Adapter provides a means of interfacing an Audio Precision System One Dual Domain (SYS-322 or SYS-302 configuration) to a variety of different data acquisition, reconstruction, and communication hardware that utilize a serial bus for the exchange of data. The SIA-322 consists of a parallel-to-serial transmitter and a serial-to-parallel receiver, each completely independent of the other. Since few serial communication standards exist, flexibility and ease of use were of primary concern in the design of the SIA-322. Some of the features provided are:

Serial frame length adjustable from 8 to 32 bits.

Single or time multiplexed dual channel operation.

Data word length adjustable from 8 to 24 bits.

Optional 0/1 padding, LSB-extension, MSB-extension.

Independent selection of LSB-first or MSB-first formats for data transmission and reception.

Programmable word clock transition timing within the data frame.

Programmable bit-wide or word-wide clock widths.

Operation from internal or external bit clock reference.

Operation from internal or external word clock reference.

All inputs and outputs support TTL or CMOS logic levels.

Logic polarity control of data, word clock, and bit clock.

SIA-322 Interface to System One

The SIA-322 exchanges data with and derives its power from the System One Dual Domain parallel ports located on the rear panel of the System One. The parallel output port provides 24-bit data output and accepts word strobe and channel select signals. The parallel input port accepts 24-bit data, word strobe and channel select signals. Two 34-conductor ribbon cables are used to connect the SIA-322 to a System One. The 34-pin connector pin-outs can be found in the System One DSP Users Manual.

Transmitter Interface to the Target System

The transmitter interfaces to the target system through a 15-pin male D-subminiature connector. Three primary signals are available on the I/O port: serial data output, word (channel) clock I/O, and bit clock I/O. Additionally, three tri-state control pins are provided, allowing the user to individually control the three primary signals in shared-bus configurations. A reference clock input and N x FS clock output are also provided. The word clock and bit clock signals are bi-directional. In input mode, these signals can be driven by TTL or CMOS sources. All output drivers are capable of driving TTL or CMOS loads. The pin assignments for the transmitter DB-15 connector are shown in TABLE SIA322.1.

TABLE SIA322.1
TRANSMITTER SERIAL CONNECTOR PIN ASSIGNMENT

Pin Number	Pin Name	Description
1	SOD	Serial Data Output
3	SOWCLK	Word Clock I/O
5	SOBCLK	Bit Clock I/O
7	SODE	SOD Enable (H)
9	SOWCLKE	SOWCLK Enable (H)
11	SOBCLKE	SOBCLK Enable (H)
13	TREFCLK	Tx Clock Ref Input
15	TNFSCLK	N x FS Clock Output
2/4/6/8/10/12/14	GND	Ground

The SODE, SOWCLKE and SOBCLKE inputs are internally tied to +5V through 100 kOhm resistors. Pulling these inputs low will disable their associated outputs.

Transmitter Configuration Switches

A set of DIP switches is used to configure the SIA-322 transmitter for the various modes of operation. The switch settings for the transmitter are as follows:

Switch Name	Description
TWL4 to TWL0	*Transmitter Word Length.* Length of transmitted serial word, minus 1. Can be set from 7 to 31, corresponding to word lengths of 8 to 32 bits.
TDL4 to TDL0	*Transmitter Data Length.* Number of significant bits of System One data word to be transmitted, minus 1. Can be set from 7 to 23, corresponding to data lengths of 8 to 24 bits.
TWCPOS4 to TWCPOS0	*Transmitter Word Clock Position.* Physical position of word clock transition within the serial frame. Can be set from 0 to 31.
TWCWID	*Transmitter Word Clock Width.* OFF = bit-wide, ON = word wide (symmetric) clock.
TFC0	*Transmitter Framing Control 0.* OFF = right, ON = left-justified data within serial frame.
TFC1	*Transmitter Framing Control 1.* OFF = zero/one pad out-of-bounds data, ON = sign extend out-of-bounds data.
TFC2	*Transmitter Framing Control 2.* Sets pad value for out-of-bounds data if TFC1 = OFF: OFF = zero, ON = one.
T2CHAN	*Transmitter Channel Select.* OFF = single channel operation, ON = two channel operation.
TLSBF	*Transmitter First-Bit Select.* Selects LSB or MSB as first valid bit within the serial frame. OFF = MSB first, ON = LSB first.
TXWCLK	*Transmitter Word Clock Source Select.* OFF = internally generated word clock, ON = external word clock.
TXBCLK	*Transmitter Bit Clock Source Select.* OFF = internally generated bit clock, ON = external bit clock.
TDPOL	*Transmitter Data Polarity Select.* OFF = data is asserted high ON = data is inverted (asserted low).
TWPOL	*Transmitter Word Clock Polarity Select.* OFF = clock is asserted high, ON = clock is inverted (asserted low).
TCPOL	*Transmitter Bit Clock Polarity Select.* OFF = clock is asserted high, ON = clock is inverted (asserted low).
TCMOS	*Transmitter CMOS Input Select.* OFF = inputs configured for TTL levels, ON = inputs configured for CMOS.
TDIV22 to TDIV20	*Transmitter Second Divider Control.* Sets divide ratio of second reference clock divider to 1/(TDIV2 + 1).
TDIV11 & TDIV10	*Transmitter First Divider Control.* Sets divide ratio of first reference clock divider (see text).

Receiver Interface to the Target System

The receiver interfaces to the target system through a 15-pin female D-subminiature connector. Three primary signals are available on the I/O port: serial data input, word (channel) clock I/O, and bit clock I/O. Additionally, two tri-state control pins are provided, allowing the user to individually control the word and bit clocks in shared-bus configurations. A reference clock input and N X FS clock output are also provided. The word clock and bit clock signals are bi-directional. In input mode, these signals can be driven by TTL or CMOS sources. All output drivers are capable of driving TTL or CMOS loads. The pin assignments for the receiver connector are shown in TABLE SIA322.2.

TABLE SIA322.2
RECEIVER SERIAL CONNECTOR PIN ASSIGNMENT

Pin Number	Pin Name	Signal Description
1	SID	Serial Data Input
3	SIWCLK	Word Clock I/O
5	SIBCLK	Bit Clock I/O
7	---------	No Connection
9	SIWCLKE	SIWCLK Enable (H)
11	SIBCLKE	SIBCLK Enable (H)
13	RREFCLK	Rx Clock Ref Input
15	RNFSCLK	N X FS Clock Output
2/4/6/8/10/12/14	GND	Ground

The SIWCLKE and SIBCLKE inputs are internally tied to +5V through 100 kOhm resistors. Pulling these inputs low will disable their associated outputs.

Receiver Configuration Switches

A set of DIP switches is used to configure the SIA receiver for the various modes of operation. The switch settings for the receiver are as follows:

Switch Name	Description
RWL4 to RWL0	*Receiver Word Length.* Length of received serial word, minus 1. Can be set from 7 to 31 corresponding to word lengths of 8 to 32 bits.
RDL4 to RDL0	*Receiver Data Length.* Number of significant bits from received serial word to be transmitted to System One, minus 1. Can be set from 7 to 23 corresponding to data lengths of 8 to 24 bits.
RWCPOS4 to RWCPOS0	*Receiver Word Clock Position.* Physical position of word clock transition within the serial frame. Can be set from 0 to 31.
RWCWID	*Receiver Word Clock Width.* Width of receiver word clock pulse. OFF = bit-wide clock pulse, ON = word wide (symmetric) clock.
RFC0	*Receiver Framing Control 0.* OFF = right, ON = left-justified data within the serial frame.
R2CHAN	*Receiver Channel Select.* OFF = single channel operation, ON = two channel operation.
RLSBF	*Receiver First-Bit Select.* Selects LSB or MSB as first valid bit within the serial frame. OFF = MSB first, ON = LSB first.
RXWCLK	*Receiver Word Clock Source Select.* Selects source of word clock. OFF = internally generated word clock, ON = external word clock.
RXBCLK	*Receiver Bit Clock Source Select.* Selects source of bit clock. OFF = internally generated bit clock, ON = external bit clock.
RDPOL	*Receiver Data Polarity Select.* OFF = data is asserted high, ON = data is inverted (asserted low).
RWPOL	*Receiver Word Clock Polarity Select.* OFF = clock is asserted high, ON = clock is inverted (asserted low).
RCPOL	*Receiver Bit Clock Polarity Select.* OFF = clock is asserted high, ON = clock is inverted (asserted low).
RCMOS	*Receiver CMOS Input Select.* OFF = inputs configured for TTL logic, ON = inputs configured for CMOS.
RDIV22 to RDIV20	*Receiver Second Divider Control.* Sets divide ratio of second reference clock divider to 1/(RDIV2+1).
RDIV11 to RDIV10	*Receiver First Divider Control.* Sets divide ratio of first reference clock divider (see text).

Transmitter Theory of Operation

The majority of the transmitter control logic is encapsulated in a Xilinx XC2018 programmable gate array (PGA), with other functions implemented in peripheral HCT and ACT-series logic. These functions are the System One parallel port interface and serial output interface. Due to limitations in available power from the System One parallel port interface, CMOS devices are used exclusively in the design.

The XC2018 PGA controller (U441) provides all of the system control and sequencing for the transmitter. Four banks of DIP switches are used for configuring the transmitter for the various modes of operation. All configuration signals, with the exception of TDIV1 and TDIV2, are wired as asserted-low logic.

Parallel data from the System One is latched in U671, U672 and U681, and applied to a 24:1 multiplexer consisting of U571, U572 and U581. The register latch and multiplexer select lines are controlled by the XC2018. The word clock, data strobe and channel select lines from the parallel interface are buffered via Schmitt trigger inverters (U561) and connected to pins on the XC2018.

Transmitter Bit Clock Generation

The SIA-322 is capable of generating word, bit, and N X FS clocks from an externally supplied reference (TREFCLK); or it can be slaved to externally generated bit and word clocks. Two programmable dividers are used to divide TREFCLK down to an appropriate rate for the target system.

The first divider, consisting of U632 and U641, divides TREFCLK by 1/2/4/8 or 4/8/16/32, depending on the setting of the 3-pin jumper plug P641 (P641 is located on the SIA circuit board near U641). In its default configuration, P641 enables 1/2/4/8 division rates. The user may optionally set P641 to enable 4/8/16/32 division rates (see the SIA-322 Users Manual for additional information on jumper configuration). The 4 possible division rates for a given P641 setting are selected via the TDIV1 front panel configuration switches. The output of the first divider is connected to P11-15 (TNFSCLK) via a 74HC126 buffer (U213), as well as the input of the second divider.

The second divider, consisting of U541 and U542, further divides TREFCLK by a ratio of 1 to 8. The division rate is selected via the TDIV2 front panel configuration switches. Shift register U541's output register is clocked by the output of the first divider, while its internal shift register chain is clocked by an inverted version of the first divider's output. The shift register input is tied high, so its outputs will go high, one after another following a clear operation. Selector U542 routes one of the shift register outputs to the transmitter circuitry and an inverted version of the same output to the shift register /SRCLR (clear) input. When the selected output goes high the clear input is driven low, resetting the shift register outputs low. The resulting waveform is a high pulse separated by a selectable number of low intervals.

The output of the second divider is routed to the transmitter XC2018 and used as the master bit clock when TXBCLK is off (as selected by the user). This bit clock is optionally inverted via an XOR gate (within the XC2018) and routed to P11-5 (SOBCLK) via a 74HCT125 buffer (U212).

The XC2018 generates the word clock output (SOWCLK, P11-3) by dividing the bit clock received from the second divider by the equation T2CHAN*(TWL+1); that is, in two-channel mode, the XC2018 word clock divider can be set from 16 to 64, and in one-channel mode it can be set from 8 to 32. The word clock output is optionally inverted and routed to P11-3 via a 74HCT125 buffer (U212).

The word and bit clocks may optionally be generated by external hardware and applied to P11-3 and P11-5 when the SIA is configured for slave mode operation (TXBCLK, TXWCLK = ON).

Serial Output Buffers and Tri-State Control

A simple buffer stage provides isolation between the target system and the SIA-322, a means of tri-stating all serial interface outputs and support for TTL or CMOS logic levels on inputs. Tri-state buffers (74HC126/HCT125) are used on all inputs and outputs, and output tri-state control is provided from the OR-ing of the appropriate serial enable pins on the serial interface with TXBCLK and TXWCLK configuration switches. Input logic family selection is a function of the TCMOS, TXBCLK, and TXWCLK configuration settings, and is controlled by the XC2018.

The enable pins on the serial interface are tied high through 100k Ohm resistors. During normal operation these pins can be left unconnected. To disable the outputs, the appropriate enable pins must be pulled to the low TTL state.

The transmitter I/O lines have 22 Ohm series resistors and 1N4152 clamping diodes between the logic lines and VCC/GND to reduce ringing. All outputs are capable of sourcing or sinking at least one TTL logic load, and will provide voltage levels capable of driving either TTL or CMOS loads.

Transmitter PGA Controller

The transmitter controller implements the logic necessary for parallel-to-serial data conversion, System One parallel interface hand shaking and word clock locking. The PGA controller performs the following tasks:

1) Parallel data read from the System One parallel port must be converted to serial form in one of several user-specified formats (e.g. LSB-first, right justified, etc.). Bit truncation, insertion, or sign extension may optionally be performed.

2) An internal word clock must be generated with transitions at the appropriate time within the serial data frame. If the internal word clock is disabled, the system must be able to lock to an externally supplied clock and provide output data at the appropriate time.

3) The appropriate word and bit clock sources (either internal or external) must be selected and routed to the appropriate logic within the PGA and externally.

4) Tri-state buffer controls for the serial I/O buffering logic must be generated based upon the current transmitter configuration.

Receiver Theory of Operation

The majority of the receiver control logic is encapsulated in a Xilinx XC2018 programmable gate array (PGA), with other functions implemented in peripheral HCT and ACT-family logic. These functions are the System One parallel port interface and serial input interface. Due to limitations in available power from the System One parallel port interface, CMOS devices are used exclusively in the design.

The XC2018 PGA controller (U391) provides all of the system control and sequencing for the receiver. Four banks of DIP switches are used for configuring the receiver for the various modes of operation. All configuration signals, with the exception of RDIV1 and RDIV2, are wired as asserted-low logic.

Data read from the serial port is routed through the receiver PGA and applied to a 1:24 demultiplexer consisting of addressable latches U592, U591 and U582. When a complete word has been assembled in the addressable latch it is stored in three 8 bit latches U692, U691, and U683. This holds the data stable while the next word is constructed one bit at a time. The parallel output data lines have 22 Ohm series resistors to reduce the rise and fall times of the bus, thereby reducing noise generation. The register latch line and the addressable latch lines are controlled by the receiver PGA U291. The word clock, data strobe and channel select lines to the parallel interface are buffered via Schmitt Trigger inverters (U493) and routed directly to the receiver XC2018.

Receiver Bit Clock Generation

The SIA-322 is capable of generating word, bit, and N X FS clocks from an externally supplied reference (RREFCLK); or can be slaved to externally generated bit and word clocks. Two programmable dividers are used to divide RREFCLK down to an appropriate rate for the target system.

The first divider, consisting of U483 and U484, divides RREFCLK by 1/2/4/8 or 4/8/16/32, depending on the setting of the 3-pin jumper plug P591 (P591 is located on the SIA circuit board near U484). In its default configuration, P591 enables 1/2/4/8 division rates. The user may optionally set P591 to enable 4/8/16/32 division rates (see the SIA-322 Users Manual for additional information on jumper configuration). The 4 possible division rates for a given P591 setting are selected via the RDIV1 front panel configuration switches. The output of the first divider is connected to J12-15 (RNFSCLK) via a 74HC126 buffer (U232), as well as the input of the second divider.

The second divider, consisting of U491 and U492, further divides RREFCLK by a ratio of 1 to 8. The division rate is selected via the RDIV2 front panel configuration switches. Shift register U491's output register is clocked by the output of the first divider, while its internal shift register chain is clocked by an inverted version of the first divider's output. The shift register input is tied high, so its outputs will go high, one after another following a clear operation. Selector U492 routes one of the shift register outputs to the receiver circuitry and an inverted version of the same output to the shift register /SRCLR (clear) input. When the selected output goes high the clear input is driven low, resetting the shift register outputs low. The resulting waveform is a high pulse separated by a selectable number of low intervals.

The output of the second divider is routed to the receiver XC2018 and used as the master bit clock when RXBCLK is off (as selected by the user). This bit clock is optionally inverted via an XOR gate (within the XC2018) and routed to J12-5 (SIBCLK) via a 74HCT125 buffer (U231).

The XC2018 generates the word clock output (SIWCLK, J12-3) by dividing the bit clock received from the second divider by the equation R2CHAN*(RWL+1); that is, in two-channel mode, the XC2018 word clock divider can be set from 16 to 64, and in one-channel mode it can be set from 8 to 32. The word clock output is optionally inverted and routed to J12-3 via a 74HCT125 buffer (U231).

The word and bit clocks may optionally be generated by external hardware and applied to J12-3 and J12-5 when the SIA is configured for slave mode operation (RXBCLK, RXWCLK = ON).

Serial Input Buffers and Tri-State Control

A simple buffer stage provides isolation between the target system and the SIA-322, a means of tri-stating the serial interface outputs and support for TTL or CMOS logic levels on inputs. Tri-state buffers (74HC126/HCT125) are used on all inputs and outputs, and output tri-state control is provided from the OR-ing of the appropriate serial enable pins on the serial interface with RXBCLK and RXWCLK configuration switches. Input logic family selection is a function of the RCMOS, RXBCLK, and RXWCLK configuration settings, and is controlled by the PGA (U391).

The enable pins on the serial interface are tied high through 100 kOhm resistors. During normal operation these pins can be left unconnected. To disable the outputs, the appropriate enable pins must be pulled to the low TTL state.

The receiver I/O lines have 22 Ohm series resistors and 1N4152 clamping diodes between the logic lines and VCC/GND to reduce ringing and protect against overvoltage. All outputs are capable of sourcing or sinking at least one TTL logic load, and will provide voltage levels capable of driving either TTL or CMOS loads.

Receiver PGA Controller

The receiver controller implements the logic necessary for serial-to-parallel data conversion, System One parallel interface hand shaking and word clock locking. Some sections of the receiver are very similar to their corresponding sections in the transmitter. The PGA controller performs the following tasks:

1) Serial data received from the serial input channel must be reassembled into a parallel word for transmission to the System One. The data may arrive in any one of the many user-specified formats (e.g. LSB-first, right justified, etc.).

2) An internal word clock must be generated with transitions at the appropriate time within the expected serial input data frame. If the internal word clock is disabled, the system must be able to lock to an externally supplied clock and latch input data at the appropriate time.

3) The appropriate word and bit clock sources (either internal or external) must be selected and routed to the appropriate logic within the PGA and externally.

4) Tri-state buffer controls for the serial I/O buffering logic must be generated based upon the current receiver configuration.

System Clocking Configuration

The majority of the PGA controller design is synchronous. The source for driving the PGA internal clock is selected from two potential sources: the master reference (TREFCLK, RREFCLK), and the external bit clock input. The source of the bit clock is selected by the state of TXBCLK or RXBCLK, as appropriate. The external bit clock may optionally be inverted depending upon the state of TCPOL or RCPOL. The selected bit clock is also optionally inverted and then routed outside the XC2018 to drive the bit clock output line on the serial interface (SOBCLK, SIBCLK).

The transmitter and receiver clock source is dependent upon the state of TXBCLK and TXWCLK or RXBCLK and RXWCLK. The four possible system clocking modes are listed in TABLE SIA322.3.

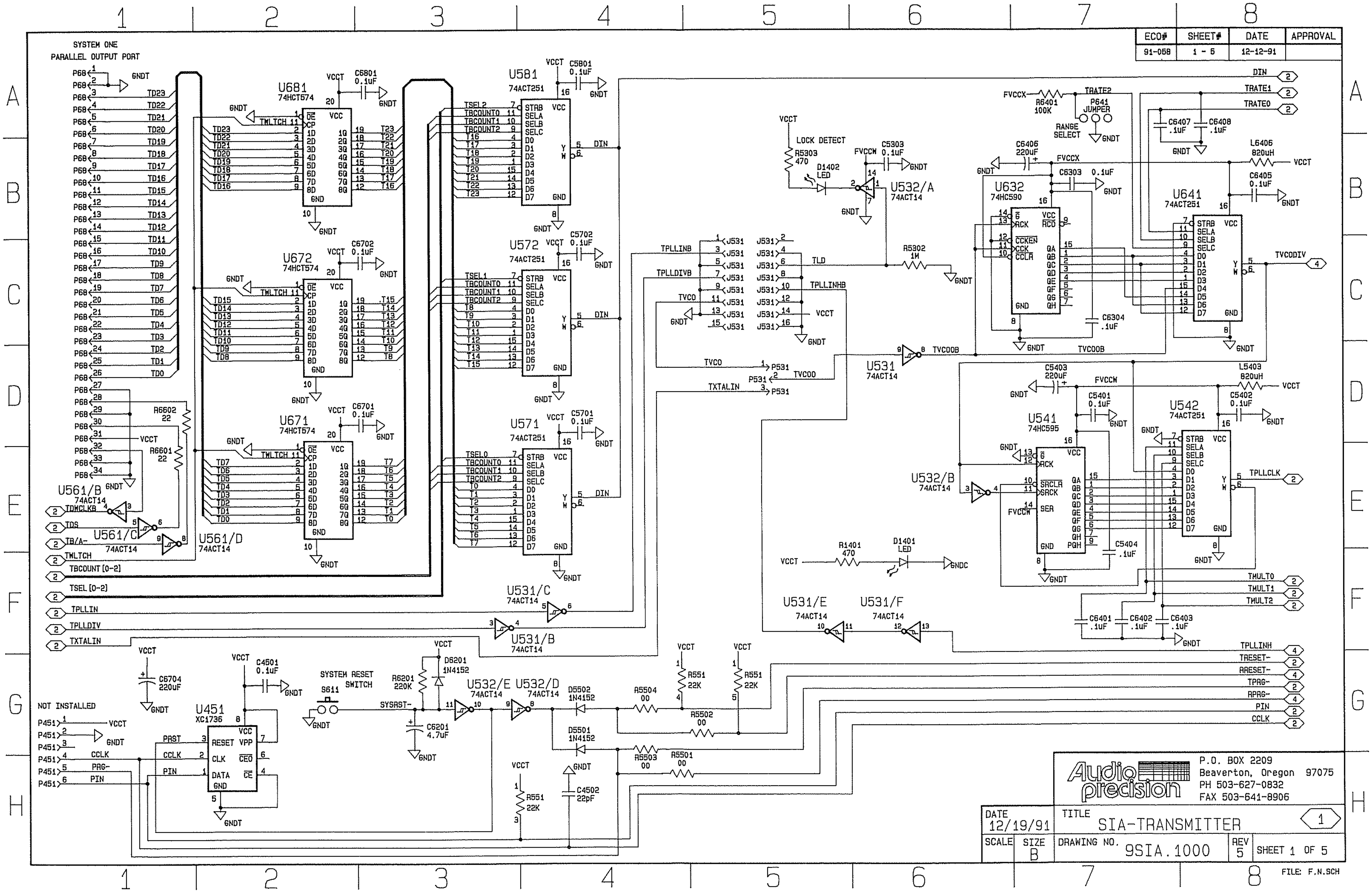
TABLE SIA322.3
Transmitter/Receiver Clock Configuration

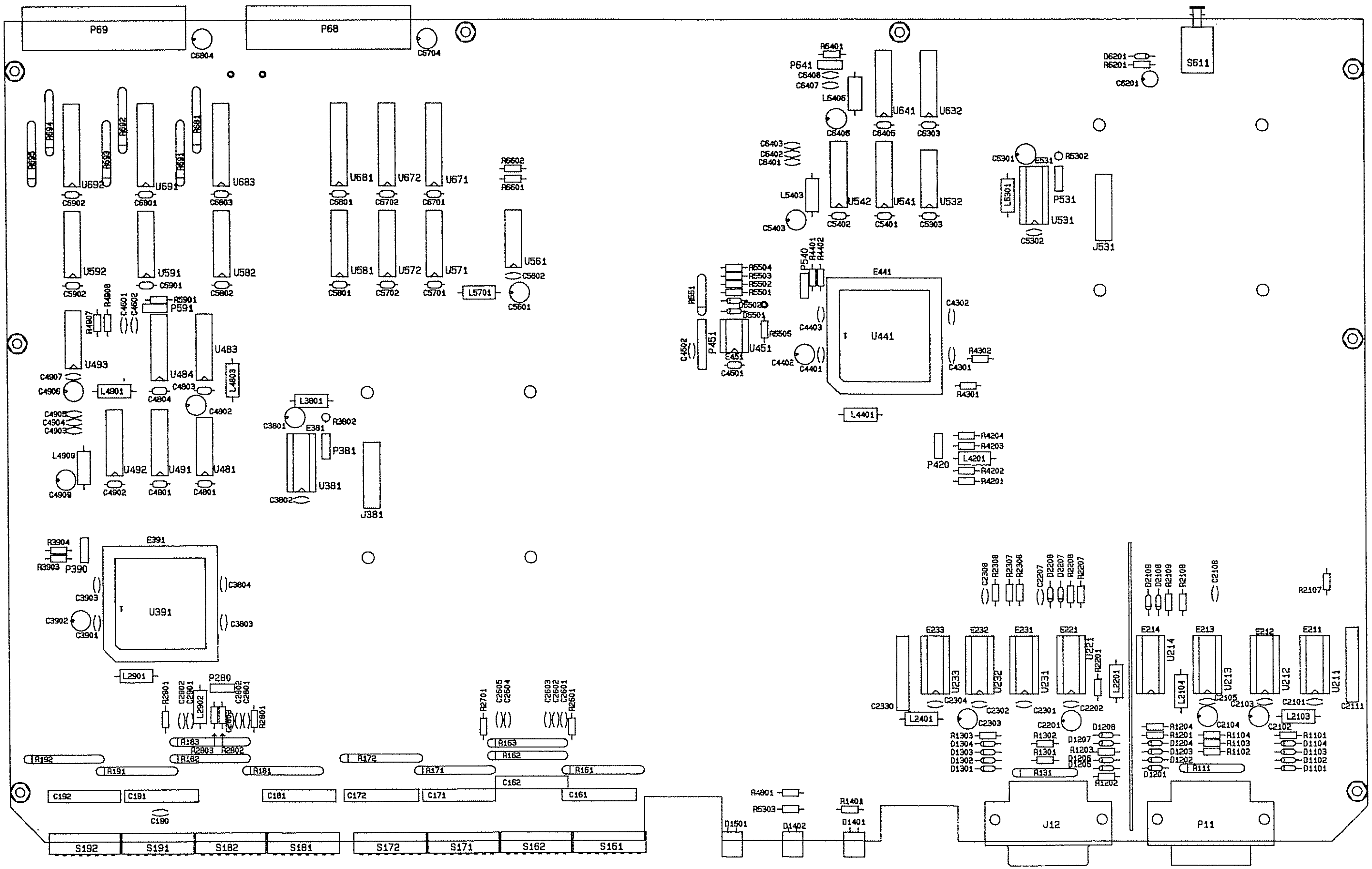
XBCLK	XWCLK	TX/RX Clock Source
OFF	OFF	Bit/word clock generated from REFCLK input
OFF	ON	not useful
ON	OFF	Word clock generated from external bit clock
ON	ON	Bit/word clocks from external source

System Reset and Download PROM

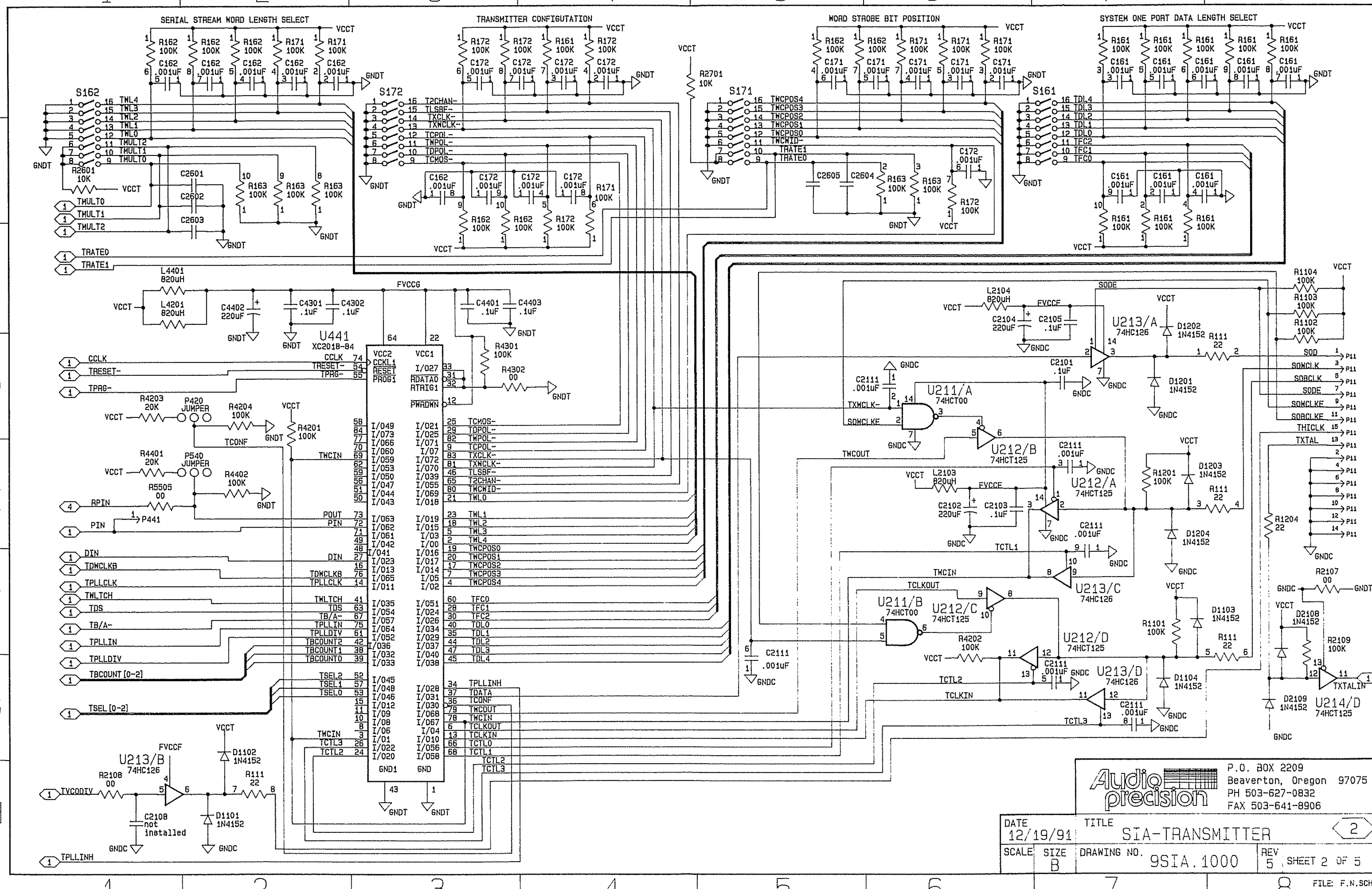
A simple RC circuit followed by a Schmitt trigger inverter is used to generate the system reset signals for both the transmitter and receiver. A SPST momentary switch, when depressed, pulls the transmit and receive XC2018 $\overline{RESET}$ and $\overline{PRG}$ pins low, initializing the PGAs for operation. Each $\overline{RESET}$ and $\overline{PRG}$ line can individually be disabled by the removal of jumper resistors R5501-R5504. This is useful only for system debugging. In normal operation the 0 Ohm resistors are installed.

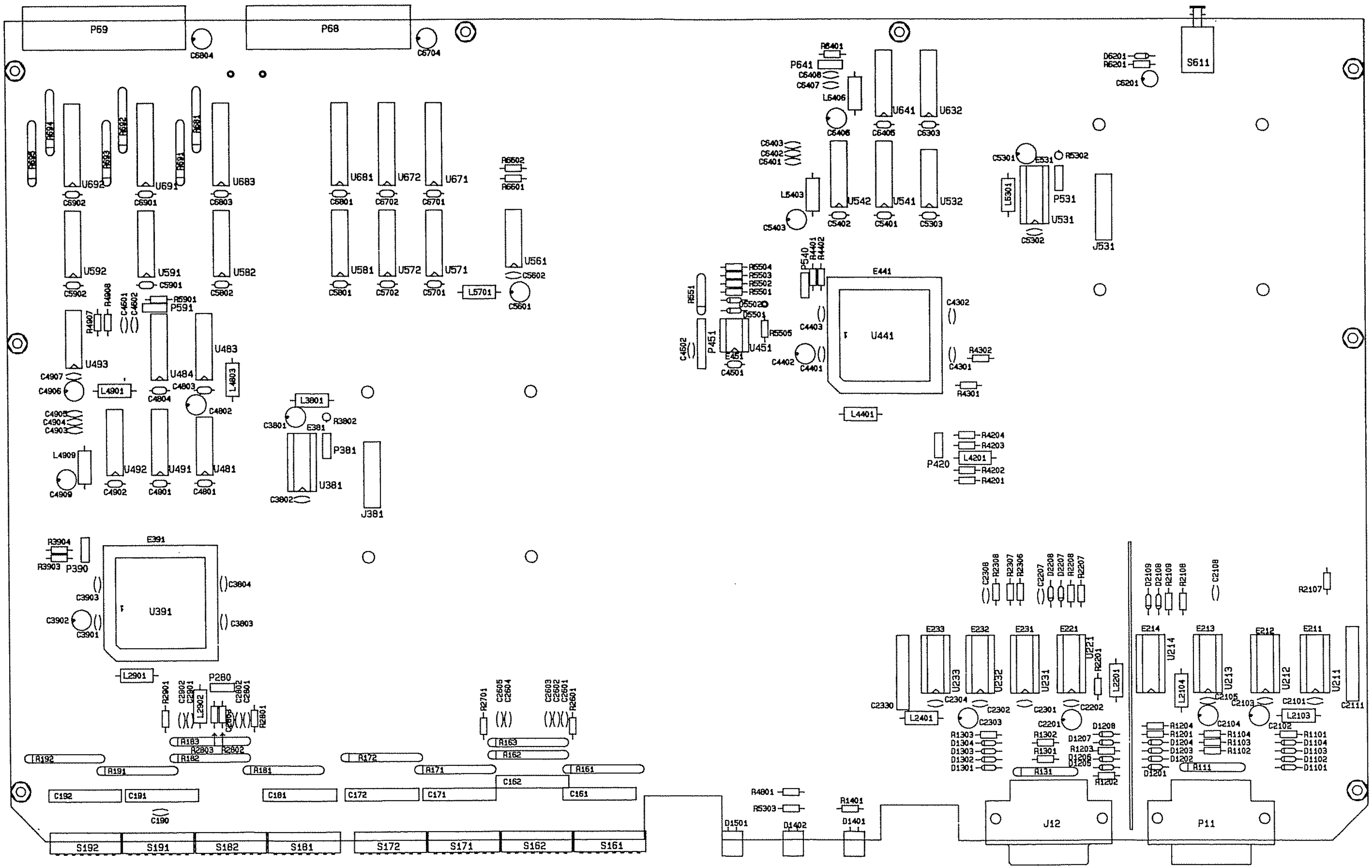
A single XC1736A serial PROM (U451) is used to download the PGA programming information into both XC2018s. During normal operation, the transmitter XC2018 generates a local bit clock that drives the download clock input on the receiver XC2018 and the PROM CCLK input. Two PGA configuration streams are stored in the PROM, the first of which is used to program the transmitter. After the transmitter is configured, the receiver XC2018 receives its serial download data from the transmitter XC2018 in a daisy-chain fashion.


SYSTEM ONE
PARALLEL OUTPUT PORT
ECO# | SHEET# | DATE | APPROVAL
91-058 | 1 - 5 | 12-12-91
U681 74HCT574
U672 74HCT574
U671 74HCT574
U581 74ACT251
U572 74ACT251
U571 74ACT251
U632 74HC590
U641 74ACT251
U541 74HC595
U542 74ACT251
U451 XC1736
U531/A 74ACT14
U532/A 74ACT14
U532/B 74ACT14
U561/B 74ACT14
U561/C 74ACT14
U561/D 74ACT14
U531/B 74ACT14
U531/C 74ACT14
U531/E 74ACT14
U531/F 74ACT14
U532/E 74ACT14
U532/D 74ACT14
LOCK DETECT
RANGE SELECT
P641 JUMPER
SYSTEM RESET SWITCH
S611
NOT INSTALLED
TDMCLKB
TDS
TB/A-
TWLTCH
TBCOUNT [0-2]
TSEL [0-2]
TPLLIN
TPLLDIV
TXTALIN
DIN
TRATE2
TRATE1
TRATE0
TVCODIV
TPLLCLK
TMULT0
TMULT1
TMULT2
TPLLINH
TRESET-
RRESET-
TPRG-
RPRG-
PIN
CCLK
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE 12/19/91
TITLE SIA-TRANSMITTER
SCALE
SIZE B
DRAWING NO. 9SIA.1000
REV 5
SHEET 1 OF 5
FILE: F.N.SCH

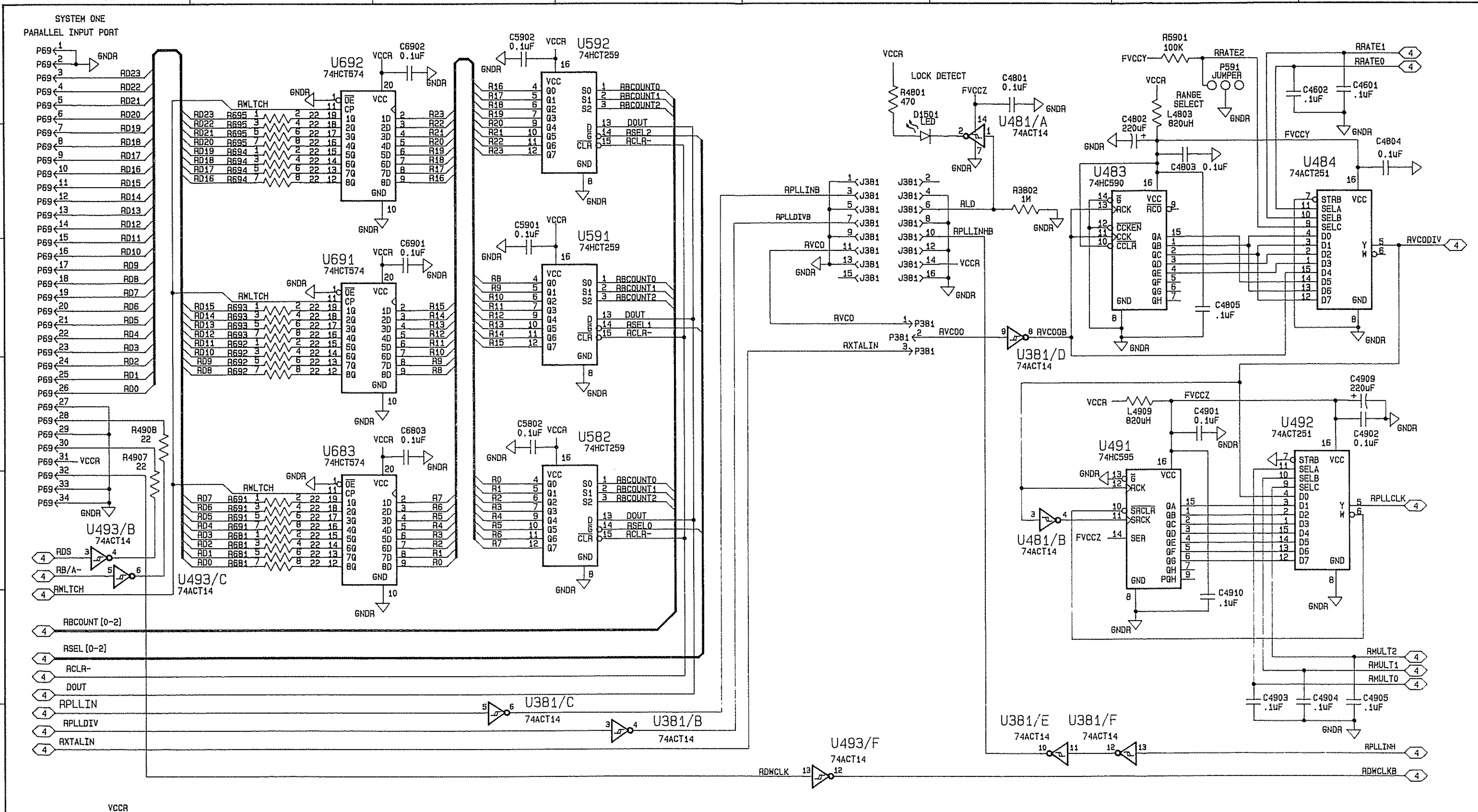


SIA-322 SERIAL INTERFACE ADAPTER 9SIA.1000 (6200.SIA1.5)


SERIAL STREAM WORD LENGTH SELECT
TRANSMITTER CONFIGUTATION
WORD STROBE BIT POSITION
SYSTEM ONE PORT DATA LENGTH SELECT
U441
XC2018-84
U211/A
74HCT00
U212/B
74HCT125
U213/A
74HC126
U212/A
74HCT125
U213/C
74HC126
U211/B
74HCT00
U212/C
74HCT125
U212/D
74HCT125
U213/D
74HC126
U214/D
74HCT125
U213/B
74HC126
Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
12/19/91
TITLE
SIA-TRANSMITTER
2
SCALE
SIZE
B
DRAWING NO.
9SIA.1000
REV
5
SHEET 2 OF 5
FILE: F.N.SCH



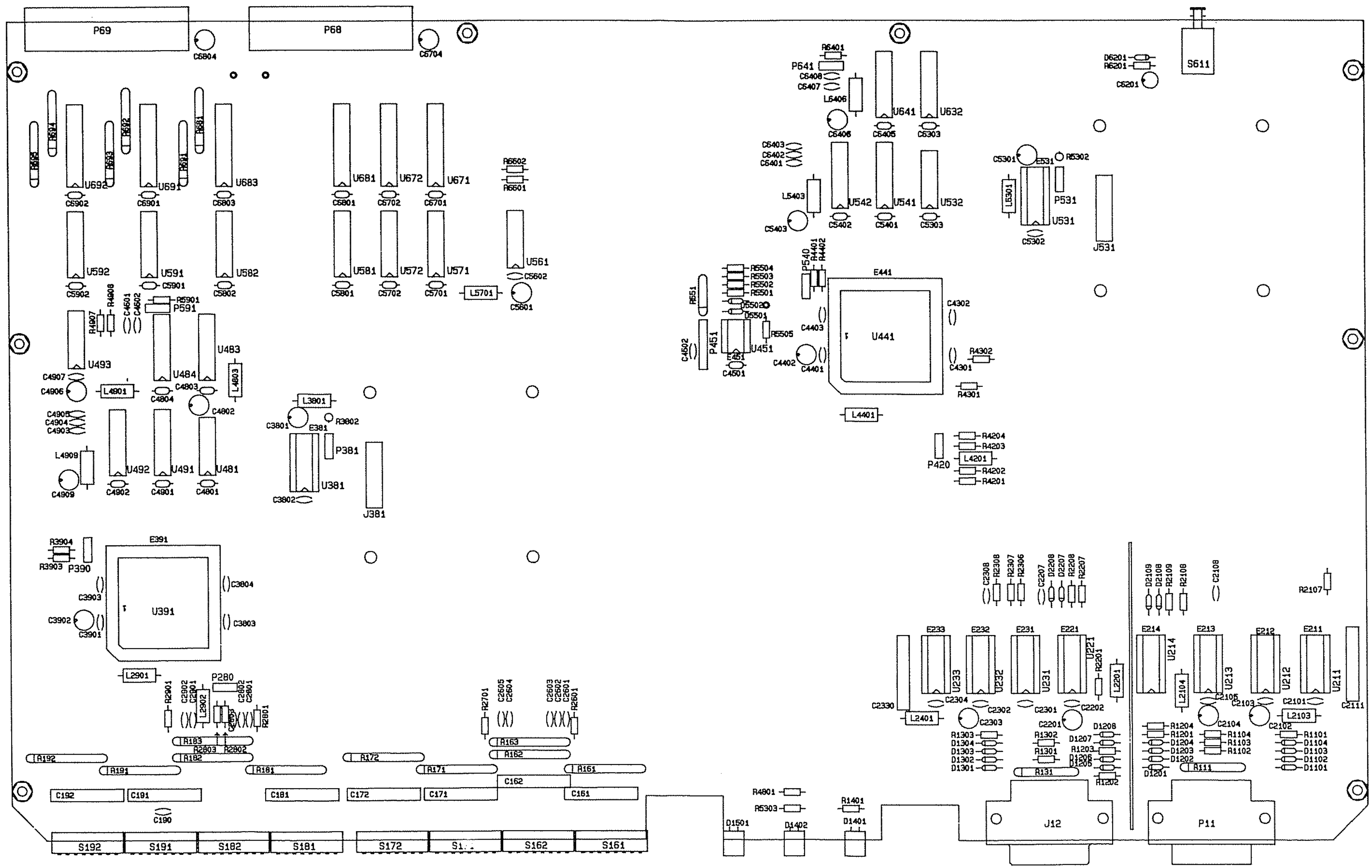
SIA-322 SERIAL INTERFACE ADAPTER 9SIA.1000 (6200.SIA1.5)



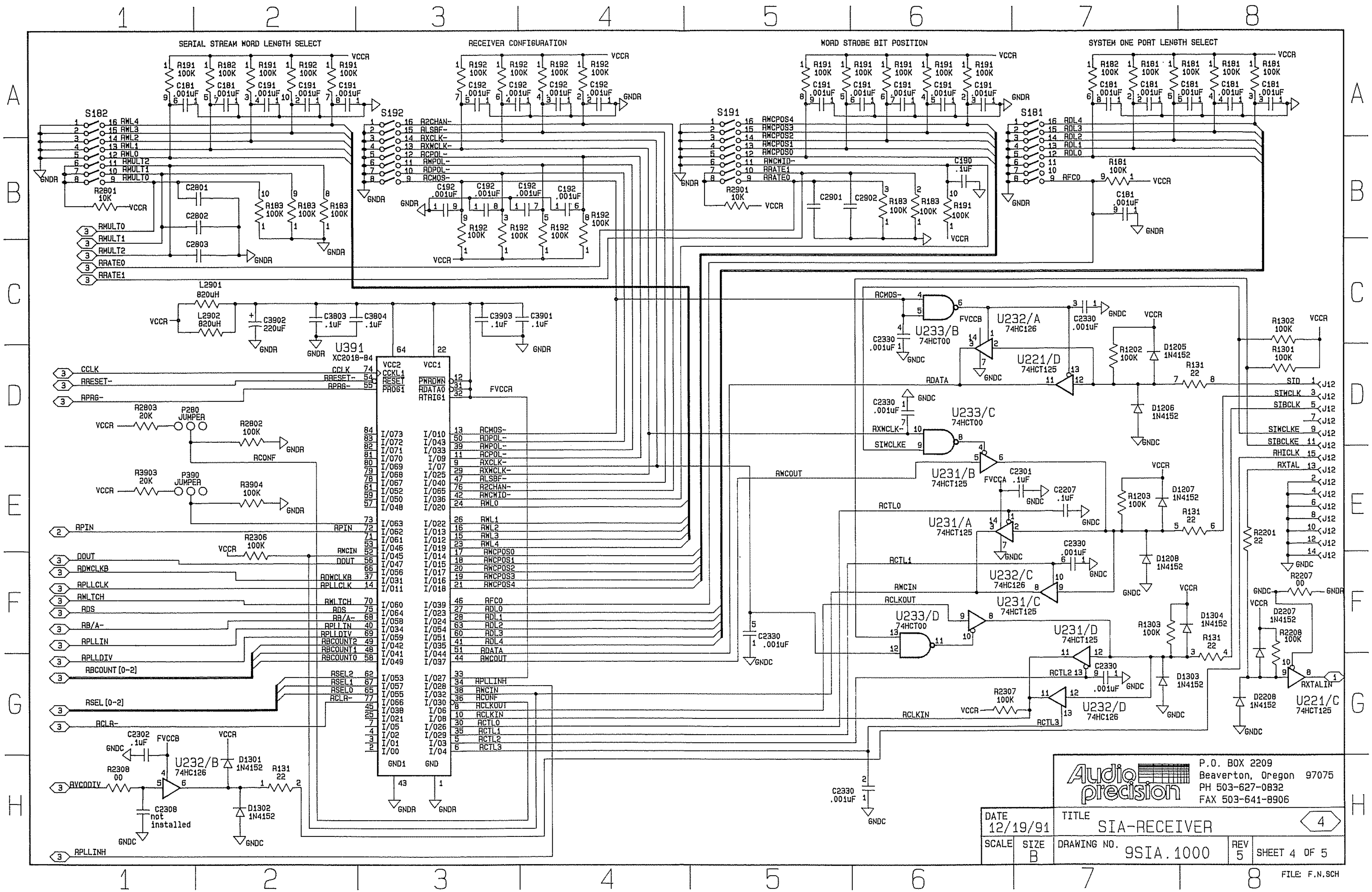
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

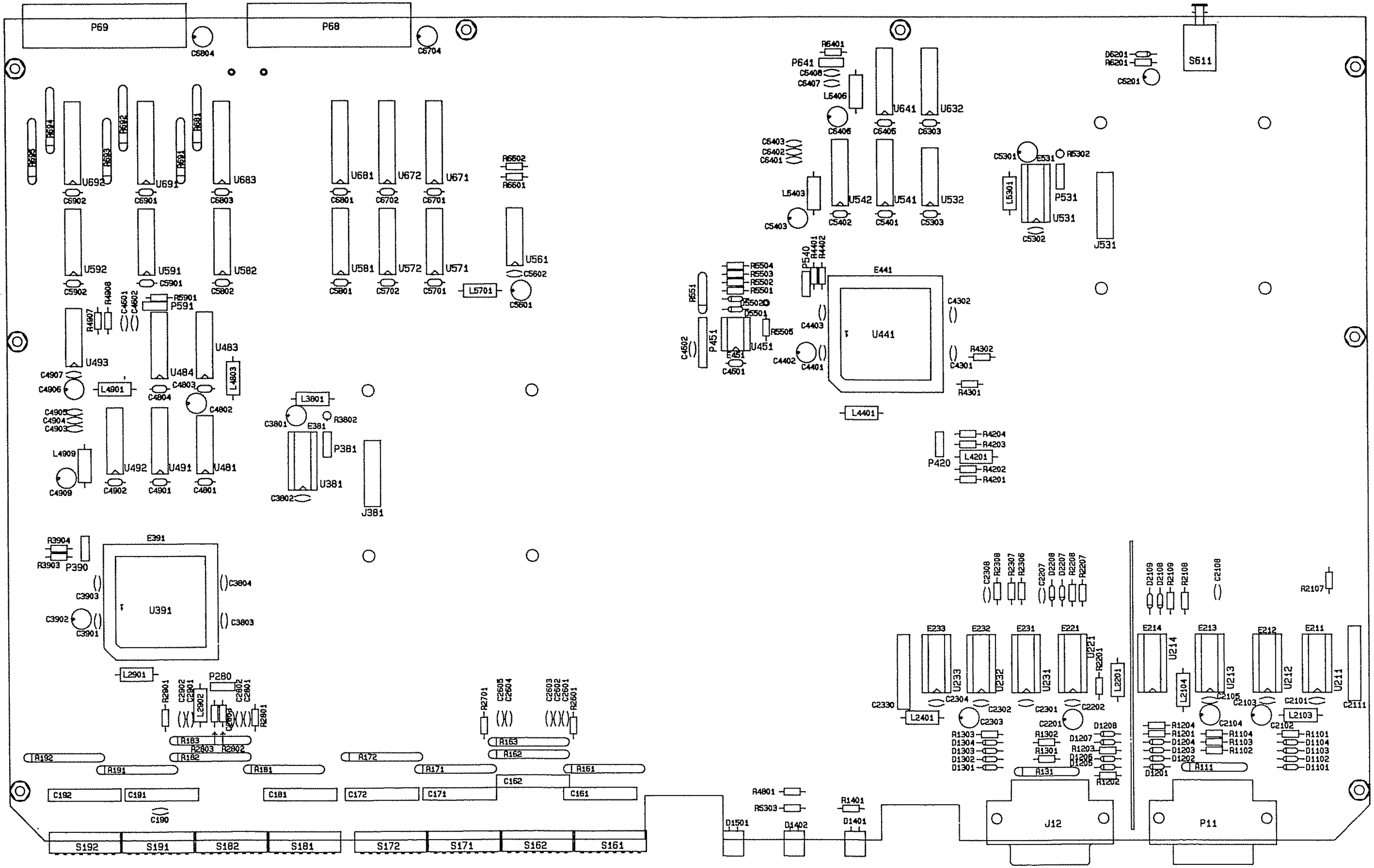
DATE	TITLE		
12/19/91	SIA-RECEIVER		3
SCALE / SIZE B	DRAWING NO. 9SIA.1000	REV 5	SHEET 3 OF 5

FILE: F.N.SCH

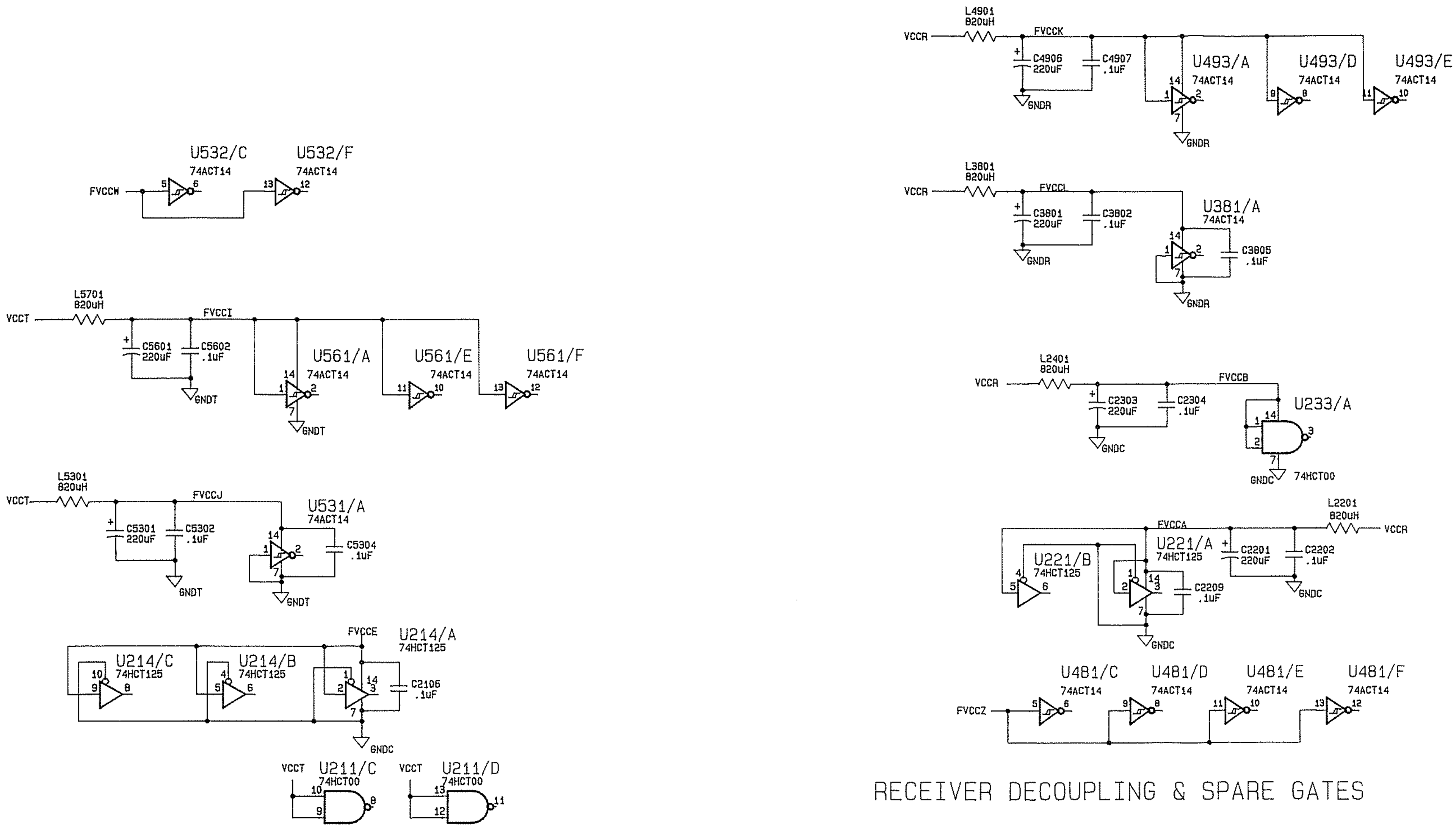


SIA-322 SERIAL INTERFACE ADAPTER 9SIA.1000 (6200.SIA1.5)


SERIAL STREAM WORD LENGTH SELECT
RECEIVER CONFIGURATION
WORD STROBE BIT POSITION
SYSTEM ONE PORT LENGTH SELECT
U391
XC2018-84
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906
DATE
12/19/91
TITLE
SIA-RECEIVER
4
SCALE
SIZE
B
DRAWING NO.
9SIA.1000
REV
5
SHEET 4 OF 5
FILE: F.N.SCH



SIA-322 SERIAL INTERFACE ADAPTER 9SIA.1000 (6200.SIA1.5)



TRANSMITTER DECOUPLING & SPARE GATES

RECEIVER DECOUPLING & SPARE GATES

Audio precision
P.O. BOX 2209
Beaverton, Oregon 97075
PH 503-627-0832
FAX 503-641-8906

DATE	TITLE		
12/19/91	DECOUPLING & SPARE GATES (5)		
SCALE / SIZE B	DRAWING NO. 9SIA.1000	REV 5	SHEET 5 OF 5

FILE: F.N.SCH

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C161	2A7,2A8,2B7	2051.8102	CAP CERNET SIP +80/-20%	.001u
C162	2A1,2A2,2B3	2051.8102	CAP CERNET SIP +80/-20%	.001u
C171	2A5,2A6	2051.8102	CAP CERNET SIP +80/-20%	.001u
C172	2A3,2A4,2B3,2B4,2B6	2051.8102	CAP CERNET SIP +80/-20%	.001u
C181	4A1,4A2,4A7,4A8	2051.8102	CAP CERNET SIP +80/-20%	.001u
C190	4B6	2172.0104	CAP CERAM 100V 20%	.1uF
C191	4A2,4A5,4A6	2051.8102	CAP CERNET SIP +80/-20%	.001u
C192	4A4,4B3,4B4	2051.8102	CAP CERNET SIP +80/-20%	.001u
C2101	2D7	2172.0104	CAP CERAM 100V 20%	.1uF
C2102	2E6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2103	2E6	2172.0104	CAP CERAM 100V 20%	.1uF
C2104	2C6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2105	2C7	2172.0104	CAP CERAM 100V 20%	.1uF
C2106	5F3	2454.0104	CAP POLYE 50V 5%	.1uF
C2111	2D6,2E7,2G7,2F5,2F6	2051.8102	CAP CERNET SIP +80/-20%	.001u
C2201	5E7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2202	5E7	2172.0104	CAP CERAM 100V 20%	.1uF
C2207	4E7	2172.0104	CAP CERAM 100V 20%	.1uF
C2209	5F7	2454.0104	CAP POLYE 50V 5%	.1uF
C2301	4E7	2172.0104	CAP CERAM 100V 20%	.1uF
C2302	4G1	2172.0104	CAP CERAM 100V 20%	.1uF
C2303	5D6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2304	5D6	2172.0104	CAP CERAM 100V 20%	.1uF
C2330	4F5,4C6,4D6,4F7,4G7,4C7	2051.8102	CAP CERNET SIP +80/-20%	.001u
C2601	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C2602	2B2	2172.0104	CAP CERAM 100V 20%	.1uF
C2603	2C2	2172.0104	CAP CERAM 100V 20%	.1uF
C2604	2B5	2172.0104	CAP CERAM 100V 20%	.1uF
C2605	2B5	2172.0104	CAP CERAM 100V 20%	.1uF
C2801	4B2	2172.0104	CAP CERAM 100V 20%	.1uF
C2802	4B2	2172.0104	CAP CERAM 100V 20%	.1uF
C2803	4C2	2172.0104	CAP CERAM 100V 20%	.1uF
C2901	4B5	2172.0104	CAP CERAM 100V 20%	.1uF
C2902	4B6	2172.0104	CAP CERAM 100V 20%	.1uF
C3801	5C6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C3802	5C6	2172.0104	CAP CERAM 100V 20%	.1uF
C3803	4C2	2172.0104	CAP CERAM 100V 20%	.1uF
C3804	4C3	2172.0104	CAP CERAM 100V 20%	.1uF
C3805	5F3	2454.0104	CAP POLYE 50V 5%	.1uF
C3901	4C4	2172.0104	CAP CERAM 100V 20%	.1uF
C3902	4C2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C3903	4C3	2172.0104	CAP CERAM 100V 20%	.1uF
C4301	2C2	2172.0104	CAP CERAM 100V 20%	.1uF
C4302	2C2	2172.0104	CAP CERAM 100V 20%	.1uF
C4401	2C3	2172.0104	CAP CERAM 100V 20%	.1uF
C4402	2C2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4403	2C4	2172.0104	CAP CERAM 100V 20%	.1uF
C4501	1G2	2172.0104	CAP CERAM 100V 20%	.1uF
C4502	1H4	2172.0220	CAP CERAM 100V 20%	22pF
C4601	3A8	2172.0104	CAP CERAM 100V 20%	.1uF
C4602	3A8	2172.0104	CAP CERAM 100V 20%	.1uF
C4801	3A6	2172.0104	CAP CERAM 100V 20%	.1uF

REPLACEABLE ELECTRICAL PARTS LIST: 9SIA.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
C4802	3B7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4803	3B7	2172.0104	CAP CERAM 100V 20%	.1uF
C4804	3B8	2172.0104	CAP CERAM 100V 20%	.1uF
C4805	3C7	2454.0104	CAP POLYE 50V 5%	.1uF
C4901	3D7	2172.0104	CAP CERAM 100V 20%	.1uF
C4902	3D8	2172.0104	CAP CERAM 100V 20%	.1uF
C4903	3F7	2172.0104	CAP CERAM 100V 20%	.1uF
C4904	3F7	2172.0104	CAP CERAM 100V 20%	.1uF
C4905	3F8	2172.0104	CAP CERAM 100V 20%	.1uF
C4906	5A6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4907	5A6	2172.0104	CAP CERAM 100V 20%	.1uF
C4909	3D8	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C4910	3E7	2454.0104	CAP POLYE 50V 5%	.1uF
C5301	5E2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5302	5E2	2172.0104	CAP CERAM 100V 20%	.1uF
C5303	1B6	2172.0104	CAP CERAM 100V 20%	.1uF
C5304	5E3	2454.0104	CAP POLYE 50V 5%	.1uF
C5401	1D7	2172.0104	CAP CERAM 100V 20%	.1uF
C5402	1D8	2172.0104	CAP CERAM 100V 20%	.1uF
C5403	1D7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5404	1E7	2454.0104	CAP POLYE 50V 5%	.1uF
C5601	5D2	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C5602	5D2	2172.0104	CAP CERAM 100V 20%	.1uF
C5701	1D4	2172.0104	CAP CERAM 100V 20%	.1uF
C5702	1C4	2172.0104	CAP CERAM 100V 20%	.1uF
C5801	1A4	2172.0104	CAP CERAM 100V 20%	.1uF
C5802	3D3	2172.0104	CAP CERAM 100V 20%	.1uF
C5901	3C3	2172.0104	CAP CERAM 100V 20%	.1uF
C5902	3A3	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	1G3	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6303	1B7	2172.0104	CAP CERAM 100V 20%	.1uF
C6304	1C7	2454.0104	CAP POLYE 50V 5%	.1uF
C6401	1F6	2172.0104	CAP CERAM 100V 20%	.1uF
C6402	1F7	2172.0104	CAP CERAM 100V 20%	.1uF
C6403	1F7	2172.0104	CAP CERAM 100V 20%	.1uF
C6405	1B8	2172.0104	CAP CERAM 100V 20%	.1uF
C6406	1B7	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C6407	1A8	2172.0104	CAP CERAM 100V 20%	.1uF
C6408	1A8	2172.0104	CAP CERAM 100V 20%	.1uF
C6701	1D2	2172.0104	CAP CERAM 100V 20%	.1uF
C6702	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C6704	1G1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C6801	1A2	2172.0104	CAP CERAM 100V 20%	.1uF
C6803	3D3	2172.0104	CAP CERAM 100V 20%	.1uF
C6804	3H1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C6901	3C3	2172.0104	CAP CERAM 100V 20%	.1uF
C6902	3A3	2172.0104	CAP CERAM 100V 20%	.1uF
D1101	2H2	3110.4152	DIODE SIGNAL	4152
D1102	2G2	3110.4152	DIODE SIGNAL	4152
D1103	2F7	3110.4152	DIODE SIGNAL	4152
D1104	2G7	3110.4152	DIODE SIGNAL	4152
D1201	2C7	3110.4152	DIODE SIGNAL	4152

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
D1202	2D7	3110.4152	DIODE SIGNAL	4152
D1203	2E7	3110.4152	DIODE SIGNAL	4152
D1204	2E7	3110.4152	DIODE SIGNAL	4152
D1205	4D7	3110.4152	DIODE SIGNAL	4152
D1206	4D7	3110.4152	DIODE SIGNAL	4152
D1207	4E7	3110.4152	DIODE SIGNAL	4152
D1208	4F7	3110.4152	DIODE SIGNAL	4152
D1301	4H2	3110.4152	DIODE SIGNAL	4152
D1302	4H2	3110.4152	DIODE SIGNAL	4152
D1303	4G7	3110.4152	DIODE SIGNAL	4152
D1304	4F8	3110.4152	DIODE SIGNAL	4152
D1401	1F6	3610.0004	LED .125 X.22	YELLOW
D1402	1B5	3610.0004	LED .125 X.22	YELLOW
D1501	3B5	3610.0004	LED .125 X.22	YELLOW
D2108	2F8	3110.4152	DIODE SIGNAL	4152
D2109	2G8	3110.4152	DIODE SIGNAL	4152
D2207	4F8	3110.4152	DIODE SIGNAL	4152
D2208	4G8	3110.4152	DIODE SIGNAL	4152
D5501	1G4	3110.4152	DIODE SIGNAL	4152
D5502	1G4	3110.4152	DIODE SIGNAL	4152
D6201	1G3	3110.4152	DIODE SIGNAL	4152
E211		4232.0014	SOCKET IC DIP	14 PIN
E212		4232.0014	SOCKET IC DIP	14 PIN
E213		4232.0014	SOCKET IC DIP	14 PIN
E214		4232.0014	SOCKET IC DIP	14 PIN
E221		4232.0014	SOCKET IC DIP	14 PIN
E231		4232.0014	SOCKET IC DIP	14 PIN
E232		4232.0014	SOCKET IC DIP	14 PIN
E233		4232.0014	SOCKET IC DIP	14 PIN
E381		4232.0014	SOCKET IC DIP	14 PIN
E391		4233.0084	SOCKET PLCC	84 PIN
E441		4233.0084	SOCKET PLCC	84 PIN
E451		4232.0008	SOCKET IC DIP	8 PIN
E531		4232.0014	SOCKET IC DIP	14 PIN
ECB01		6200.SIA1	ECB 2 LAYER 9.5X16.5	SIA
HS1		5112.1112.5	SCREW MC FLT PH BGE	#4-40X3/8
HS10		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
HS11		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
HS12		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
HS13		5532.1106.1	STANDOFF HEX M/F	JACK SCREW
HS14		5532.1106.1	STANDOFF HEX M/F	JACK SCREW
HS15		5532.1106.1	STANDOFF HEX M/F	JACK SCREW
HS16		5532.1106.1	STANDOFF HEX M/F	JACK SCREW
HS2		5112.1112.5	SCREW MC FLT PH BGE	#4-40X3/8
HS3		5112.1112.5	SCREW MC FLT PH BGE	#4-40X3/8
HS4		5112.1112.5	SCREW MC FLT PH BGE	#4-40X3/8
HS5		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
HS6		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
HS7		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
HS8		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
HS9		5112.7108	SCREW MC SEM PH ZN	#4-40X1/4
J12	4D8,4E8	4225.0015	JACK D-SUB PC 90'	15 PIN

REPLACEABLE ELECTRICAL PARTS LIST: 9SIA.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
J381	3B5,3C5	4221.1016	JACK PC 2 X .1	16 PIN
J531	1C5	4221.1016	JACK PC 2 X .1	16 PIN
L2103	2E6	4510.0821	INDUCTOR 10 OHM	820uH
L2104	2C6	4510.0821	INDUCTOR 10 OHM	820uH
L2201	5E7	4510.0821	INDUCTOR 10 OHM	820uH
L2401	5D6	4510.0821	INDUCTOR 10 OHM	820uH
L2901	4C2	4510.0821	INDUCTOR 10 OHM	820uH
L2902	4C2	4510.0821	INDUCTOR 10 OHM	820uH
L3801	5C6	4510.0821	INDUCTOR 10 OHM	820uH
L4201	2C1	4510.0821	INDUCTOR 10 OHM	820uH
L4401	2C1	4510.0821	INDUCTOR 10 OHM	820uH
L4803	3B7	4510.0821	INDUCTOR 10 OHM	820uH
L4901	5B6	4510.0821	INDUCTOR 10 OHM	820uH
L4909	3D7	4510.0821	INDUCTOR 10 OHM	820uH
L5301	5E2	4510.0821	INDUCTOR 10 OHM	820uH
L5403	1D8	4510.0821	INDUCTOR 10 OHM	820uH
L5701	5C2	4510.0821	INDUCTOR 10 OHM	820uH
L6406	1B8	4510.0821	INDUCTOR 10 OHM	820uH
M1		7110.0041	CHASSIS WRAP	SIA
M2		7130.0031	FRONT PANEL	SIA
M3		7310.0002	BRACKET COVER SUPPORT	DCX
P11	2D8,2E8	4225.0115	PLUG D-SUB PC 90'	15 PIN
P280	4D2	4221.0036	PLUG PC .1 X.43	36 PIN
P381	3C5	4221.0036	PLUG PC .1 X.43	36 PIN
P390	4E2	4221.0036	PLUG PC .1 X.43	36 PIN
P420	2D2	4221.0036	PLUG PC .1 X.43	36 PIN
P531	1D5	4221.0036	PLUG PC .1 X.43	36 PIN
P540	2E2	4221.0036	PLUG PC .1 X.43	36 PIN
P591	3A7	4221.0036	PLUG PC .1 X.43	36 PIN
P641	1A7	4221.0036	PLUG PC .1 X.43	36 PIN
P68	1A1-1E1	4221.0134	PLUG PC 90' SHROUDED	34 PIN
P69	3A1-3E1	4221.0134	PLUG PC 90' SHROUDED	34 PIN
R1101	2F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1102	2C8	1214.0104	RES 1/4W/C/FLM 5%	100K
R1103	2C8	1214.0104	RES 1/4W/C/FLM 5%	100K
R1104	2C8	1214.0104	RES 1/4W/C/FLM 5%	100K
R111	2D7,2E8,2G8,2H2	1984.4220	RES NET SIP 5% I	4 X 22
R1201	2E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1202	4D7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1203	4E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1204	2E8	1214.0220	RES 1/4W C FLM 5%	22
R1301	4D8	1214.0104	RES 1/4W/C/FLM 5%	100K
R1302	4C8	1214.0104	RES 1/4W/C/FLM 5%	100K
R1303	4F6	1214.0104	RES 1/4W/C/FLM 5%	100K
R131	4H2,4E8,4D8	1984.4220	RES NET SIP 5% I	4 X 22
R1401	1F5	1214.0471	RES 1/4W C FLM 5%	470
R161	2A4,2A7,2A8,2C7	1984.9104	RES NET SIP 5% B	9 X 100K
R162	2A1,2A2,2A5,2C3	1984.9104	RES NET SIP 5% B	9 X 100K
R163	2B2,2B6	1984.9104	RES NET SIP 5% B	9 X 100K
R171	2A2,2A6,2B4	1984.9104	RES NET SIP 5% B	9 X 100K
R172	2A3,2A4,2C4,2B6	1984.9104	RES NET SIP 5% B	9 X 100K
R181	4A7,4A8,4B7	1984.9104	RES NET SIP 5% B	9 X 100K

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
R182	4A2,4A7	1984.9104	RES NET SIP 5% B	9 X 100K
R183	4B2,4B6	1984.9104	RES NET SIP 5% B	9 X 100K
R191	4A1,4A2,4A5,4A6,4B6	1984.9104	RES NET SIP 5% B	9 X 100K
R192	4A3,4A4,4B4,4C3,4C4	1984.9104	RES NET SIP 5% B	9 X 100K
R2107	2F8	1214.0000	JUMPER .4 X.25	00
R2108	2H1	1214.0000	JUMPER .4 X.25	00
R2109	2F8	1214.0104	RES 1/4W/C/FLM 5%	100K
R2201	4E8	1214.0220	RES 1/4W C FLM 5%	22
R2207	4F8	1214.0000	JUMPER .4 X.25	00
R2208	4F8	1214.0104	RES 1/4W/C/FLM 5%	100K
R2306	4E2	1214.0104	RES 1/4W/C/FLM 5%	100K
R2307	4G6	1214.0104	RES 1/4W/C/FLM 5%	100K
R2308	4H1	1214.0000	JUMPER .4 X.25	00
R2601	2B1	1214.0203	RES 1/4W C FLM 5%	20K
R2701	2A5	1214.0203	RES 1/4W C FLM 5%	20K
R2801	4B1	1214.0203	RES 1/4W C FLM 5%	20K
R2802	4D2	1214.0104	RES 1/4W/C/FLM 5%	100K
R2803	4D1	1214.0203	RES 1/4W C FLM 5%	20K
R2901	4B5	1214.0203	RES 1/4W C FLM 5%	20K
R3802	3B6	1214.0105	RES 1/4W C FLM 5%	1M
R3903	4E1	1214.0203	RES 1/4W C FLM 5%	20K
R3904	4E2	1214.0473	RES 1/4W C FLM 5%	47K
R4201	2D2	1214.0104	RES 1/4W/C/FLM 5%	100K
R4202	2F6	1214.0104	RES 1/4W/C/FLM 5%	100K
R4203	2D2	1214.0203	RES 1/4W C FLM 5%	20K
R4204	2D2	1214.0104	RES 1/4W/C/FLM 5%	100K
R4301	2D3	1214.0104	RES 1/4W/C/FLM 5%	100K
R4302	2D3	1214.0000	JUMPER .4 X.25	00
R4401	2E2	1214.0203	RES 1/4W C FLM 5%	20K
R4402	2E2	1214.0104	RES 1/4W/C/FLM 5%	100K
R4801	3A5	1214.0471	RES 1/4W C FLM 5%	470
R4907	3D1	1214.0220	RES 1/4W C FLM 5%	22
R4908	3D1	1214.0220	RES 1/4W C FLM 5%	22
R5302	1C6	1214.0105	RES 1/4W C FLM 5%	1M
R5303	1B5	1214.0471	RES 1/4W C FLM 5%	470
R5501	2E1	1214.0000	JUMPER .4 X.25	00
R5502	1G4	1214.0000	JUMPER .4 X.25	00
R5503	1H4	1214.0000	JUMPER .4 X.25	00
R5504	1G4	1214.0000	JUMPER .4 X.25	00
R5505	2E1	1214.0000	JUMPER .4 X.25	00
R551	1G4,1G5,1H4	1985.4223	RES NET SIP 2% B	4 X 22K
R5901	3A7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6201	1G3	1214.0224	RES 1/4W M FLM 5%	220K
R6401	1A7	1214.0104	RES 1/4W/C/FLM 5%	100K
R6601	1E1	1214.0220	RES 1/4W C FLM 5%	22
R6602	1D1	1214.0220	RES 1/4W C FLM 5%	22
R681	3E2	1984.4220	RES NET SIP 5% I	4 X 22
R691	3E2	1984.4220	RES NET SIP 5% I	4 X 22
R692	3D2	1984.4220	RES NET SIP 5% I	4 X 22
R693	3C2	1984.4220	RES NET SIP 5% I	4 X 22
R694	3B2	1984.4220	RES NET SIP 5% I	4 X 22
R695	3B2	1984.4220	RES NET SIP 5% I	4 X 22

REPLACEABLE ELECTRICAL PARTS LIST: 9SIA.1000

ITEM	SCHEMATIC LOCATOR	A-P NUMBER	ITEM DESCRIPTION	
S161	2A7	4311.0008	SWITCH DIP 90'	8 POLE
S162	2A1	4311.0008	SWITCH DIP 90'	8 POLE
S171	2A5	4311.0008	SWITCH DIP 90'	8 POLE
S172	2A3	4311.0008	SWITCH DIP 90'	8 POLE
S181	4A7	4311.0008	SWITCH DIP 90'	8 POLE
S182	4A1	4311.0008	SWITCH DIP 90'	8 POLE
S191	4A5	4311.0008	SWITCH DIP 90'	8 POLE
S192	4A3	4311.0008	SWITCH DIP 90'	8 POLE
S611	1G2	4321.0004	SWITCH PUSH MOMENTARY	SPDT
TAG01		8500.0001	TAG .5 X1.2	W/PSA SER #,EPROM
U211	2D6,2F6,5G3	3324.0000	GATE 4 X 2-IN NAND	74HCT00
U212	2E6,2E7,2F6,2F7	3324.0125	BUFFER 4X TRI-ST	74HCT125
U213	2E7,2F8,2G8,2H1	3323.0126	BUFFER 4X TRI-ST	74HC126
U214	2G8,5F2,5F3	3324.0125	BUFFER 4X TRI-ST	74HCT125
U221	5D6	3324.0125	BUFFER 4X TRI-ST	74HCT125
U231	4D7,4E6,4F6,4F7	3324.0125	BUFFER 4X TRI-ST	74HCT125
U232	4H1,4C6,4F6,4G7	3323.0126	BUFFER 4X TRI-ST	74HC126
U233	4C6,4D6,4F6,5D7	3324.0000	GATE 4 X 2-IN NAND	74HCT00
U381	3G3,3G4,3C6,3G6,5C7	3326.0014	TRIGGER SCHMITT 8X	74ACT14
U391	4D3-4H3	3343.2018	LOGIC CELL ARRAY	XC2018
U441	2D3-2H3	3343.2018	LOGIC CELL ARRAY	XC2018
U451	1G2	3723.1736	PROM CMOS SERIAL	36K X 1
U481	3A6,3D6,5F6,5F7	3326.0014	TRIGGER SCHMITT 8X	74ACT14
U483	3B6	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U484	3B8	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U491	3D6	3323.0595	SHIFT REG 8BIT W/LATCH	74HC595
U492	3D7	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U493	3G5,3E1,5B7,5B8	3326.0014	TRIGGER SCHMITT 8X	74ACT14
U531	1F3,1F5,1F6,1D6,5E3	3326.0014	TRIGGER SCHMITT 8X	74ACT14
U532	1E6,1B6,1G3,1G4,5B2	3326.0014	TRIGGER SCHMITT 8X	74ACT14
U541	1D7	3323.0595	SHIFT REG 8BIT W/LATCH	74HC595
U542	1D8	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U561	1E1,5D3,5D4	3326.0014	TRIGGER SCHMITT 8X	74ACT14
U571	1D4	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U572	1C4	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U581	1A4	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U582	3D4	3324.0259	LATCH 8X ADDRESSABLE	74HCT259
U591	3C4	3324.0259	LATCH 8X ADDRESSABLE	74HCT259
U592	3A4	3324.0259	LATCH 8X ADDRESSABLE	74HCT259
U632	1B6	3323.0590	COUNTER 8-BIT TRI-ST	74HC590
U641	1B8	3326.0251	MULTIPLEXER TRI-ST	74ACT251
U671	1D2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U672	1C2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U681	1A2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U683	3D2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U691	3C2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574
U692	3A2	3324.0574	FLIP-FLOP 8X D TRI-ST	74HCT574

SECTION 6
MECHANICAL DIAGRAMS & PARTS LISTS

This section contains exploded drawings and replaceable mechanical parts lists for the System One, the SWR-122 switcher family, the DCX-127 multifunction accessory, and the SIA-322 serial interface adapter. Unless otherwise specified, all dimensions are in inches. When ordering a replacement part please include the instrument or system nomenclature in addition to the Audio Precision part number and item description.

ABBREVIATIONS used in the MECHANICAL PARTS LISTS

"	Inch
#	Number or Size
A	Ampere
AL	Aluminum
ANLR	Analyzer
ASSY	Assembly
AUX	Auxiliary
BAN	Banana
BGE	Beige
BLK	Black
BO	Black Oxide
BZ	Black Zinc
COND	Conductor
CONN	Connector
CONT	Continuous
C&S	Cut and Strip
D-SUB	D-Subminiature
ECB	Etched Circuit Board
EL	Electro-luminescent
F	Female
FLT	Flat head
Ga	Gauge
GEN	Generator
GNDED	Grounded
GRY	Grey
HDWR	Hardware
HEX	Hexagonal
INSUL	Insulated
INT	Internal
INTF	Interface
I/O	Input/Output
LED	Light Emitting Diode
M	Male
MC	Machine
M/F	Male / Female
MOD	Module
MON	Monitor
MT	Mount
PAN	Pan Head
PC	Printed Circuit
PH	Phillips
PNL	Panel
POLY	Polyethylene
PSA	Pressure Sensitive Adhesive
RBN	Ribbon
RND	Round
RT	Right
SEM	SEMS Captive Washer
SHLD	Shield
SS	Stainless Steel
TF	Thread Forming
THRD	Thread or Threaded
TRS	Truss Head
VSEL	Voltage Selector
W/	With
W/O	Without
XFMR	Transformer
ZN	Zinc

SECTION 6
MECHANICAL DIAGRAMS & PARTS LISTS

This section contains exploded drawings and replaceable mechanical parts lists for the System One, the SWR-122 switcher family, the DCX-127 multifunction accessory, and the SIA-322 serial interface adapter. Unless otherwise specified, all dimensions are in inches. When ordering a replacement part please include the instrument or system nomenclature in addition to the Audio Precision part number and item description.

ABBREVIATIONS used in the MECHANICAL PARTS LISTS

"	Inch	INTF	Interface
#	Number or Size	I/O	Input/Output
A	Ampere	LED	Light Emitting Diode
AL	Aluminum	M	Male
ANLR	Analyzer	MC	Machine
ASSY	Assembly	M/F	Male / Female
AUX	Auxiliary	MOD	Module
BAN	Banana	MON	Monitor
BGE	Beige	MT	Mount
BLK	Black	PAN	Pan Head
BO	Black Oxide	PC	Printed Circuit
BZ	Black Zinc	PH	Phillips
COND	Conductor	PNL	Panel
CONN	Connector	POLY	Polyethylene
CONT	Continuous	PSA	Pressure Sensitive Adhesive
C&S	Cut and Strip	RBN	Ribbon
D-SUB	D-Subminiature	RND	Round
ECB	Etched Circuit Board	RT	Right
EL	Electro-luminescent	SEM	SEMS Captive Washer
F	Female	SHLD	Shield
FLT	Flat head	SS	Stainless Steel
Ga	Gauge	TF	Thread Forming
GEN	Generator	THRD	Thread or Threaded
GNDED	Grounded	TRS	Truss Head
GRY	Grey	VSEL	Voltage Selector
HDWR	Hardware	W/	With
HEX	Hexagonal	W/O	Without
INSUL	Insulated	XFMR	Transformer
INT	Internal	ZN	Zinc

Replaceable Mechanical Parts List for Figure 6.1

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7170.0001	Rack Ear
-2	5113.1110.1	Screw, MC FLT PH GRY #6-32 x 5/16
-3	7150.0001	Cover, Top & Bottom Mainframe
-4	5113.1108.1	Screw, MC FLT PH GRY #6-32 x 1/4
-5	5621.0001	Foam w/PSA, .25 x .75 x 3.75
-6	8500.0003	Label, Warning Power Supply
-7	7150.0002	Cover, Tunnel Mainframe
-8	5620.0101	Grommet, Cont Polye 2.4 x .031
-9	5113.7112	Screw, MC SEM PH ZN #6-32 x 3/8
-10	5113.1108	Screw, MC FLT PH ZN #6-32 x 1/4
-11	7140.0001.2	Rear Panel with A-version digital interface option
	7140.0003	Rear Panel with G-version digital interface option
	7140.0004	Rear Panel with S-version digital interface option
-12	7120.0001	Side Panel, Mainframe
-13	5640.0001	Tape, BLK 0.001 x .5
-14	7110.0001.1	Chassis Plate, Mainframe
-15	4800.0315	Fan, 3.15 x 3.15 x 1.5
-16	5222.0001	Nut, KEP #4-40
-17	7161.0001	Shield, Fan
-18	7130.0001.1	Front Panel, Mainframe
-19	5660.0001	Filter, Fan 4 x 4 Foam
-20	7130.0002	Fan Grill, SYS-22/-11/-02/-20 configurations
	7130.0002.1	Fan Grill, SYS-222/-202 configurations
	7130.0002.2	Fan Grill, SYS-322/-302 configurations
-21	5112.3140	Screw, MC PAN PH ZN #4-40 x 1.25
-22	4350.0001	Switch, Rocker DPDT
-23	7130.0003	Escutcheon, Switch Panel
-24	7110.0002	Bracket, XFMR mounting
-25	5113.7112	Screw, MC SEM PH ZN #6-32 x 3/8
-26	4522.0002	XFMR, Power, plus mounting hardware
		NOTE: Older systems contain a large "E-I" style power transformer. Please contact Audio Precision for information regarding replacement.
-27	5115.8880	Screw, MC HEX Hx ZN #10-32 x 2.5
-28	5630.0001	Feet, BLK .5 x .5 x .25
-29	4540.0001	Line Conn, Vsel, Fuse Holder, RFI Filter
-30	5113.7116	Screw, MC SEM PH ZN #6-32 x 1/2
-31	3610.0004	LED, .125 x .22 YEL MV53124
-32	5620.0001	Insulator, Mica TO3
-33	3221.5883	Transistor, PNP TO3 2N5883

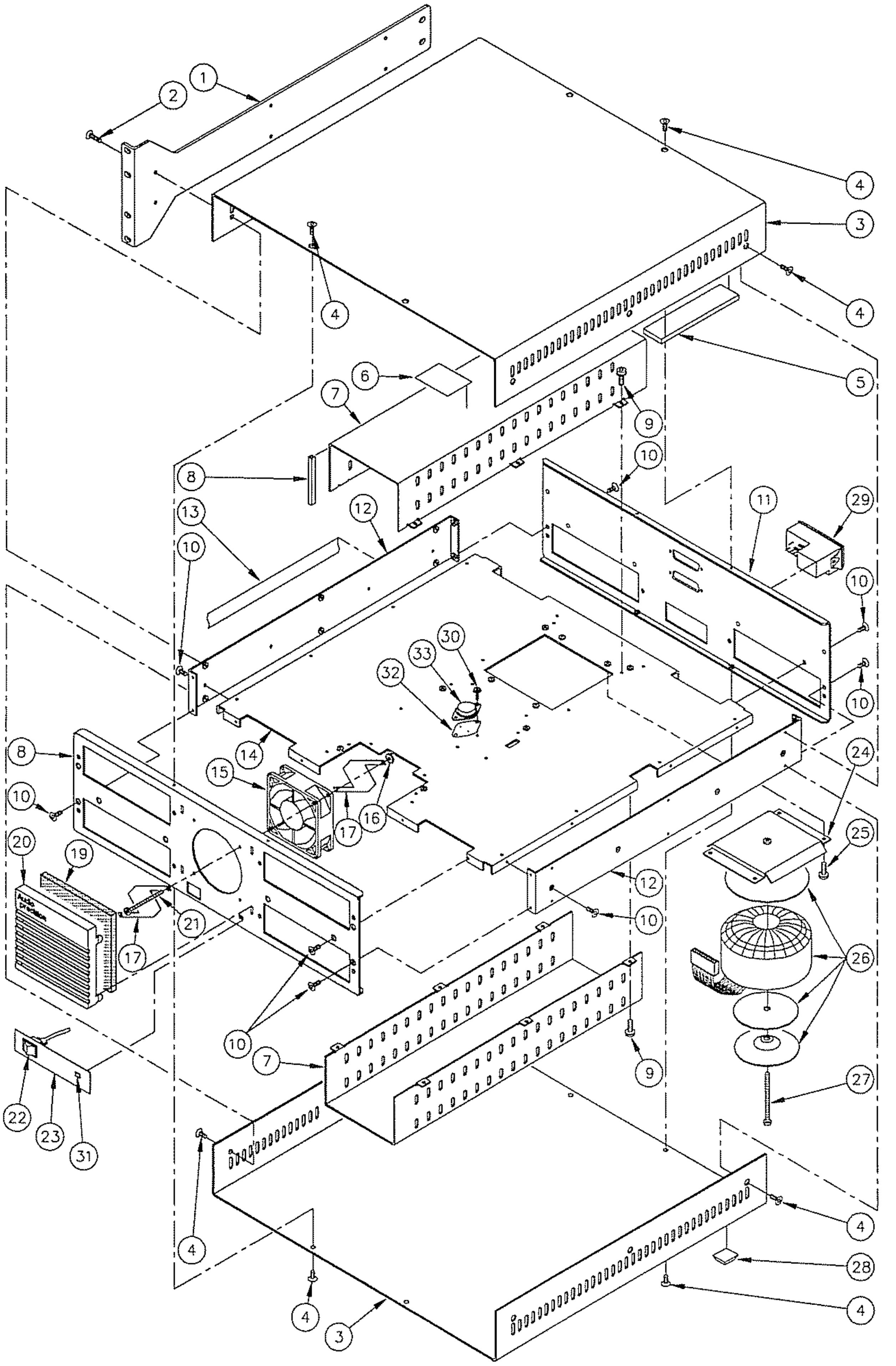
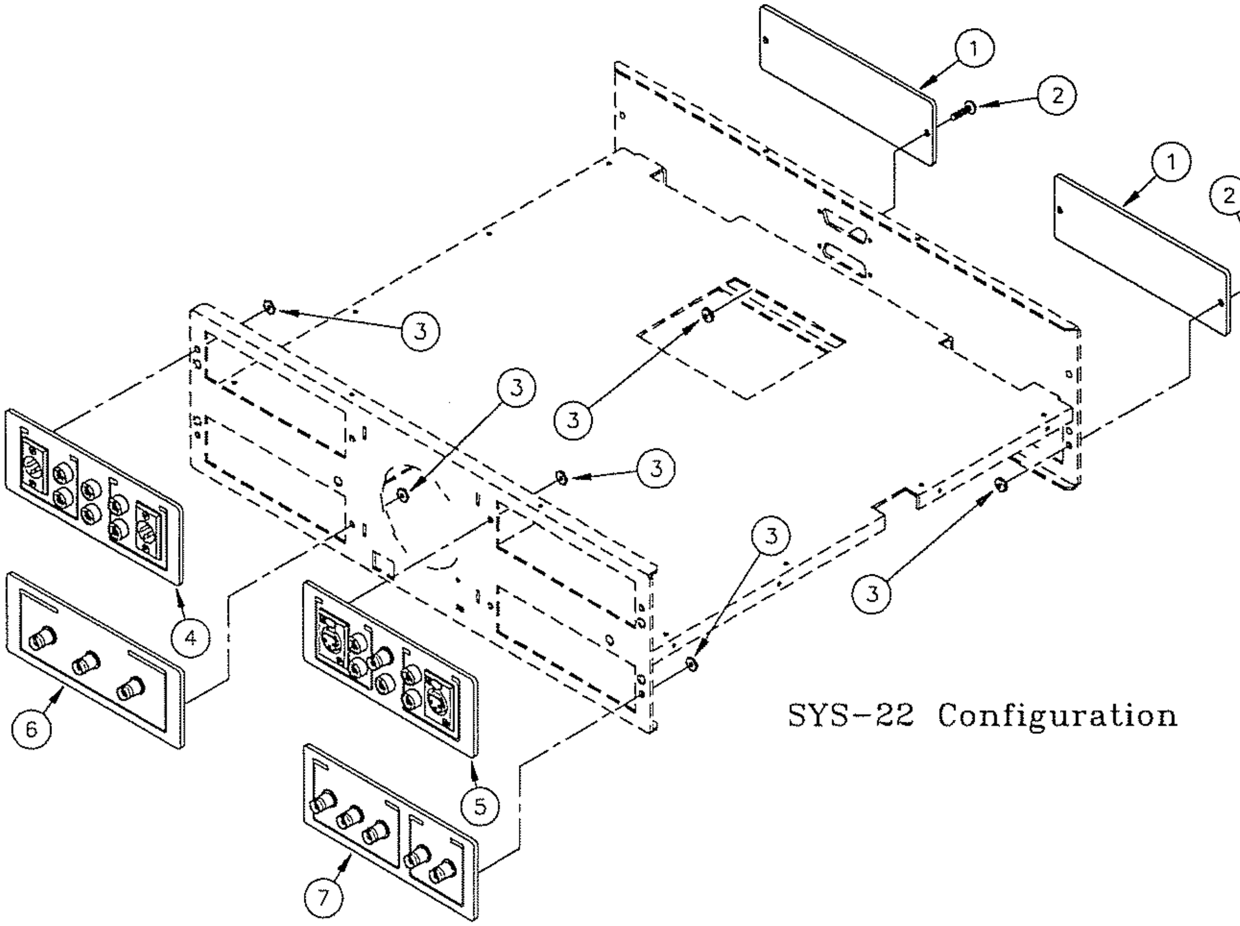


Figure 6.1 SYSTEM ONE MAINFRAME ENCLOSURE ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.2a

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7140.0002	Rear Cover Panel
-2	5114.4116	Screw, MC TRS PH ZN #8-32 x 1/2
-3	5224.0001	Nut, KEP #8-32
-4	9XMB.2000	GEN Output Panel
-5	9XFM.2000	ANLR Input Panel
-6	9BNC.3010	GEN Aux Panel
-7	9BNC.5000	ANLR Aux Panel
-8	9XMB.1000	SYS-11 GEN Panel
-9	9XFB.1000	SYS-11 ANLR Panel
-10	9XMS.2000	GEN MON Panel for SYS-20
	9XMS.3000	GEN MON Panel for SYS-20 with option DSP
-11	9XFS.2000	GEN MON Panel for SYS-02
	9XFS.3000	GEN MON Panel for SYS-202 and SYS-302
-12	7131.0000	Blank Front Panel
-13	9BNC.6000	SYS-2xx Aux Panel
-14	9DDR.3000	SYS-3xx Rear Panel
-15	9DDF.3010	SYS-3xx Serial I/O Panel, with optical
-16	9DDF.3000	SYS-3xx Serial I/O Panel, w/o optical



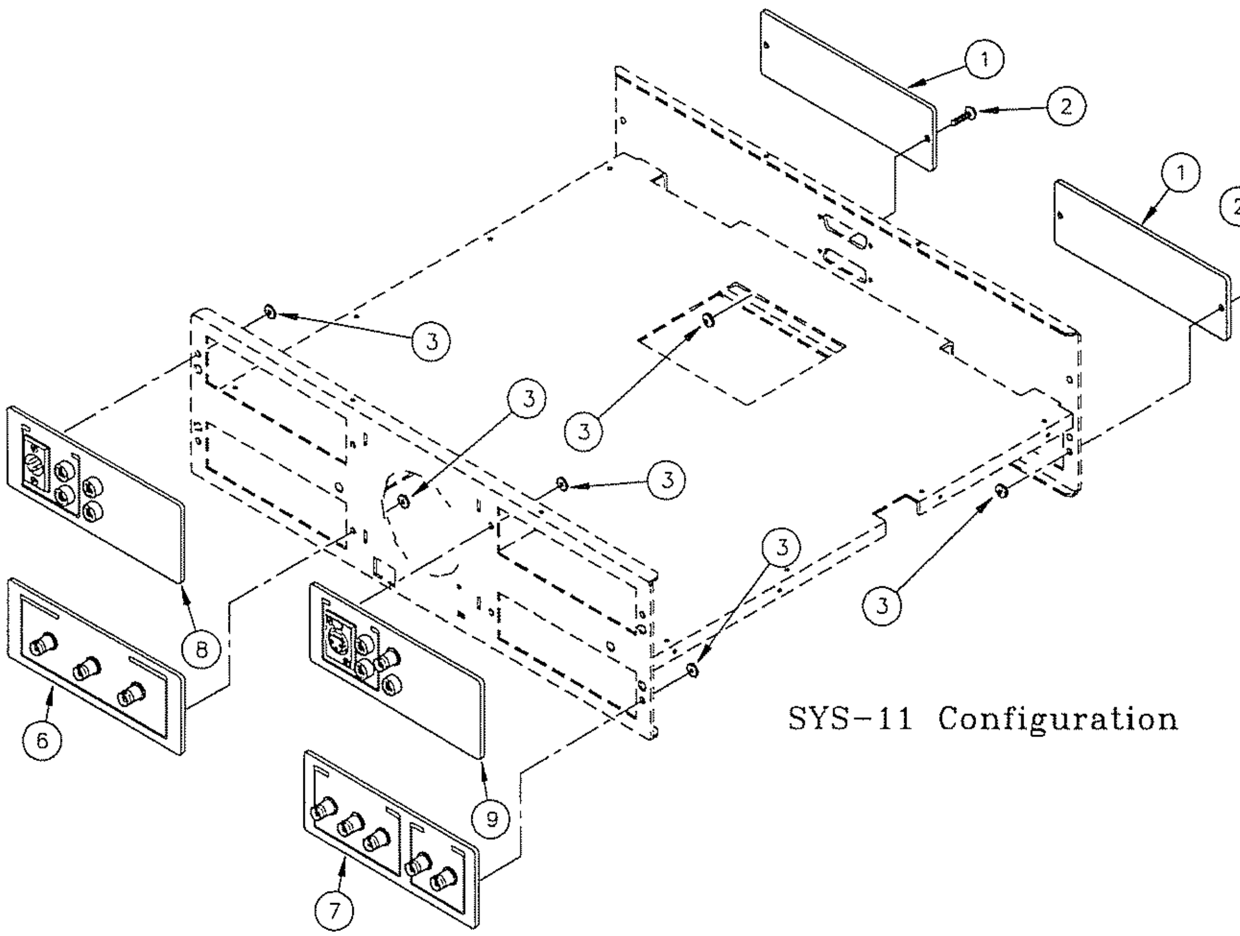
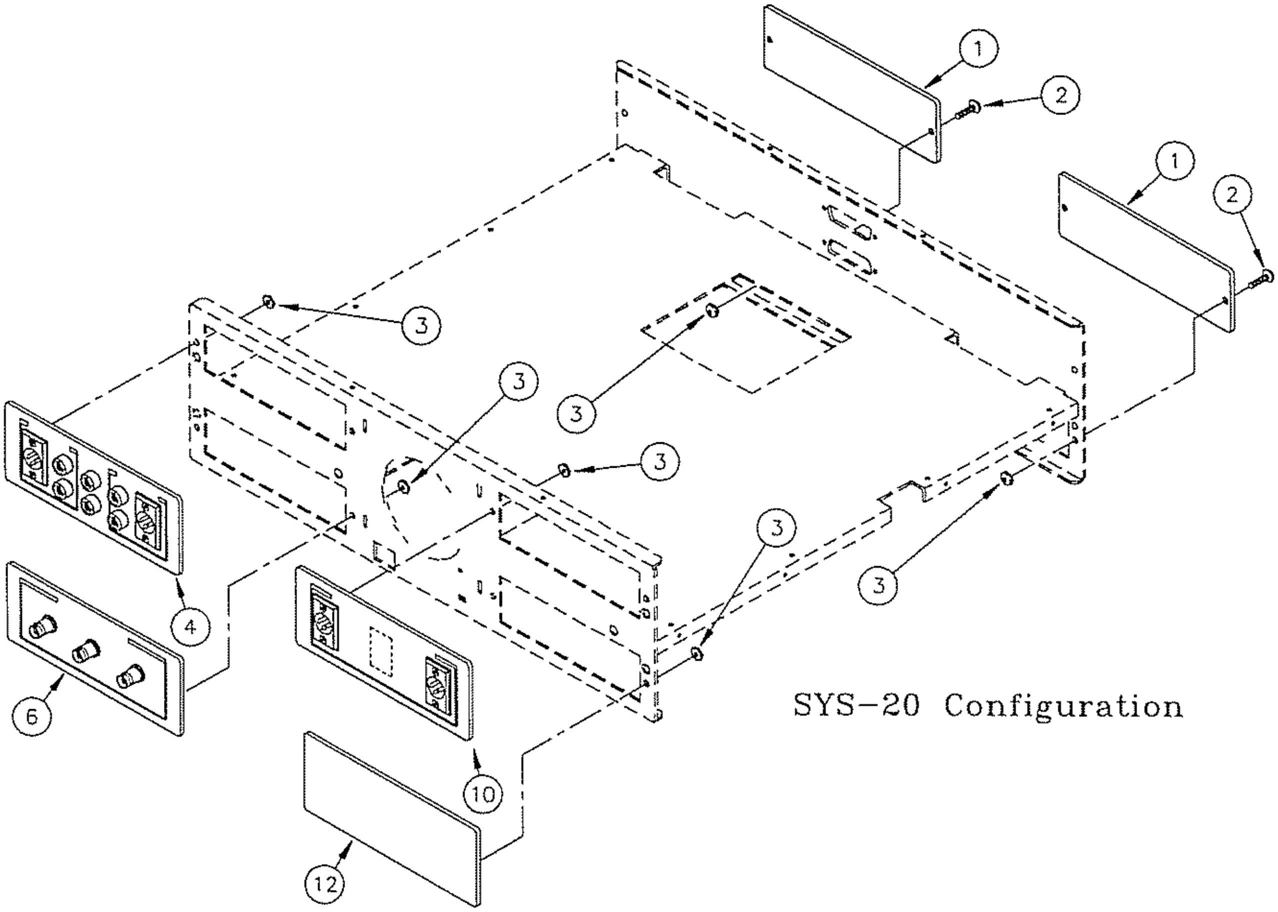


Figure 6.2a FRONT AND REAR PANEL ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.2b

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7140.0002	Rear Cover Panel
-2	5114.4116	Screw, MC TRS PH ZN #8-32 x 1/2
-3	5224.0001	Nut, KEP #8-32
-4	9XMB.2000	GEN Output Panel
-5	9XFM.2000	ANLR Input Panel
-6	9BNC.3010	GEN Aux Panel
-7	9BNC.5000	ANLR Aux Panel
-8	9XMB.1000	SYS-11 GEN Panel
-9	9XFB.1000	SYS-11 ANLR Panel
-10	9XMS.2000	GEN MON Panel for SYS-20
	9XMS.3000	GEN MON Panel for SYS-20 with option DSP
-11	9XFS.2000	GEN MON Panel for SYS-02
	9XFS.3000	GEN MON Panel for SYS-202 and SYS-302
-12	7131.0000	Blank Front Panel
-13	9BNC.6000	SYS-2xx Aux Panel
-14	9DDR.3000	SYS-3xx Rear Panel
-15	9DDF.3010	SYS-3xx Serial I/O Panel, with optical
-16	9DDF.3000	SYS-3xx Serial I/O Panel, w/o optical



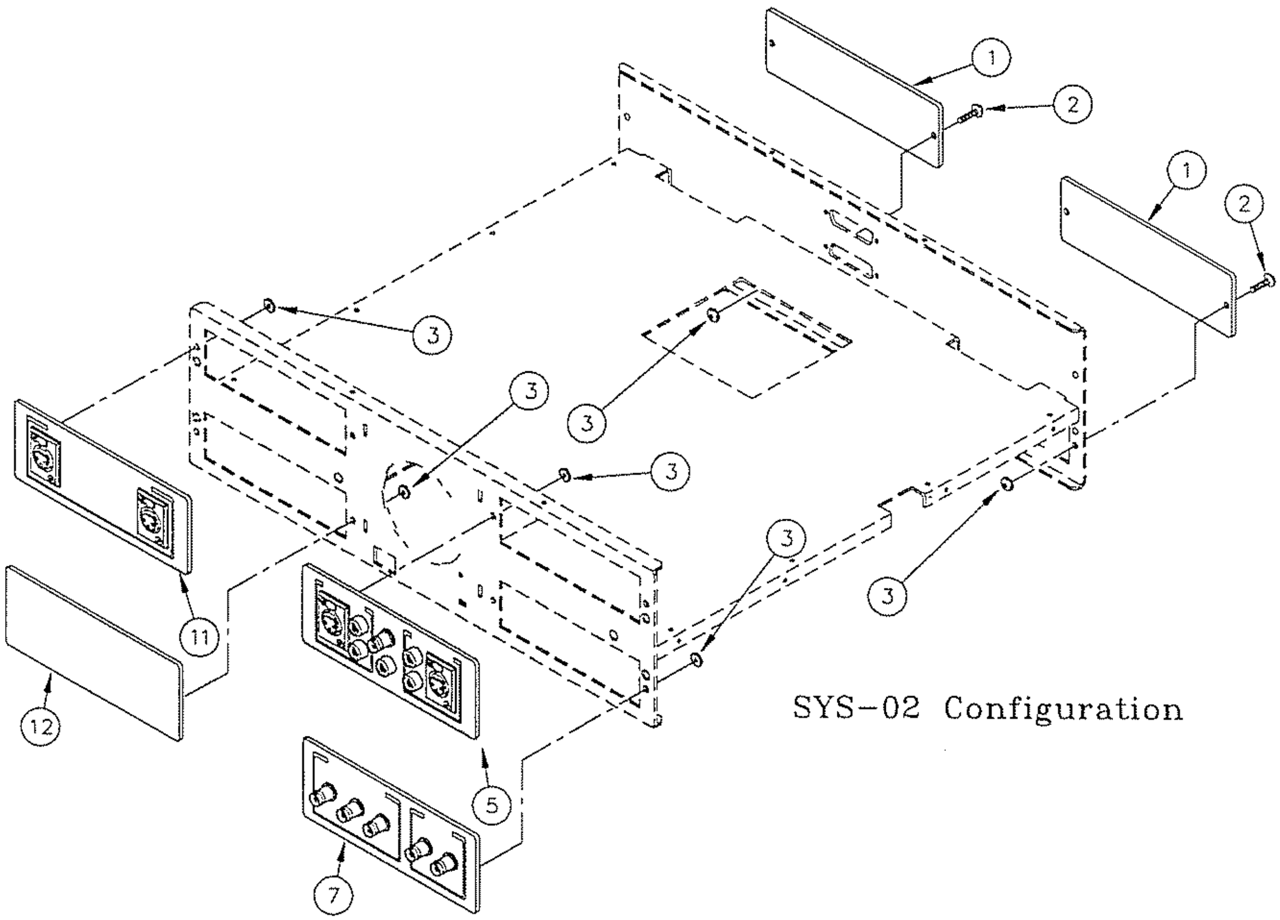
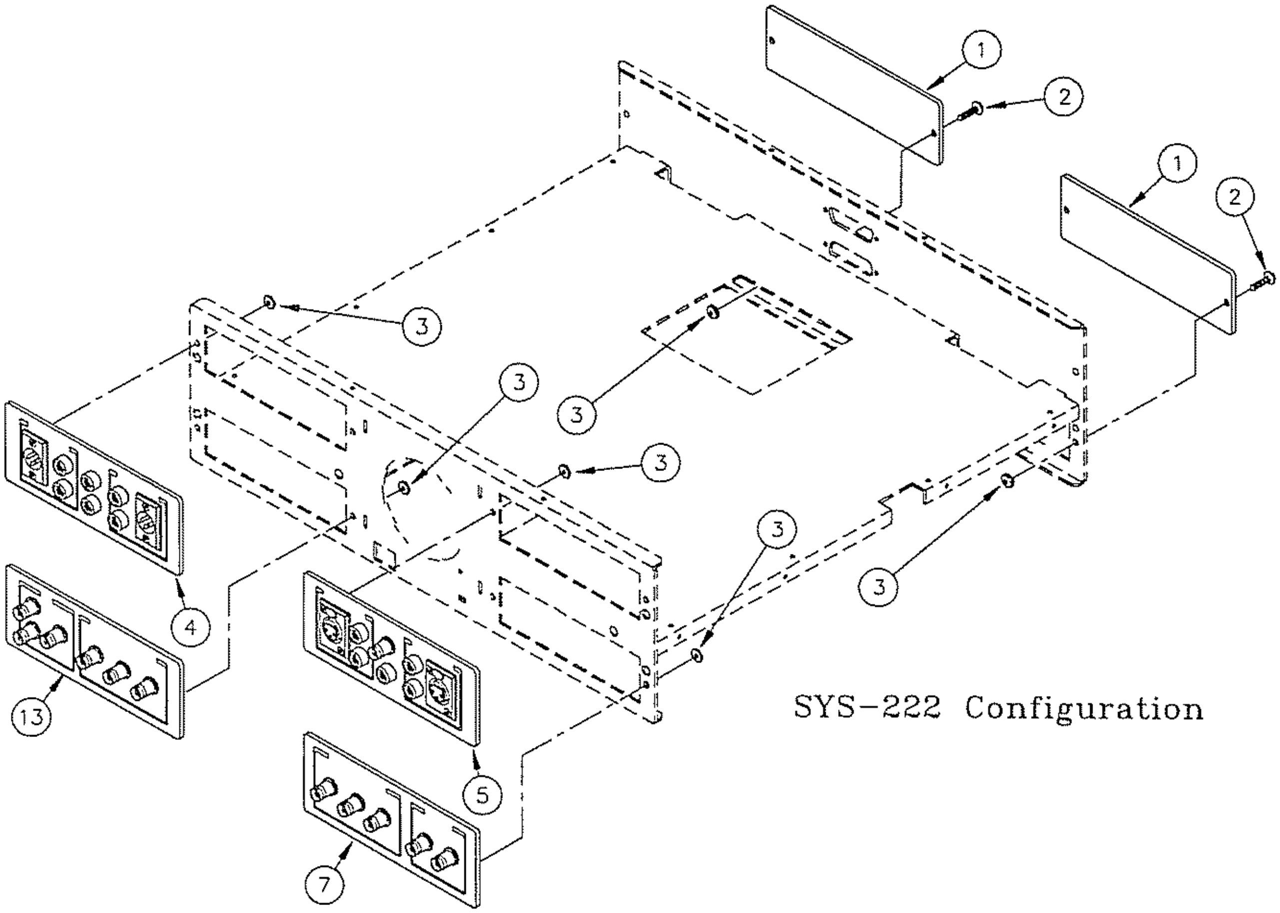


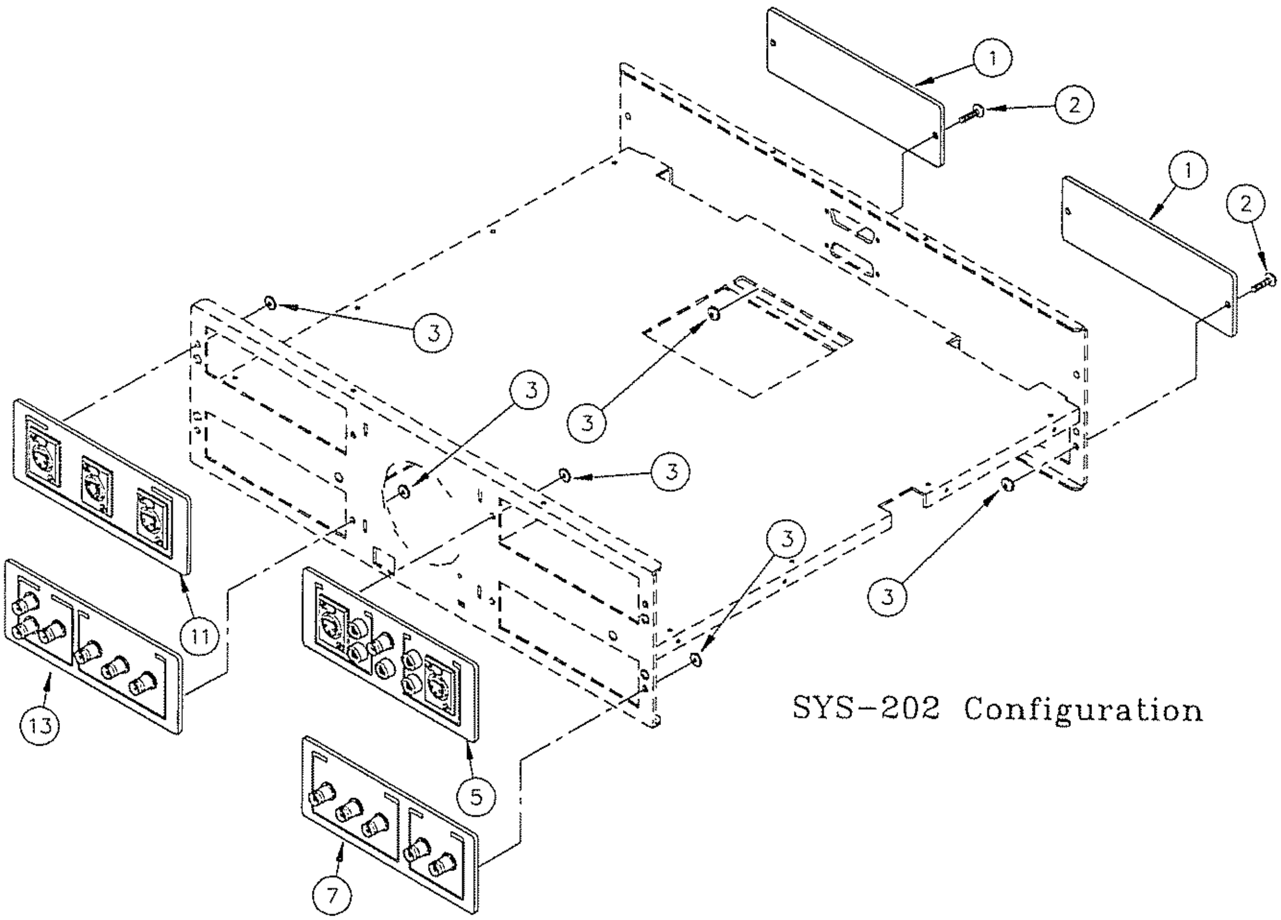
Figure 6.2b FRONT AND REAR PANEL ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.2c

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7140.0002	Rear Cover Panel
-2	5114.4116	Screw, MC TRS PH ZN #8-32 x 1/2
-3	5224.0001	Nut, KEP #8-32
-4	9XMB.2000	GEN Output Panel
-5	9XFM.2000	ANLR Input Panel
-6	9BNC.3010	GEN Aux Panel
-7	9BNC.5000	ANLR Aux Panel
-8	9XMB.1000	SYS-11 GEN Panel
-9	9XFB.1000	SYS-11 ANLR Panel
-10	9XMS.2000	GEN MON Panel for SYS-20
	9XMS.3000	GEN MON Panel for SYS-20 with option DSP
-11	9XFS.2000	GEN MON Panel for SYS-02
	9XFS.3000	GEN MON Panel for SYS-202 and SYS-302
-12	7131.0000	Blank Front Panel
-13	9BNC.6000	SYS-2xx Aux Panel
-14	9DDR.3000	SYS-3xx Rear Panel
-15	9DDF.3010	SYS-3xx Serial I/O Panel, with optical
-16	9DDF.3000	SYS-3xx Serial I/O Panel, w/o optical



SYS-222 Configuration

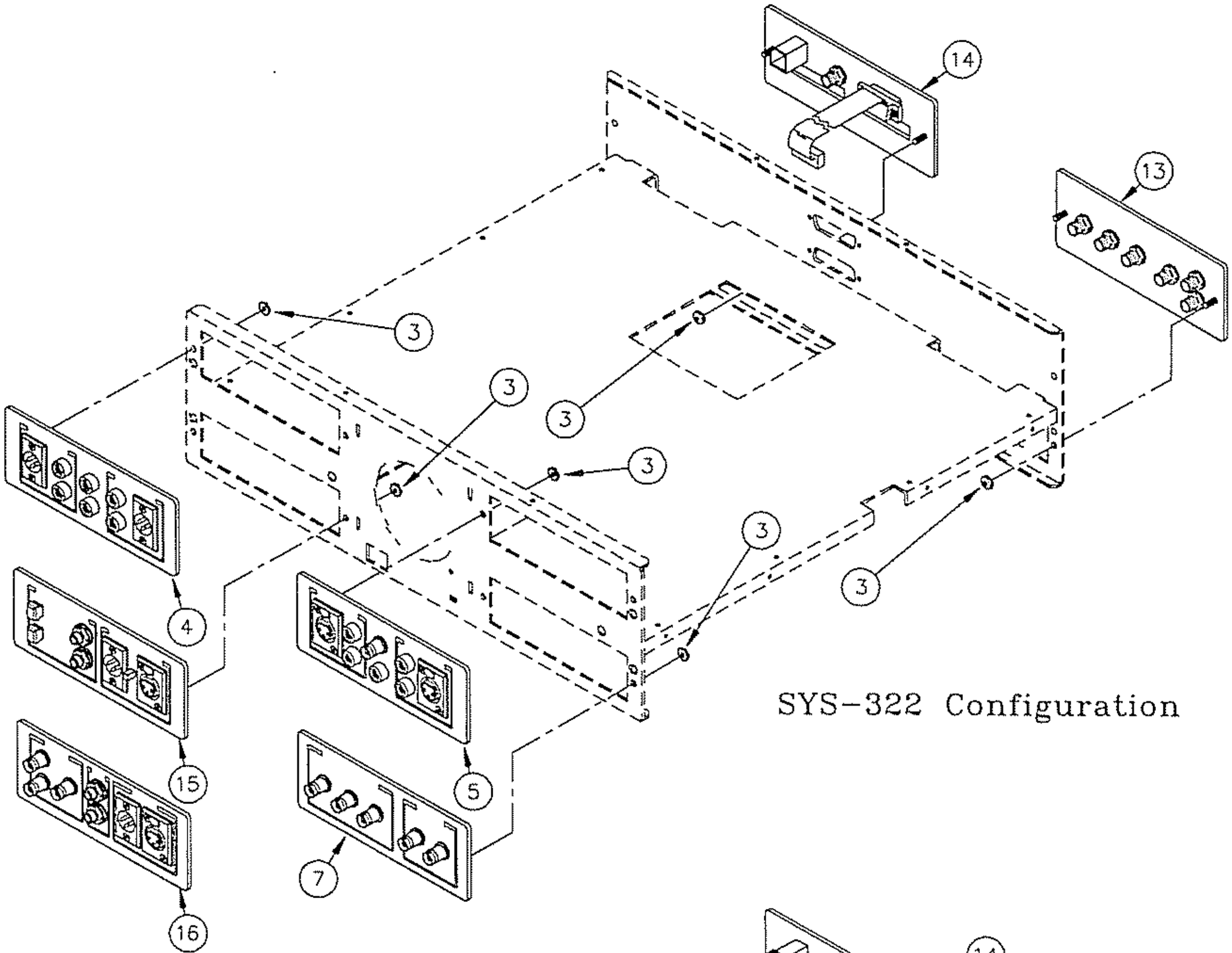


SYS-202 Configuration

Figure 6.2c FRONT AND REAR PANEL ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.2d

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7140.0002	Rear Cover Panel
-2	5114.4116	Screw, MC TRS PH ZN #8-32 x 1/2
-3	5224.0001	Nut, KEP #8-32
-4	9XMB.2000	GEN Output Panel
-5	9XFM.2000	ANLR Input Panel
-6	9BNC.3010	GEN Aux Panel
-7	9BNC.5000	ANLR Aux Panel
-8	9XMB.1000	SYS-11 GEN Panel
-9	9XFB.1000	SYS-11 ANLR Panel
-10	9XMS.2000	GEN MON Panel for SYS-20
	9XMS.3000	GEN MON Panel for SYS-20 with option DSP
-11	9XFS.2000	GEN MON Panel for SYS-02
	9XFS.3000	GEN MON Panel for SYS-202 and SYS-302
-12	7131.0000	Blank Front Panel
-13	9BNC.6000	SYS-2xx Aux Panel
-14	9DDR.3000	SYS-3xx Rear Panel
-15	9DDF.3010	SYS-3xx Serial I/O Panel, with optical
-16	9DDF.3000	SYS-3xx Serial I/O Panel, w/o optical



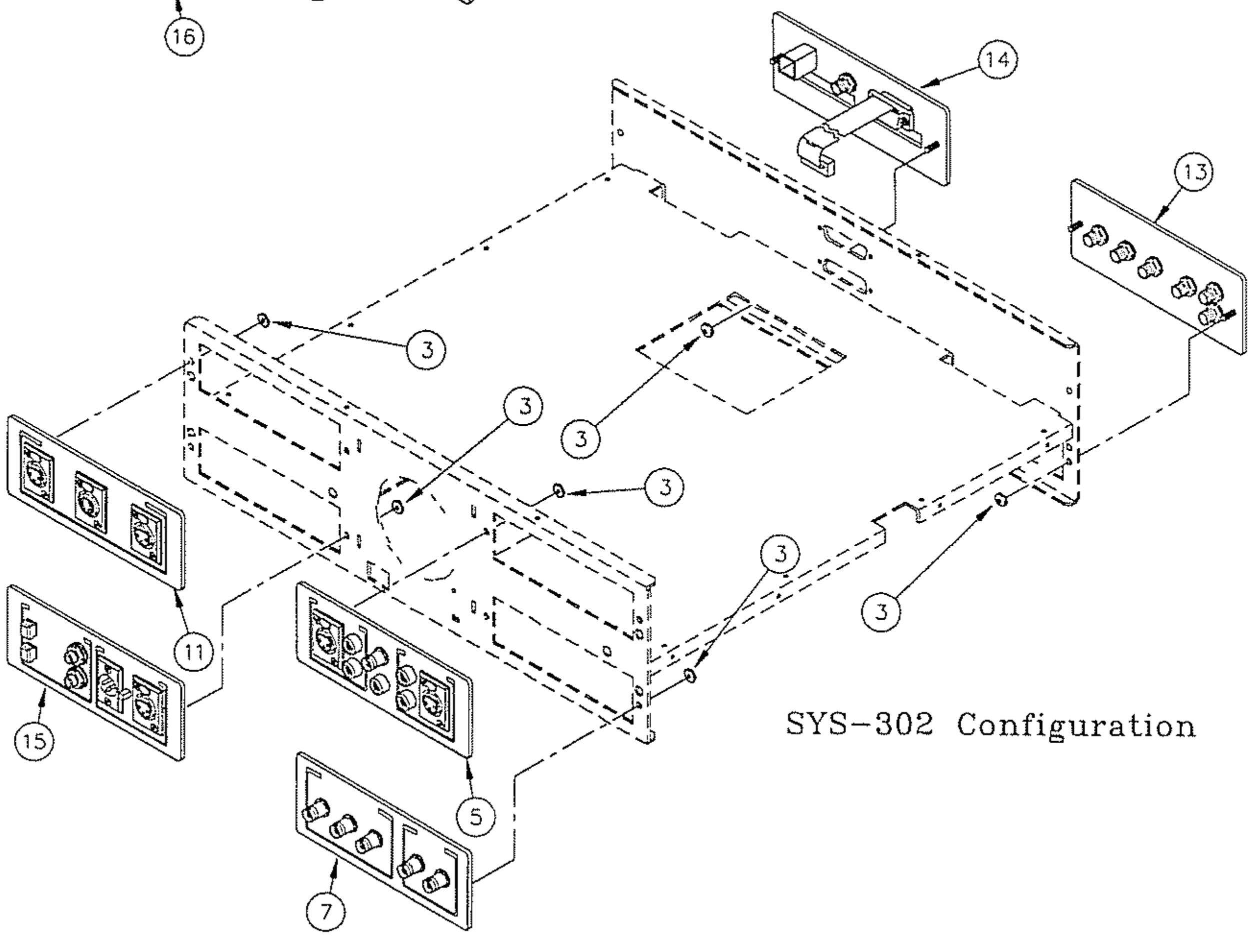


Figure 6.2d FRONT AND REAR PANEL ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.3a

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	9GEN.1000	GEN-1, Generator Module Assy
-2	5112.7110	Screw, MC SEM PH ZN #4-40 x 5/16
-3	5532.1212	Standoff, HEX M/F 1/4 x 3/8
-4	5532.1240	Standoff, HEX M/F 1/4 x 1.25
-5	5522.1212	Standoff, HEX Thrd 1/4 x 3/8
-6	9MFI.1000	MFI-1 Interface Assy
	9MFI.2000	MFI-2 Interface Assy
-7	5532.1106.1	Standoff, HEX M/F Jack Screw
-8	9LVF.2000	LVF-2 Analyzer Module Assy
		NOTE: Units serial number 10001-10299 contain the LVF-1 version. Please contact Audio Precision before ordering replacement.
-9	9DIS.2000	DIS-2 Distortion Measurement Module Assy
		NOTE: Units serial number 10001-10299 contain the DIS-1 version. Please contact Audio Precision before ordering replacement.
-10	9PSA.1000	PSA-1 Power Supply board
	9PSA.2000	PSA-2 Power Supply board
-11	9DSP.1000	DSP-1 dsp Module Assy
	9DSP.2000	DSP-2 dsp Module Assy
-12	9MFI.3000	MFI-3 Interface Assy
	9MFI.4000	MFI-4 Interface Assy
	9MFI.5000	MFI-5 Interface Assy
-13	9OMI.300G	OMI-3 with GPIB Interface board
-14	5532.2208	Standoff, RND M/F 1/4 x 1/4
-15	5532.1214	Standoff, HEX M/F 1/4 x 7/16
-16	9MFI.3000	MFI-3 Interface Assy
	9MFI.4000	MFI-4 Interface Assy
-17	9OMI.300S	OMI-3 with RS-232 Interface board
-18	5532.1224	Standoff, HEX M/F 1/4 x 3/4
-19	4225.0024	Shield (included with GPIB Connector)

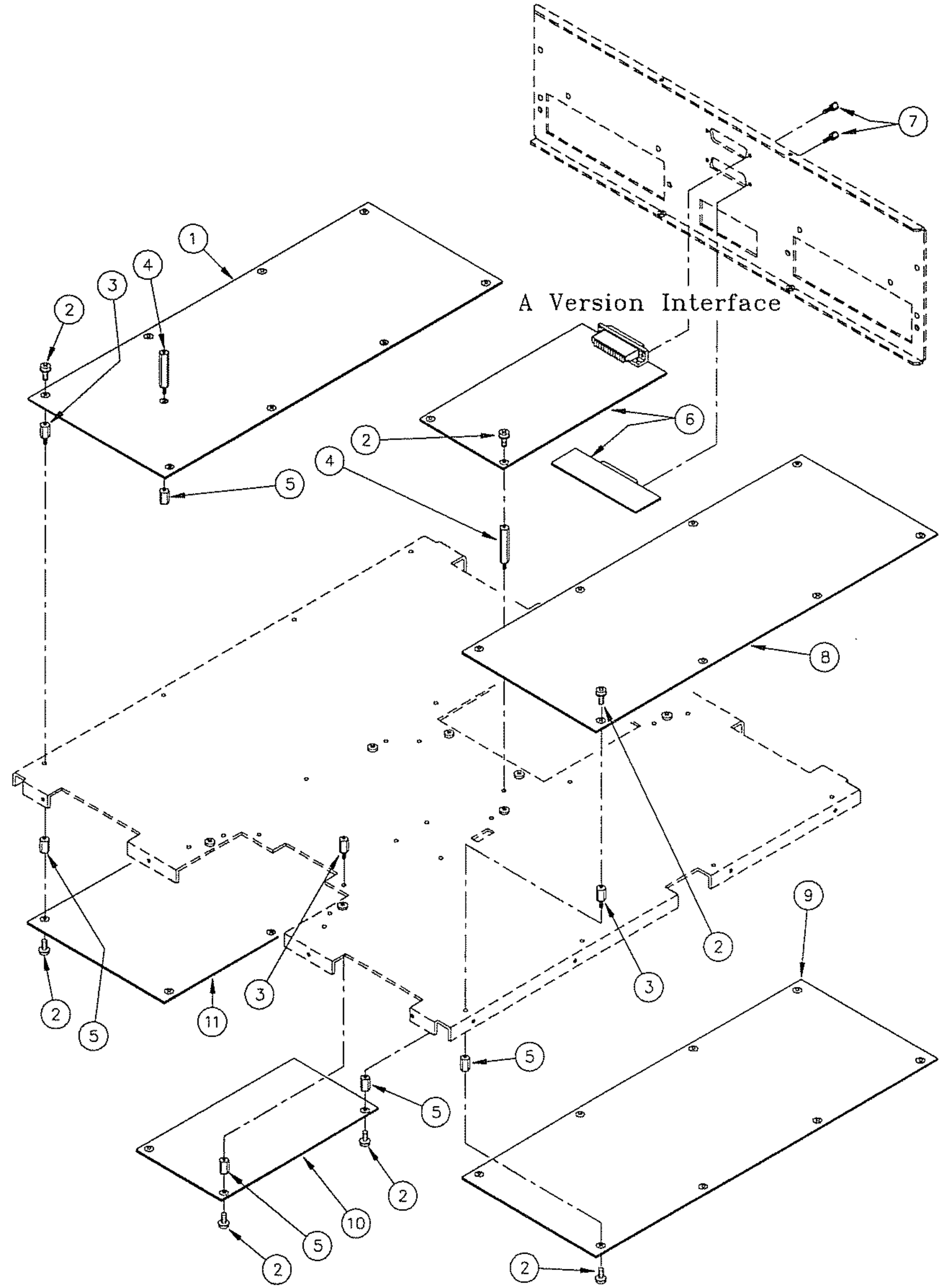
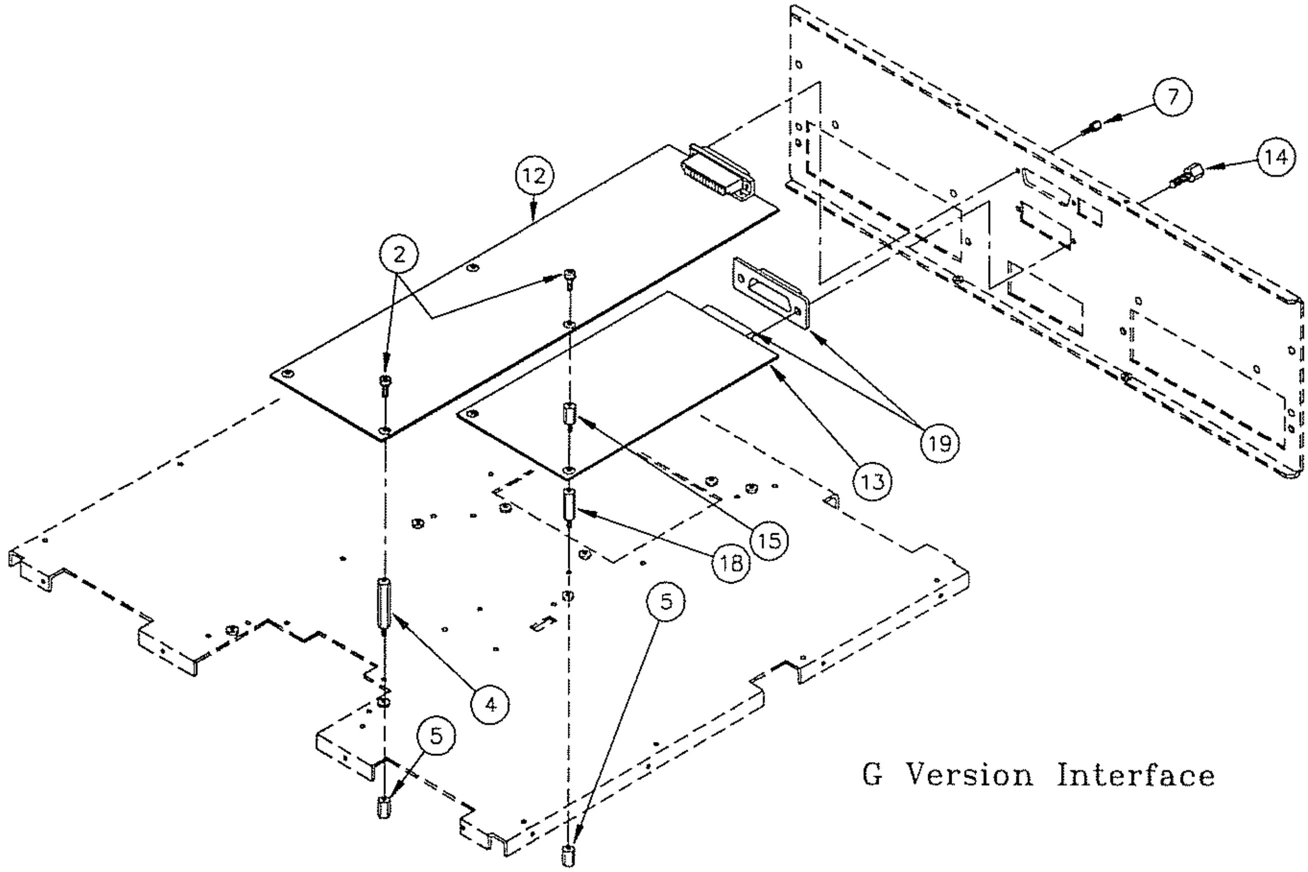


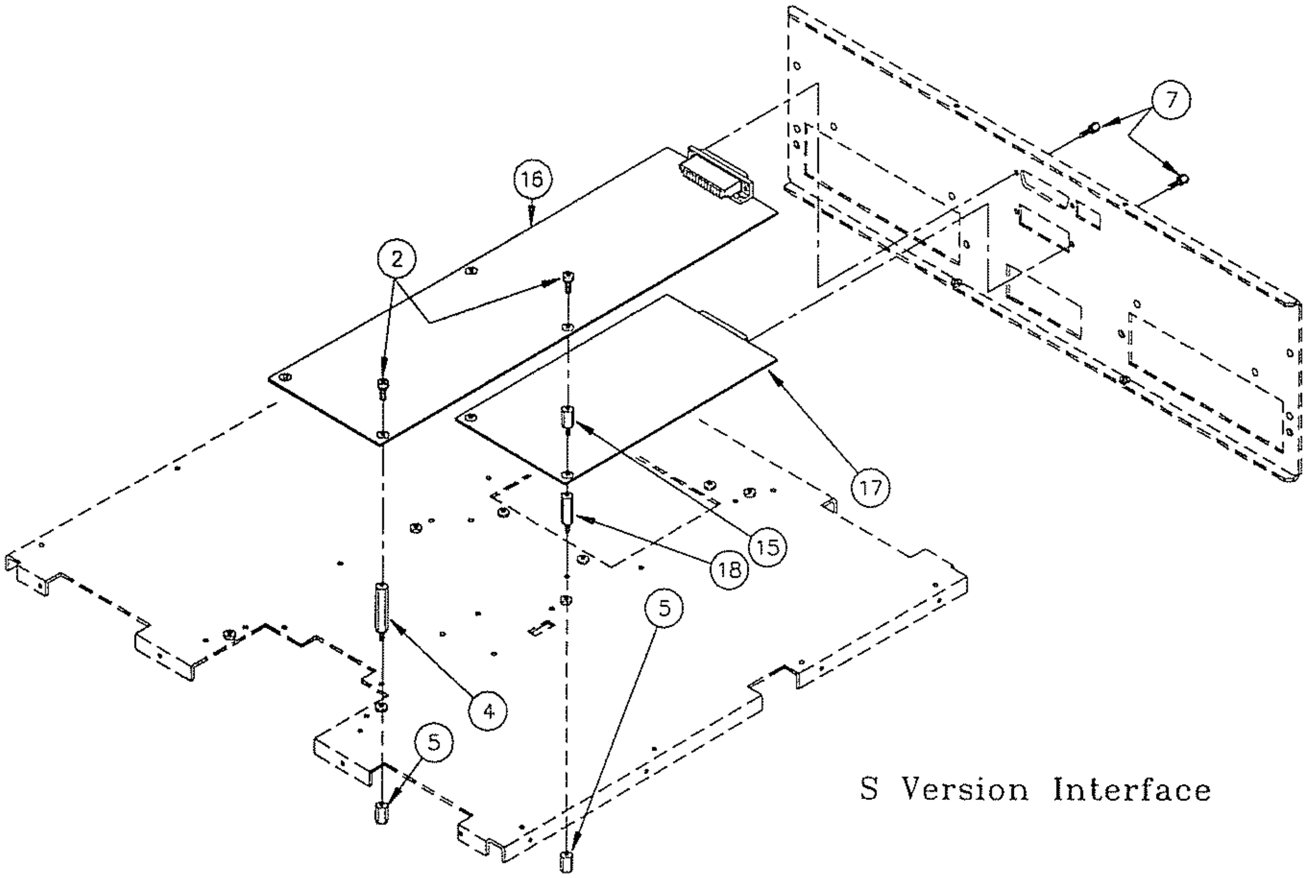
Figure 6.3a MAIN MODULE CIRCUIT BOARD ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.3b

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	9GEN.1000	GEN-1, Generator Module Assy
-2	5112.7110	Screw, MC SEM PH ZN #4-40 x 5/16
-3	5532.1212	Standoff, HEX M/F 1/4 x 3/8
-4	5532.1240	Standoff, HEX M/F 1/4 x 1.25
-5	5522.1212	Standoff, HEX Thrd 1/4 x 3/8
-6	9MFI.1000	MFI-1 Interface Assy
	9MFI.2000	MFI-2 Interface Assy
-7	5532.1106.1	Standoff, HEX M/F Jack Screw
-8	9LVF.2000	LVF-2 Analyzer Module Assy
		NOTE: Units serial number 10001-10299 contain the LVF-1 version. Please contact Audio Precision before ordering replacement.
-9	9DIS.2000	DIS-2 Distortion Measurement Module Assy
		NOTE: Units serial number 10001-10299 contain the DIS-1 version. Please contact Audio Precision before ordering replacement.
-10	9PSA.1000	PSA-1 Power Supply board
	9PSA.2000	PSA-2 Power Supply board
-11	9DSP.1000	DSP-1 dsp Module Assy
	9DSP.2000	DSP-2 dsp Module Assy
-12	9MFI.3000	MFI-3 Interface Assy
	9MFI.4000	MFI-4 Interface Assy
	9MFI.5000	MFI-5 Interface Assy
-13	9OMI.300G	OMI-3 with GPIB Interface board
-14	5532.2208	Standoff, RND M/F 1/4 x 1/4
-15	5532.1214	Standoff, HEX M/F 1/4 x 7/16
-16	9MFI.3000	MFI-3 Interface Assy
	9MFI.4000	MFI-4 Interface Assy
-17	9OMI.300S	OMI-3 with RS-232 Interface board
-18	5532.1224	Standoff, HEX M/F 1/4 x 3/4
-19	4225.0024	Shield (included with GPIB Connector)



G Version Interface



S Version Interface

Figure 6.3b INTERFACE BOARD ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.4

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	9IMG.1000	IMG-1 IMD Generator board (option)
-2	5112.7108	Screw, MC SEM PH ZN #4-40 x 1/4
-3	5532.1214	Standoff, HEX M/F 1/4 x 7/16
-4	9BUR.1000	BUR-1 Burst Gen board (option)
-5	5532.1224	Standoff, HEX M/F 1/4 x 3/4
-6	5532.1240	Standoff, HEX M/F 1/4 x 1.25
-7	---------	Option filters
-8	9W&F.1000	W&F-1 Wow and Flutter anlr board (option)
-9	9PHA.1000	PHA-2 Dual Input/Phasemeter board
		NOTE: Units serial number 10001-10299 contain the PHA-1 version. Please contact Audio Precision before ordering replacement.
-10	7161.0002	Shield, phasemeter
-11	9IMA.1000	IMA-1 IMD Analyzer board (option)
-12	5522.1212	Standoff, HEX Thrd 1/4 x 3/8
-13	9DIO.1000	DIO-1 Digital I/O board (SYS-3xx only)
	9DIO.2000	DIO-2 Digital I/O board (SYS-3xx only)
-14	9DUA.1000	DUA-1 Dual output board
-15	5532.1212	Standoff, HEX M/F 1/4 x 3/8

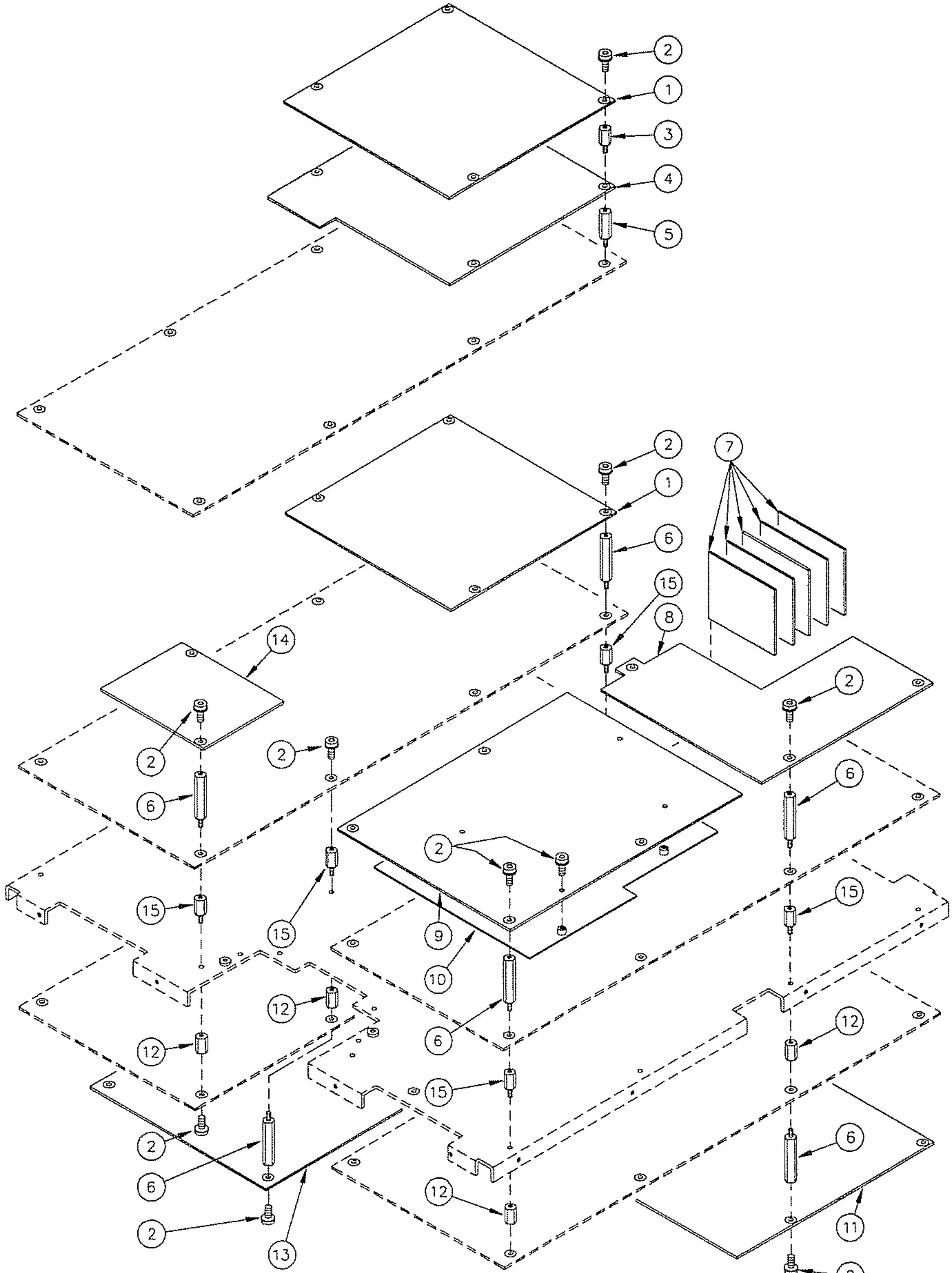


Figure 6.4 CIRCUIT BOARD ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.5

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7160.0011	Rack Ear
-2	5113.1110.1	Screw, MC FLT PH GRY #6-32 x 5/16
-3	7150.0011	Cover, Top & Bottom
-4	5113.1108.1	Screw, MC FLT PH GRY #6-32 x 1/4
-5	5132.1108	Screw, SN FLT H ZN #4-40 x 3/8
-6	4253.0011	XLR Conn, male 3-pin, PC 90 for SWR-122F
	4253.0012	XLR Conn, female 3-pin, PC 90 for SWR-122M
-7	4253.0011	XLR Conn, male 3-pin, PC 90 for SWR-122M
	4253.0012	XLR Conn, female 3-pin, PC 90 for SWR-122F
	4253.0021	XLR Conn, male 5-pin, PC 90 for SWR-122P
-8	4225.0125	Plug, D-Sub, PC 90 25-pin
-9	5532.1106.1	Standoff, HEX M/F Jack Screw
-10	4225.0025	Jack, D-Sub, PC 90 25-pin
-11	5112.1112.4	Screw MC FLT PH SS #4-40 x 3/8
-12	4262.0001	Fuse Holder PC Universal
-13	5112.7110	Screw, MC SEM PH ZN #4-40 x 5/16
-14	7110.0011	Chassis Wrap, Switcher
-15	7161.0011	Shield
-16	4340.0001	Switch, Slide 120V-240V DPDT
-17	5222.0001	Nut, KEP #4-40
-18	5412.0001	Solder Lug #4
-19	4256.0001	Plug, PC mount 240V 3 Cond
-20	5620.0011	Insulator, Mica TO220
-21	3225.0032	Xstr NPN TO220 TIP32C
-22	5346.0002	Washer, shoulder
-23	9SWR.122F	SWR-122F ECB assy
	9SWR.122M	SWR-122M ECB assy
	9SWR.122P	SWR-122P ECB assy
	9SWR.122T	SWR-122T ECB assy
-24	5111.3106	Screw, MC PAN PH ZN #2-56 x 3/16
-25	7130.0012	Front Sub Panel for SWR-122F and SWR-122M
	7130.0014	Front Sub Panel for SWR-122P and SWR-122T
-26	5112.1112.5	Screw, MC FLT PH BGE #4-40 x 3/8
-27	7130.0010	Front Panel for SWR-122F
	7130.0011	Front Panel for SWR-122M
	7130.0015	Front Panel for SWR-122P
	7130.0013	Front Panel for SWR-122T
-28	5132.1108	Screw, SM FLT PH ZN #4-40 x 1/4
-29	5640.0001	Tape, BLK, 1 Mil x .5
-30	5630.0001	Feet, BLK .5 x .5 x .25

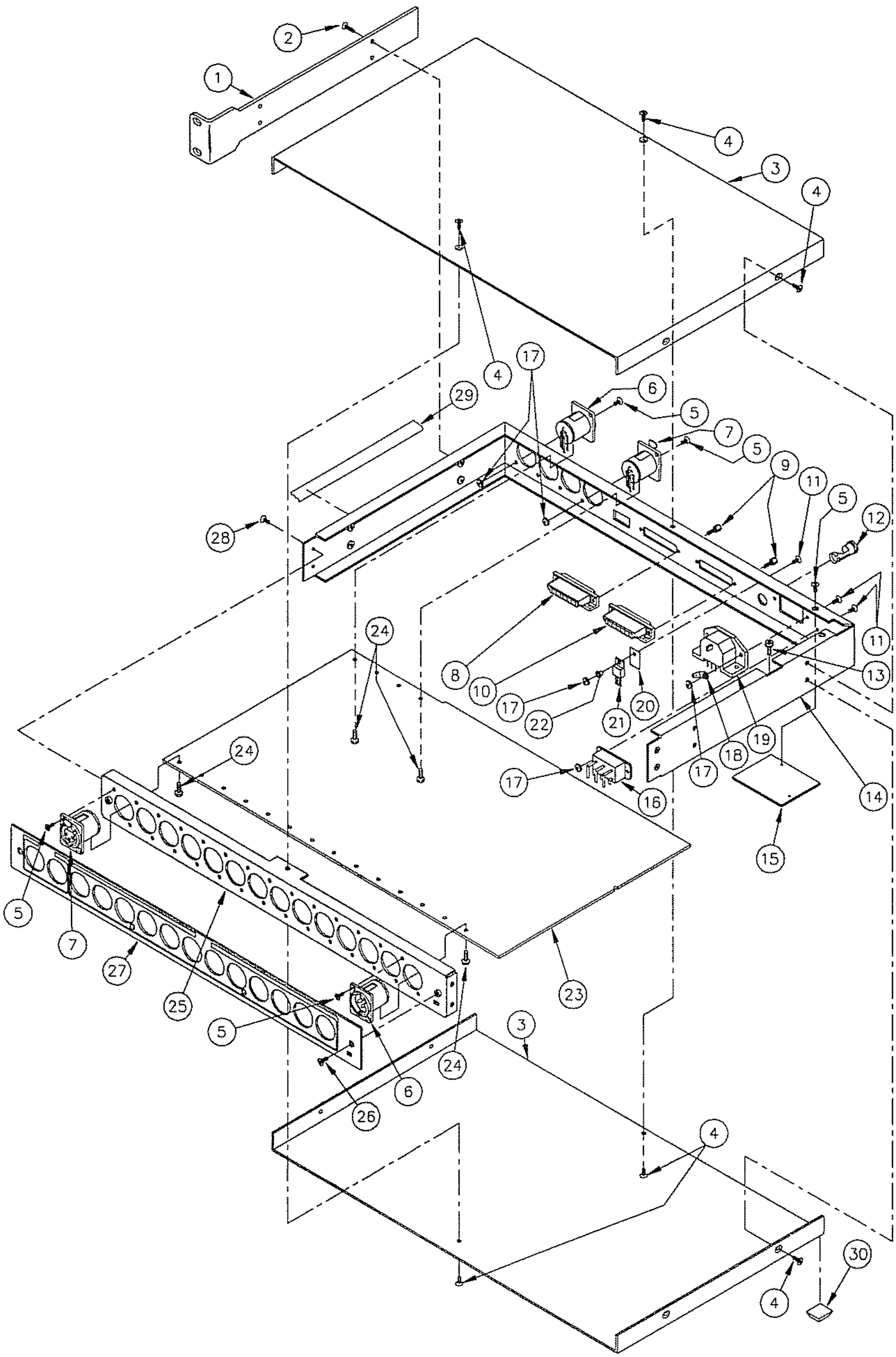


Figure 6.5 SWR-122 SWITCHER ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.6

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7160.0011	Rack Ear
-2	5113.1110	Screw, MC FLT PH BGE #6-32 x 5/16
-3	7150.0011	Cover, Top & Bottom
-4	5113.1110.1	Screw, MC FLT PH BGE #6-32 x 5/16
-5	4225.0009	Jack, D-Sub PC 90 9-Pin
-6	5532.1106.1	Standoff, HEX M/F Jack Screw
-7	4225.0015	Jack, D-Sub PC 90 15-Pin
-8	4225.0125	Plug, D-Sub PC 90 25-Pin
-9	4225.0025	Jack, D-Sub PC 90 25-Pin
-10	5112.1112.4	Screw, MC FLT PH SS #4-40 x 3/8
-11	4530.0001	Line Conn, V Sel, Fuse, RFI Filter
-12	7110.0021	Chassis Wrap, DCX
-13	7160.0011	Shield
-14	5413.0001	Lug, Solder #4
-15	5222.0001	Nut, KEP #4-40
-16	3430.2940.5	Volt Reg Pos 5.0V TO220 LM2940
-17	5132.3408	Screw, PL PAN SL #4-40 x 1/4
-18	7161.0003	Shield, DMM
-19	5522.1220	Standoff, HEX Thrd 1/4 x 5/16
-20	9DMM.1270	DMM Assy
-21	5532.1214	Standoff, HEX M/F 1/4 x 7/16
-22	5132.3408	Screw, PL PAN SL #4-40 x 1/4
-23	5112.7110	Screw, MC Sem PH ZN #4-40 x 5/16
-24	5670.0001	Shaft, Switch Extension 6"
-25	5720.0001	Knob, Push BLK
-26	5112.1112.5	Screw, MC FLT PH BGE #4-40 x 3/8
-27	4225.0001	Jack, Banana BLK, Insul, w/Hdwr
-28	5346.0001	Washer, Shoulder Nylon 1/4
-29	7310.0002	Bracket, Cover Support
-30	4225.0109	Plug, D-Sub PC 90 9-Pin
-31	7130.0021	Front Panel, DCX-127
-32	5640.0001	Tape, BLK, 1 Mil x .5
-33	5630.0001	Feet, BLK .5 x .5 x .25
-34	5132.1109	Screw, SM FLT PH ZN #4-40 x 1/4
-35	4255.0002	Jack, Banana Knurled, w/Hdwr
-36	5416.0001	Lug, Solder 1/4"

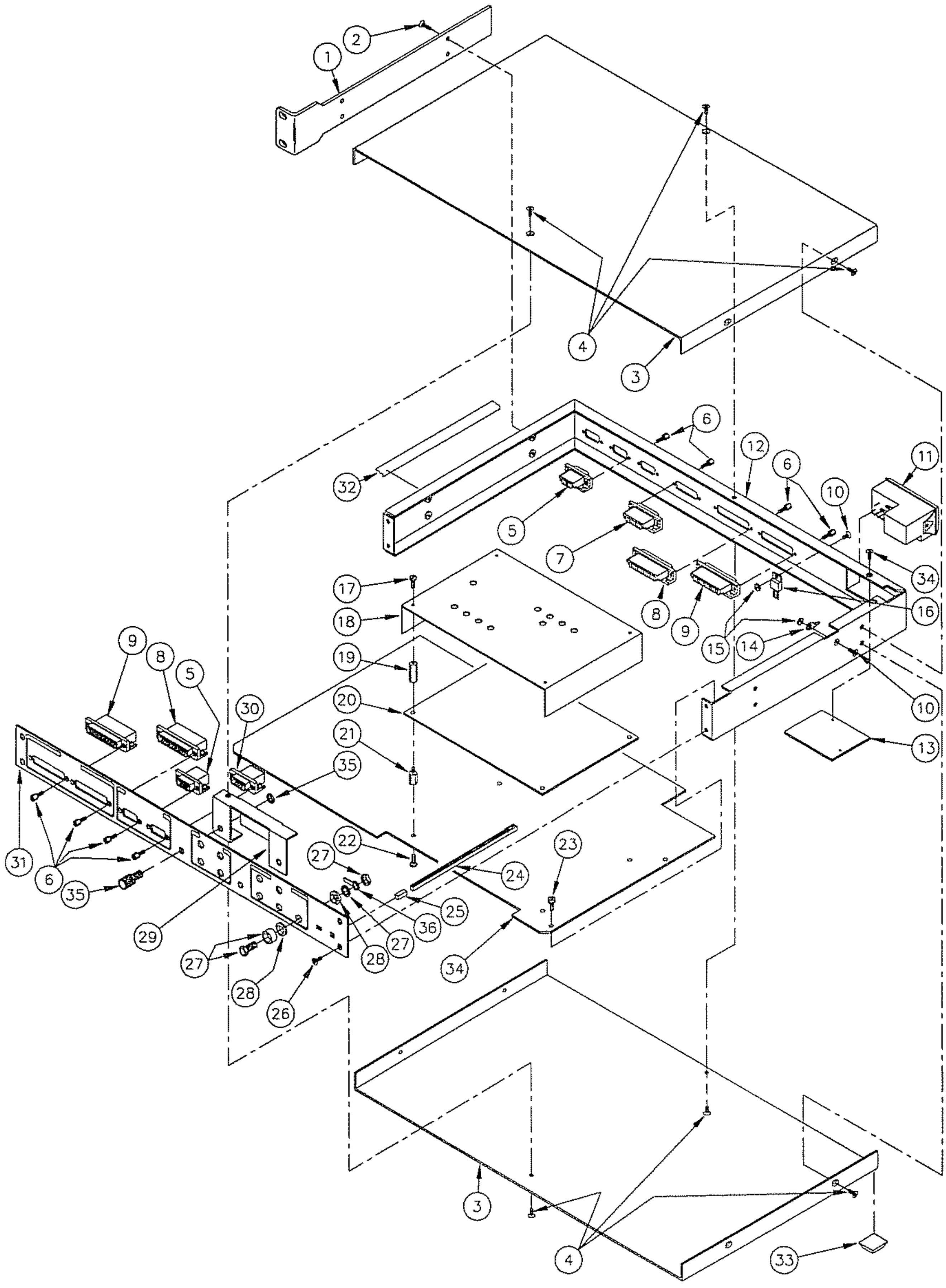


Figure 6.6 DCX-127 MULTIFUNCTION MODULE ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.7

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	7160.0011	Rack Ear
-2	5113.1110	Screw, MC FLT PH BGE #6-32 x 5/16
-3	7150.0011	Cover, Top & Bottom
-4	5113.1110.1	Screw, MC FLT PH BGE #6-32 x 5/16
-5	4225.0015	Jack, D-Sub PC 90 15-Pin
-6	5532.1106.1	Standoff, HEX M/F Jack Screw
-7	5112.1112.5	Screw, MC FLT, PH BGE #4-40 x 3/8
-8	4255.0002	Jack, Banana Knurled, w/Hdwr
-9	7310.0002	Bracket, Cover Support
-10	7130.0031	Front Panel, SIA-322
-11	9SIA.1000	SIA-322 ECB Assy
-12	5112.7110	Screw, MC Sem PH ZN #4-40 x 5/16
-13	4225.0115	Plug, D-Sub PC 90 15-Pin
-14	5640.0001	Tape, BLK, 1 Mil x .5
-15	7110.0041	Chassis Wrap, SIA-322
-16	4151.1234	Cable Assy, .05" RBN, 12", 34-Cond
-17	5630.0001	Feet, BLK .5 x .5 x .25

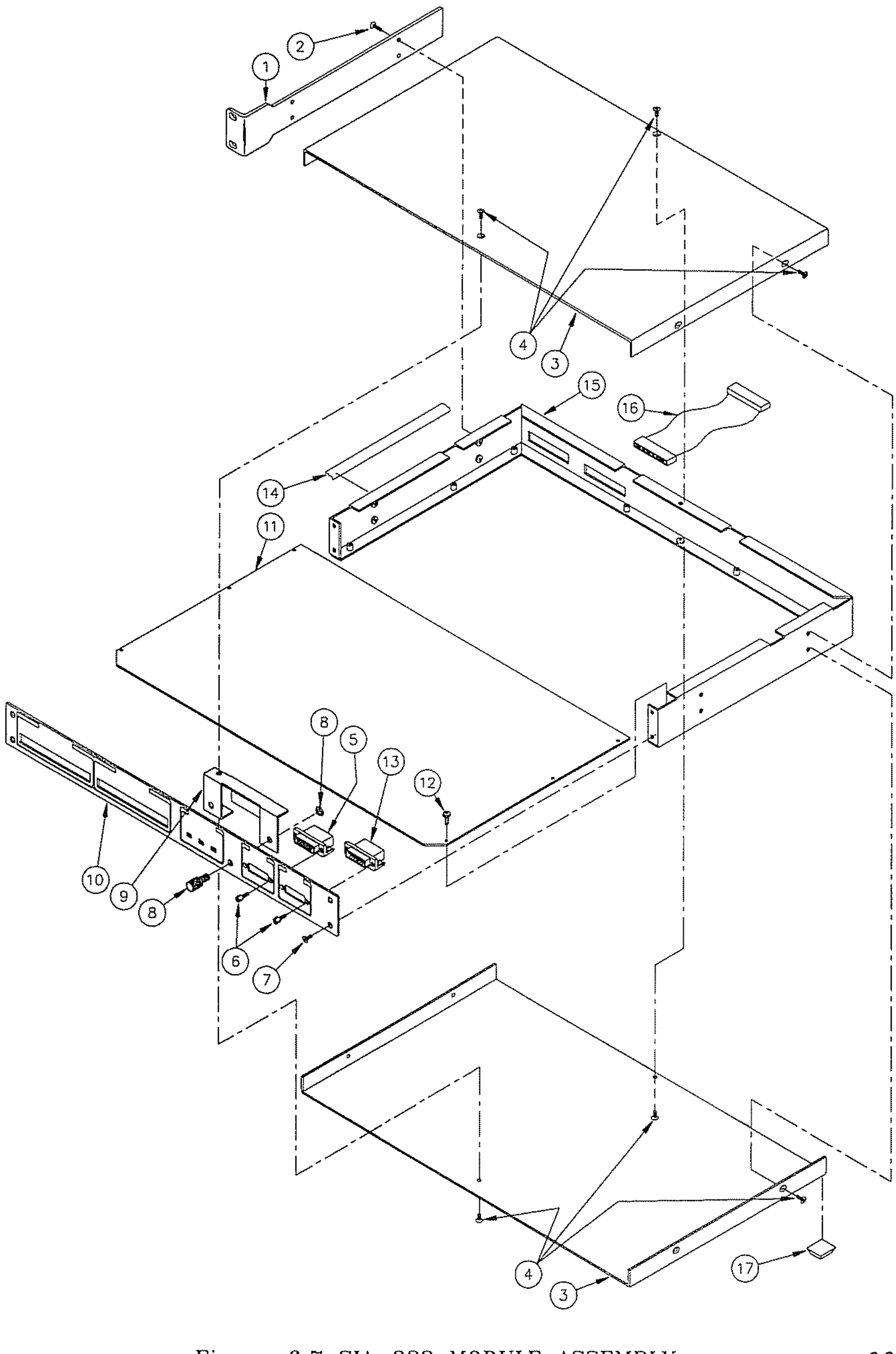


Figure 6.7 SIA-322 MODULE ASSEMBLY

Replaceable Mechanical Parts List for Figure 6.8

INDEX #	A-P NUMBER	ITEM DESCRIPTION
-1	4163.0001	Cord, Power, right angle, US
-2	4163.0002	Cord, Power, right angle, Euro
-3	4153.0001	Cable, Intf, 25 cond D-Sub, 2 meters
-4	4153.0002	Cable, Intf, 25 cond D-Sub, 0.5 meters

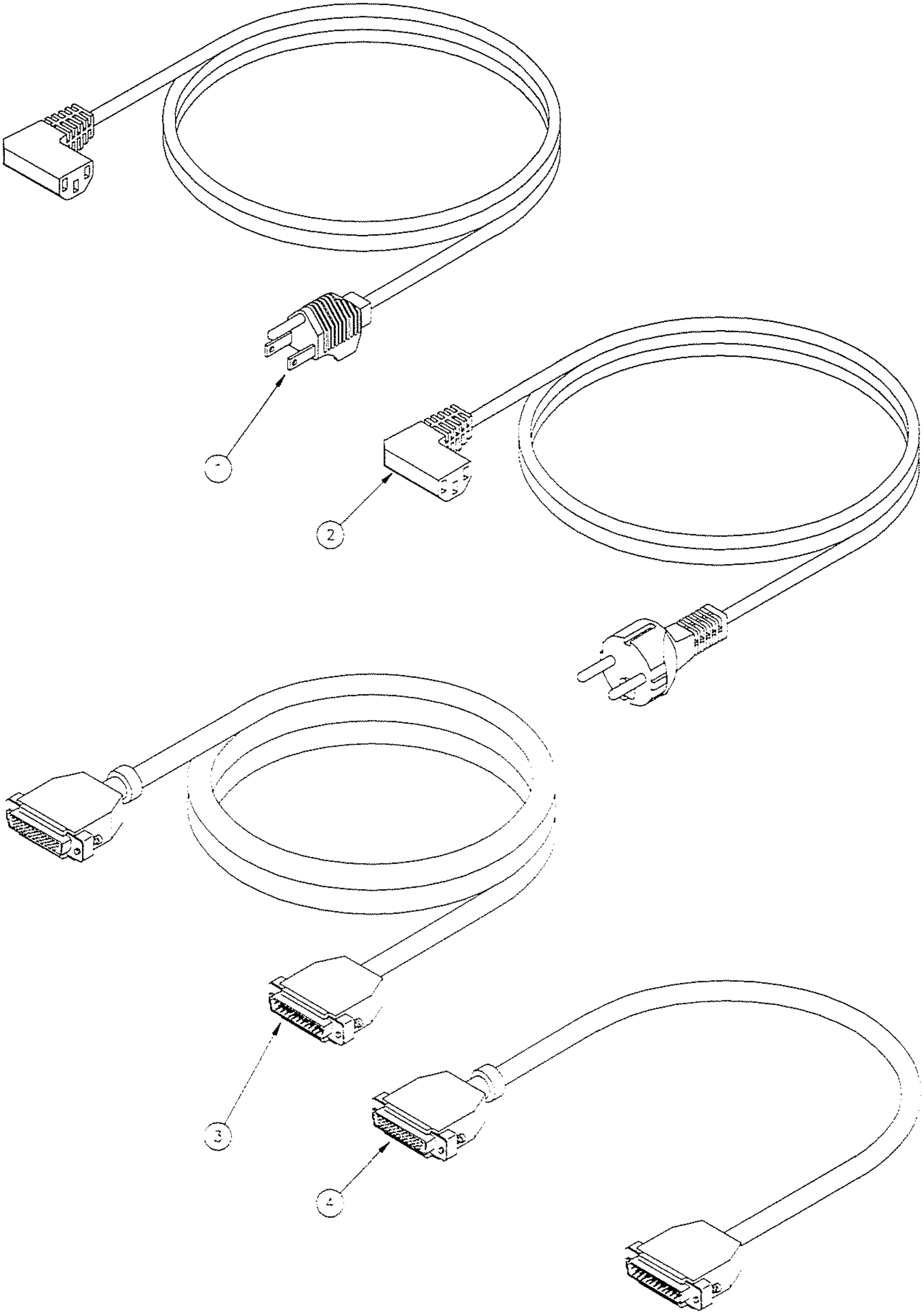


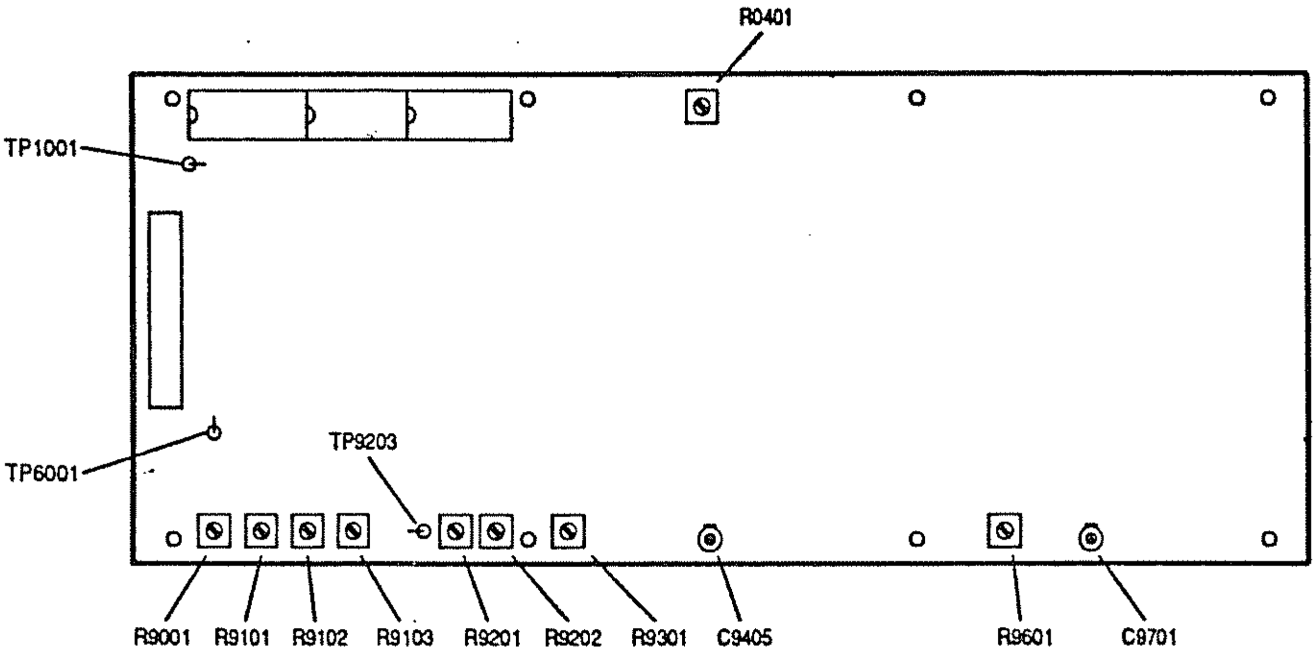
Figure 6.8 CABLES

SECTION 7
SUPPLEMENTAL DOCUMENTATION FOR SYSTEM ONE UNITS S/N 10001 - 10299

This supplement contains circuit descriptions, schematics, and electrical parts lists for the original production "-1" versions of the LVF, PHA, and DIS modules. Only System One units with serial numbers 10001-10299 (manufactured prior to December of 1986) contain the LVF-1, PHA-1, and DIS-1 modules. The "-2" versions of these modules were introduced in January 1977 to add a secondary signal path for simultaneous two-channel amplitude and crosstalk measurements. The "-1" and "-2" versions are not compatible with each other. All three modules must be the same version for proper operation.

Audio Precision reserves the right to make changes without prior notice. If a component value differs from that shown on the schematics use the value of the existing component for replacement purposes, or contact Audio Precision.

LVF-1 ANALYZER MAIN MODULE
(S/N 10001-10299 ONLY)



LVF-1, ANALYZER MODULE

The LVF-1 module contains the Channel-A input stage, bandwidth limiting filters, option filter sockets, "Reading" meter with selectable detectors, and frequency counter. The ranging circuits, voltmeter readings, and frequency counter are controlled by a 6805 microprocessor.

Interface Logic <1>

The data bus from the host computer enters via the 40-pin cable connector and is buffered by U101. After buffering the data bus is designated the "D" bus. The data bus of the 6805 microprocessor is designated the "C" bus to distinguish it from the host data bus. Address information also enters via the 40-pin cable connector and drives the appropriate decoding circuits. The address lines from the host are labeled "A" and the 6805 address lines are labeled "B".

The D bus drives the data latches on the board which receive settings information for filters, detectors, and input configuration. The D bus is also connected to a dual port RAM constructed by eight 4-bit-by-4 register files, U111, U211, U311, U411, U112, U212, U312, U412. These contain four 4-bit latches and address decoding logic so that the inputs of the four latches may be written to independently of the reading of the outputs at the other side. Inputs are labeled "xD", outputs are labeled "xQ". The RAM is allocated as follows:

TABLE LVF1.1
DUAL PORT RAM ALLOCATION

IC#	ADDRESS	FUNCTION
111, 212	0 - 3	range information to host
211, 312	4 - 7	frequency reading
311, 412	8 - 11	measure and phase readings
411	12 - 15	readings counters
112	0 - 3	reading rate & range info to 6805

The module address, normally set to 0, is decoded by a 4-bit comparator U601. When a match is found the output goes high, driving the output of Q4101 low and signaling the host that the board is present. The output of U601 also drives U221, a dual 2-to-4 line decoder. The upper half decodes the read addresses of the dual port RAM (pins 9-12). The other half decodes the write addresses, one bank of four enables RAM U112 while another bank of four goes to U241 for further decoding. The first three outputs of U241A drive the settings latches. The fourth, labeled /INT, drives the 6805 interrupt line. Whenever this is strobed the processor will abandon its current task and begin a new reading cycle.

Power-on resets are latched by U181A so that correct range and reading rate information may be written to the dual port RAM before the 6805 begins its readings cycle. The reset state is cleared by the strobing of the /INT line.

U141 latches the input relay settings, A/B selection and phasemeter range from the host. Only six of the eight bits are latched. The remaining two are used to enable the input 600 Ohm or 150 Ohm termination resistors. These are latched in individual flip-flops so they may be reset by an input overload condition without affecting the other seven bits.

Microprocessor <2>

The 20 MHz master clock is divided down by U121 to provide both a 4 MHz clock to the 6805 and a 5 MHz clock to the frequency counter. The 6805 microprocessor contains onboard EPROM and RAM and does not use the external pins for address or data information. All of the pins are latched and are used only for accessing peripheral ICs for reading or writing data. The eight lines on pins 12 through 19 are used as a bidirectional data bus and are labeled C0 through C7. Pins 20 through 24 are used as an address bus and are labeled B0 through B4. Read and write strobes appear on pins 26 and 25 respectively. They go low to read or write data on the C bus from or to the address selected by the B bus.

The 6805 executes a program loop which involves a sequence of steps which are always executed in the same order. When the processor finishes the steps in the loop it waits until it is time to begin the loop again. This timing is set by an internal counter which divides the master clock and interrupts the processor. This occurs at approximately 32.77 msec intervals, corresponding to the fastest reading rate of the voltmeters. This also sets the rate at which the ranging comparators are sampled and all other tasks are completed.

When the processor is busy performing operations it sets the CYCLE test point (pin 27) high. When it is waiting for another timer interrupt it sets the CYCLE test point low. Many of the tasks the 6805 must perform are not performed every time through the loop. For example, at reading rates slower than 32 rdg/sec the voltmeters and frequency counter will not be serviced every time through the loop. At 16 rdg/sec the voltmeters will be serviced once every two times through the loop. At 8 rdg/sec they will be handled every four times and at 4 rdg/sec it will be every eight times.

The frequency counter is slightly more complicated because it must also wait for zero crossings of the input signal before it may be serviced. At input frequencies above approximately 2 kHz the processor will not have to wait for zero crossings. At lower frequencies there may be an additional loop service required to obtain a counter reading. These factors make the signal at the CYCLE test point vary with reading rate and input signal. However, for diagnostic purposes the reading rate may be set to 32 and a high frequency input signal applied. The display should be a stable pulse train at a 32.8 msec rate. As the reading rate is reduced the display should show a change in pulse width every 2, 4 or 8 pulses at 16, 8 and 4 rdg/sec, respectively.

All voltmeters are implemented with voltage to frequency (V-F) converters whose outputs are counted to obtain the reading. This counting is performed by a triple counter peripheral IC U022. It contains three 16-bit counters which may be programmed and read by the processor. They count the number of pulses at their clock inputs during the time that their gate inputs are high. To read them the processor sets PC3 low which drives the gate low and stops the counting. When the read operation is finished they are reset and the gate is returned high. The count thus obtained for any given input voltage will vary by factors of two depending on the reading rate selected. This is corrected by the 6805 before the data is passed to the host.

The frequency counter is a reciprocating period based counter. The input signal and a master clock are counted for the desired number of 32.77 msec intervals. The resulting counts are divided and scaled to produce the frequency value. These counters are also implemented with a triple 16-bit counter peripheral IC, U021. One section is used to count the input signal and two are cascaded to count the 5 MHz master clock. A 16-bit counter is not large enough to handle all the counts at maximum frequency and the slowest reading rates. The overflow is counted by U121D.

Flip-flop U251B is used to synchronize the two counters to guarantee that the master clock is counted between an integer number of input signal cycles. Its output drives the gate input of the two counter chains and an status input (PC1) on the processor. The input signal is applied to the appropriate counter and to the clock input of the flip-flop.

Autorange Comparators <3>

The signal from the channel A input amplifier is fed through the preemphasis network R4512, R4511, C4501. This compensates for the slew rate limitations of the op-amps in the preamplifier, reducing amplitude of signal at high frequencies before an up-range occurs. This signal feeds four comparators, two sense the need to up-range and two sense the need to downrange. The two comparators in each pair are used to sense the positive peak value and negative peak value of the signal.

Consider the operation of U361B. Its negative input is connected to the signal input and its positive input is connected to a +1.75 V reference. The output of the comparator will go low when positive signal peak exceeds this reference. U361A performs the same comparison function for negative peaks. The outputs of the two comparators are wired together. Since these are open collector outputs, if either comparator senses too large a peak value the output line will go low. R3504 and RP261 level shift the -15 V output of the comparators to the +5 V logic of U271A. When the comparator output goes low it will set the flip-flop U271A. The microprocessor reads the output of this flip-flop through tri-state buffer U151 and knows if an overrange condition occurred. When the microprocessor reads this information the clock input of U271A is strobed, clearing the overrange indication. The flip-flop allows momentary signal overloads to be detected with infrequent monitoring by the microprocessor.

Comparators U361C and U361D perform the same comparison function on the signal at a 6 dB lower amplitude. If the signal is below this level the microprocessor knows that the input gain must be increased. When the correct input range is achieved the upper comparator output will be high and the lower comparator output will be low. Any change of state in the comparators causes an uprange or downrange as appropriate. Quad comparators U351 and dual flip-flop U261 perform the same level comparison functions on the range amplifier signal.

Comparators U371C and U371D monitor the signal level against a 100 mV reference. This is used to sense when the signal is of insufficient amplitude to guarantee accurate phasemeter operation. When this occurs the output of the comparators will rise. This signal must remain under this minimum level until C3601 charges for the processor to shut down the phasemeter reading.

Tri-state buffer U151 allows the microprocessor to read the state of various logic signals on the phasemeter board. In addition to the three range comparison signals described above, the state of the Channel A input termination resistors (/TERMA) and the channel selection signal (A/B) are monitored.

Frequency Counter Comparator <3>

The Channel A signal enters through R4408. When line LB goes to 0 V, JFET switch Q4402 connects the grounded capacitor C4406 and forms a lowpass filter to reduce the effects of noise and interfering components above 100 kHz. These signals are buffered by U544 which drives the comparators and peak detectors.

Diodes D4403 and D4404 cause the output of U544 to be offset from the input by one diode drop. For positive signal voltages the output will be 0.6 V higher than the input, for negative voltages the output will be 0.6 V lower than the input. This output signal is rectified by diodes D4401 and D4402. The positive voltage from D4402 is stored on capacitor C4404 and serves as the positive threshold reference for the comparators. The negative voltage from D4401 is stored on capacitor C4405 and serves as the negative reference for the comparators. The input signal is developed across RP341 and fed to the two comparators in U342. Each comparator compares the signal to a different reference, one to each of the two references discussed above.

Series resistor-capacitor networks R4404-C4408 and R4403-C4407 provide hysteresis to prevent oscillation on the comparator transitions without disturbing the dc value of the reference voltage. The outputs of the comparators are used to drive flip-flop U251A. The use of separate comparators to compare the zero crossing and the peak provides a large amount of hysteresis and reduces the sensitivity of the counter to interfering noise.

Lowpass filter R3501 and C3501 create the average value of the comparator output. This is compared to TTL thresholds by buffer U151. This creates a duty cycle comparison and is used to derive the polarity information for the polarity function of the analyzer.

Input Circuit <4>

The input signal is derived from the panel connectors or the internal generator monitor path via relays K481 and K581. Relays K481 and K581 are ganged together to provide optimum input isolation when monitoring the generator output. P681 connects to a shielded cable originating on the channel A output of the generator.

Relay K891 selects the 600 Ohm and 150 Ohm terminations. Its control bit originates from the Q output of flip-flop U181B. When a termination is selected the flip-flop Q output clocks high and causes relay K891 to be energized through Q3802. Relay K591 provides 600/150 Ohm selection. In the 600 Ohm selection, relay K591 is open and the termination is composed of resistors R7902-R7904 and R4902. R7901 shunts the 600 Ohm termination to obtain the 150 Ohm termination (300 Ohms in units with option **EURZ**).

The terminations are protected against excessive power dissipation by sensing a small portion of the total input voltage through the divider action of R7903, R4902, and R7904 and the ac optocoupler U491. An input level greater than approximately +32 dBu (30 Vrms) will forward bias the light-emitting diodes inside U491. This causes the phototransistor inside U491 to conduct, thus clearing the control flip-flop U181B and de-energizing relay K891.

The selected input signal passes through RF suppression filters composed of R6801, C6801, R6802, and C6802. In some units C6801 or C6802 may be shunted with a small capacitor to balance the total input capacitance. The signal is then ac-coupled to the input attenuators through C8801 and C8802. C8801 and C8802 are matched for optimum low frequency common mode rejection and must be replaced as a set.

The input attenuators provide four 12 dB steps from 0 dB to -36 dB. Relay K571 is energized in the 0 dB state, K572 for -12 dB, and K672 for -24 dB. -36 dB is the default range with all relays off. Refer to TABLE LVF1.2 for information concerning attenuator selection versus input voltage. C9701 adjusts the attenuator high frequency flatness above approximately 10 kHz. R7705 and R8709 trim the total input resistance to be 100 kOhms, each side to ground.

Signal Preamp <5>

The selected and attenuated input signal is buffered and amplified by U762, U761, U752, and U551. Diodes D5601-5604, and D5607-5610 provide overload protection by clamping the op-amp input voltage to approximately ±13 V, determined by zener diodes D5605 and D5606. High frequency distortion due to the non-linear capacitance of the diodes is minimized by the inherent bootstrap action of this configuration.

NOTE: The residual leakage current of the input clamping diodes can exhibit significant optical modulation. Exposure to fluorescent lighting with the top cover removed may cause an increase in input hum products due to this effect!

When no attenuation has been selected the incandescent lamps R471 and R472, located on schematic <4>, limit input current during an overload condition. Normally the lamps present a low resistance (typically 100-130 Ohms) to the input circuit. During an overload the lamp resistance rises dramatically.

The pre-amplifier gain is controlled by relays K671 and K771, providing +12 dB and +6 dB steps respectively. If both are energized the preamp gain is +18 dB. K651 switches an additional +12 dB gain stage comprising U551, R5501, and R5502 for higher sensitivity. See TABLE LVF1.2 for more information.

TABLE LVF1.2
CHANNEL-A INPUT RANGES & SYSTEM GAIN

	ATTENUATION			PREAMP GAIN					TOTAL
RANGE[1]		K571	K572	K672		K771	K671	K651	GAIN[2]
160 V[3]	-36dB	0	0	0	0dB	0	0	0	-36dB
80 V	-36dB	0	0	0	+6dB	1	0	0	-30dB
40 V	-24dB	0	0	1	0dB	0	0	0	-24dB
20 V	-24dB	0	0	1	+6dB	1	0	0	-18dB
10 V	-12dB	0	1	0	0dB	0	0	0	-12dB
5 V	-12dB	0	1	0	+6dB	1	0	0	-6dB
2.5 V	0dB	1	0	0	0dB	0	0	0	0dB
1.2 V	0dB	1	0	0	+6dB	1	0	0	+6dB
600 mV	0dB	1	0	0	+12dB	0	1	0	+12dB
300 mV	0dB	1	0	0	+18dB	1	1	0	+18dB
160 mV	0dB	1	0	0	+24dB	0	1	1	+24dB
80 mV	0dB	1	0	0	+30dB	1	1	1	+30dB

1 Maximum rms sinewave amplitude for linear operation.
2 INPUT to ASIG
3 140 Vrms is the maximum rated input voltage

U752 is a unity gain differential input to single ended output amplifier. Common mode rejection is trimmed by R9601 which balances the + and - input signal path gains. U651 and its related components comprise a dc servo that maintains a near zero dc offset condition at the output of U752 under all gain conditions. The output of the integrator is fed back through R8507 into the + signal path. C5502 and R5505 provide low frequency compensation that corrects for the input ac coupling rolloff below about 30 Hz.

The output signal from relay K651 is labeled ASIG and is routed several places. It is connected to the channel A input ranging comparators shown on schematic <3>, J461-6 (to the dual input/phasemeter board), and to the ASIG monitor buffers U571A and U571B. The output from U571A is connected through R8502 and a shielded cable to the front panel CHANNEL A MONITOR connector. Note that there is a 6 dB loss introduced by R8504 and R8503. U751B provides the ASIG source in SYS-2xx and SYS-3xx configurations. Under normal conditions of autoranging the peak value of ASIG will vary over a 6-7 dB window between approximately 1.60-3.75 Vpeak.

In the SYS-11 configuration only a jumper is inserted between pins 6 and 8 of J461 to connect ASIG to MAINSIG because the PHA-1 board is not present.

Range Amp & Lowpass Filters <6>

MAINSIG is routed to J951-7 connecting to the DIS-1 module. FUNCSIG is the selected signal to be passed to the main voltmeter and CNTRSIG is the signal presented to the frequency counter. In the amplitude measurement mode FUNCSIG is connected directly to MAINSIG via a relay on the DIS-1 module.

FUNCSIG is connected to the Range Amp stage consisting of a programmable 0 dB to -48 dB attenuator and a fixed +20.6 dB gain (x11) amplifier U741. CMOS switch U742 selects one of five 12 dB attenuator steps. U742 is controlled by three bits originating from Q2-Q4 of data latch U171. U741 is operated non-inverting to prevent loading on U742. C9405 adjusts high frequency flatness above approximately 50 kHz.

TABLE LVF1.3
RANGE AMPLIFIER SWITCHING

AMPLITUDE RANGE	ATTEN	U742 A	U742 B	U742 C	ADDED GAIN
≥80 mV	-48 dB	0	1	1	0 dB
20 mV	-36 dB	1	0	0	+12 dB
5 mV	-24 dB	1	0	1	+24 dB
1.2 mV	-12 dB	1	1	0	+36 dB
300 uV	0 dB	1	1	1	+48 dB

The output of the range amp U741 becomes the input to the lowpass bandwidth limiting filter stage. This stage provides four selections of high frequency rolloff including flat (">500 kHz"), 80 kHz, 30 kHz, and 22 kHz. In the flat state the upper -3 dB point is typically 600-700 kHz.

The 80 kHz and 30 kHz filters have 3-pole Butterworth response and are composed of U543A and U543B respectively. Typical -3 dB frequency accuracy is 3% (5% specified). The 22 kHz filter U541A is cascaded from the output of the 30 kHz filter to provide a 6-pole response with a sharper rolloff beyond the audio spectrum. Its -3 dB point is approximately 22.4 kHz and the response shape has been optimized to conform to CCIR Recommendation 468 for unweighted measurements. The CMOS MUX U542 selects the desired lowpass filter and is buffered through U541B. U541B also provides approximately +7 dB of gain. Filter selection is controlled by two bits originating from data latch U421, outputs 5Q and 6Q.

The output of the range amp U741 also drives an inverting amplifier composed of U544A, R6411, and R6412. This provides the signal (RANGESIG) that is routed to the comparators on schematic <3> for autoranging control of U742. When properly operating the peak output of the range amp U741 will vary over a 12-13 dB window between approximately 35-160 mV; and the output of the lowpass buffer U541B will vary between approximately 70-340 mV peak.

U841 and U842 provide regulated ±6 Volts to operate the CMOS MUXs on schematics <6> and <7>. The accuracy of these supplies is not critical to instrument calibration. The regulator ICs contain over-dissipation and current limiting protection.

Option & Highpass Filters <7>

LPSIG is the output from the lowpass bandwidth limiting filter stage and is connected to pin 8 of option filter sockets J801, J811, J812, and J813. Option filters derive their input from this signal. The outputs are connected to pin 2 of their respective socket, and selected by the CMOS MUX U521. The three control bits labeled WA, WB, and WC originate from the 3Q, 4Q, and 7Q outputs of data latch U421 located on schematic <6>. When all bits are low (0V) a bypass path is selected for no option filtering.

LPSIG also drives buffer amplifier U622B which provides the front panel EXT FILTER OUTPUT signal through a cable connected to P621. The front panel EXT FILTER INPUT is connected through P622 and overload protection resistor R6201 to the selection MUX U521.

The option filter buffer U512A provides unity gain and a low impedance source to the following highpass filter stage. R5102 and diodes D5101-D5102 limit the maximum signal amplitude during ranging transients to minimize settling time. Under normal conditions of autoranging the peak signal will not exceed approximately 340 mV, unless the external or option filters exhibit greater than unity gain.

The highpass bandwidth limiting filter stage comprises U512B, CMOS MUX U511, and related circuitry. Four selections are provided including flat (<10 Hz), 22 Hz, 100 Hz, and 400 Hz. The 100 Hz and 400 Hz filter responses are 3-pole Butterworth with a typical -3 dB frequency accuracy of 3% (5% guaranteed). The 22 Hz response is also 3-pole but has been optimized to conform to the requirements of CCIR Rec 468. R9001 adjusts the flatness above 50 Hz of the 22 Hz filter. R6100, R7100, and R5101 provide gain compensation to correct for stray capacitive loading effects in the filters.

The output of the highpass bandwidth limiting filter is coupled through C5001 to the last gain stage composed of U701 and related components. This gain stage has about +20.6 dB of gain (x11) and drives the ac-dc detectors. The signal amplitude at this point typically varies between 0-3.7 Vpeak, however significantly higher peak amplitudes may be present depending upon the exact signal and filter selection. R9101 adjusts the READSIG offset and R9102 adjusts low frequency flatness below 20 Hz.

U821A provides a buffered replica of READSIG for external monitoring. The output of U821A is coupled through R8201 and a shielded cable to the front panel READING MONITOR OUTPUT connector. U821B provides a buffered signal to the DSP module, if installed. R7201 and R7202 provide a 6 dB loss and a convenient node to couple the output signal OPTSIG from the Wow & Flutter option.

RMS, AVG, & PEAK Detectors <8>

The final processed signal, READSIG from <7>, is applied to the rms detector, U822 (Analog Devices AD637), and a precision full-wave rectifier for the average and peak detection modes. The rms detector integration time constant is determined by C8302, C4301, C4302 and controlled by one half of CMOS switch U431. R8301 adjusts the offset error term of the rms detector. The rms detector output at U431-13 is normally 0 to +2.6 V. D8301, R8302, and R8303 provide clamping to minimize settling time from ranging transients. R3302, R3304, C3301, and C3302 form a 2-pole lowpass filter to reduce the ac ripple content in the detector output dc voltage. The output of this network is applied to one of the inputs of the detector selection MUX U331.

U731A and U731B comprise a precision full-wave rectifier used for the AVG, Q-PEAK, S-PEAK, and PEAK modes of detection. R9301 adjusts the rectifier balance and is adjusted for equal amplitude peaks at TP9203 with a low level sinewave signal. R9201 adjusts for the offset error term while R9103 trims the rectifier gain. D7201 and D7202 clamp the rectifier output to minimize overload recovery from ranging transients.

Average detection is accomplished by filtering the full-wave rectified signal. Filter networks R5302-R5303-C5301-C5302, R5304-R5305-C5303-C5304, and R5306-R5307-C5305-C5306 provide three different integration time constants selected by half of CMOS MUX U431. The integration time constants are selected by two control bits originating from 5Q and 6Q of data latch U321, and are ganged to the reading rate selection.

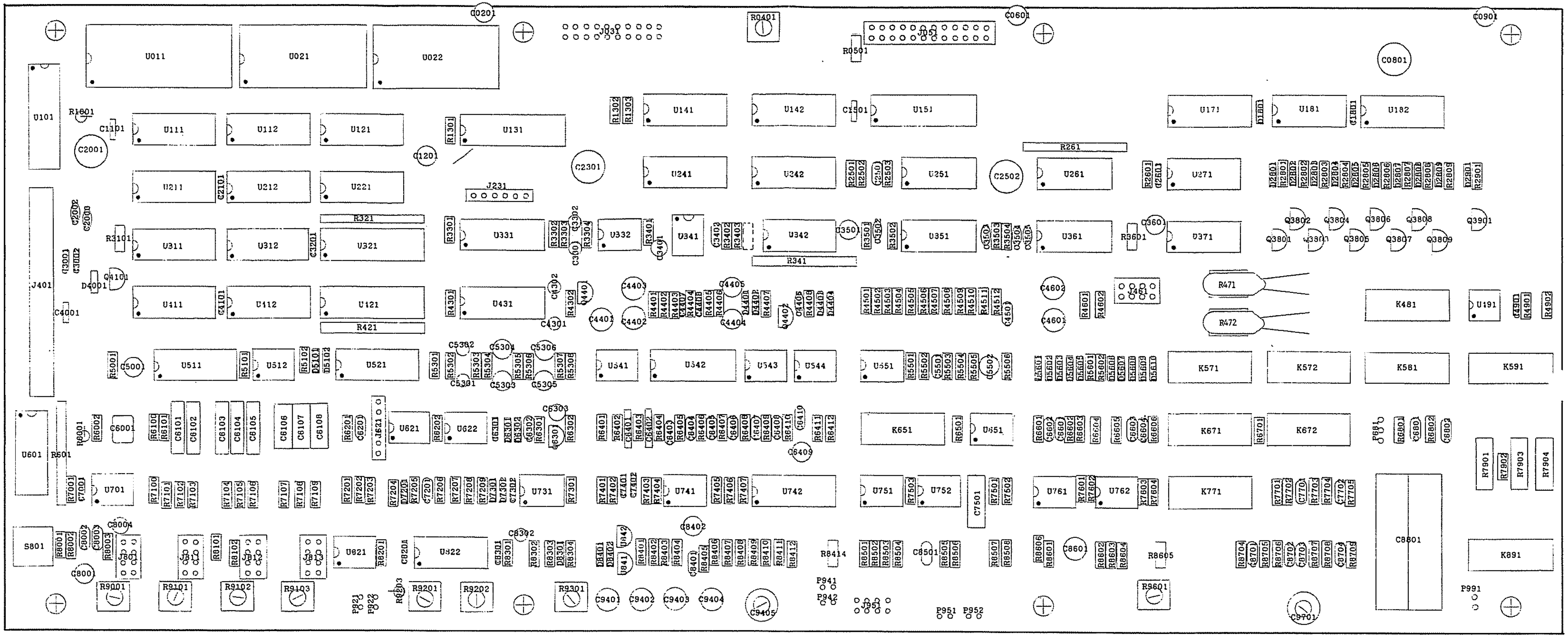
The Q-PEAK and PEAK detector is composed of U622A and buffer U322B. The S-PEAK detection mode is identical to PEAK except that readings are scaled by 0.7071 (in software) to read the rms equivalent of a sinewave with the same peak value. U622A and D6301-D6302, R6301-6302, and C6303 form a fast attack-slow decay peak detector that captures the peak value of the full-wave rectifier output. When Q6301 is off, R6302 is effectively in series with C6303 and increases the attack time to achieve the proper quasi-peak detector response. The output of buffer U322B is attenuated slightly and filtered by R4301, R3301, and C4403 to scale the output dc voltage and provide the correct ballistic response required by CCIR Recommendation 468. When Q6301 is on, the series resistance becomes very small resulting in a very fast attack time with almost ideal peak detection for repetitive signals. R6301 determines the decay time constant which is approximately 300 msec with any of the peak detector selections.

MUX U331 selects the output of the rms detector, the selected average detector integration network, the quasi-peak/peak detector output, or the output from J231-1 and J231-5 used with the Wow & Flutter option. The MUX is buffered with U332A and provides feedback for the various rms and average detector filter networks. The buffer output is additionally filtered through R3401 and C3401 before being presented to the voltage-to-frequency converter, U341.

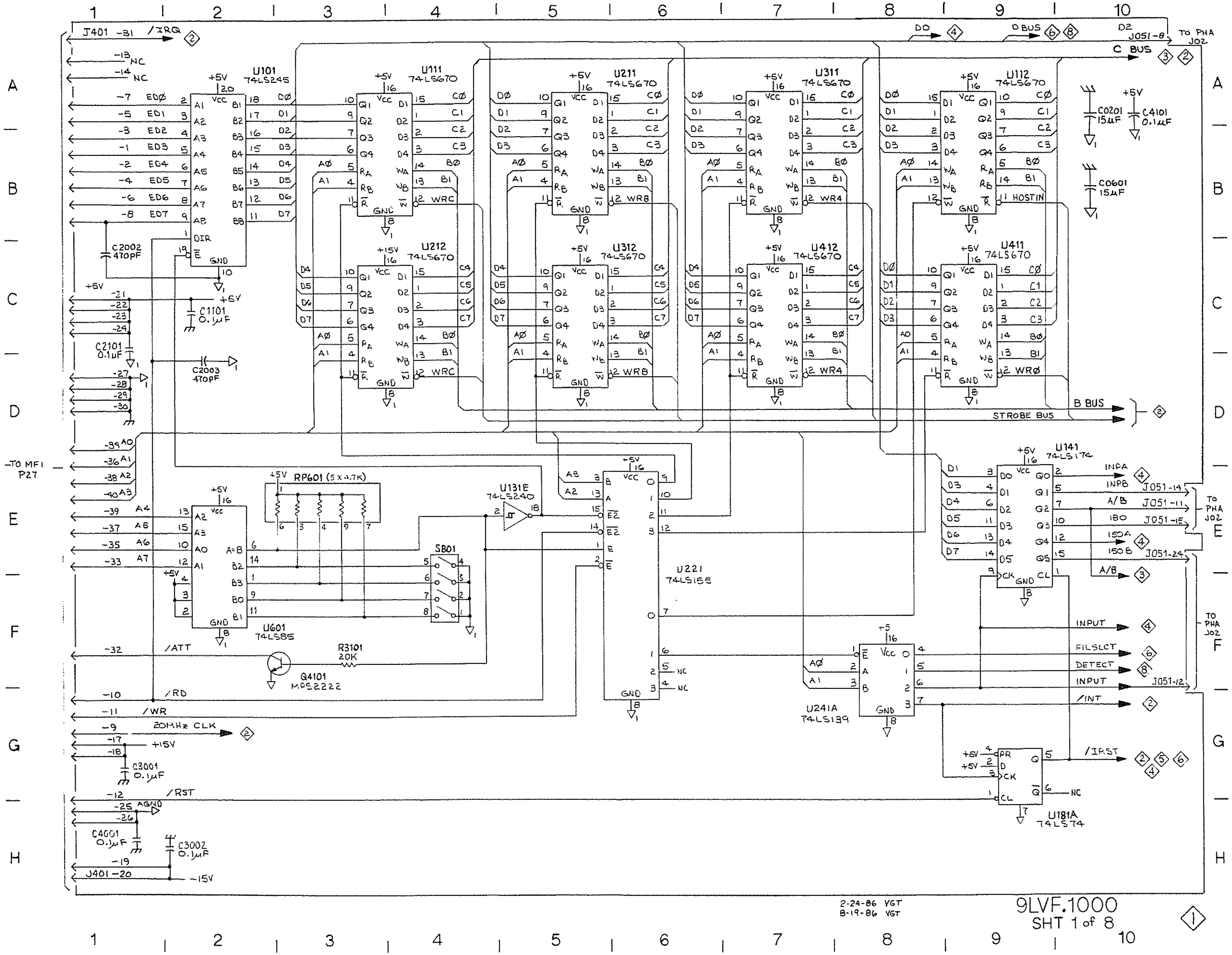
Voltage measurements are accomplished by measuring the output frequency of a voltage-to-frequency (V-F) converter. This technique offers superior noise integration and permits reading rate selection by switching the frequency counter gate interval. The V-F converter is a monolithic IC (AD654) that outputs a TTL compatible squarewave whose frequency is a linear function of the input dc voltage. A nominal 2.5-2.6 Vdc input produces a 100 kHz "full scale" output frequency. R0401 adjusts for gain tolerances in the V-F converter and its timing capacitor C3402. R3403 is selected to center the adjustment range of R0401. R3404 improves the noise immunity of the converter at very low levels. TABLE LVF1.4 gives the approximate full scale resolution as a function of reading rate.

TABLE LVF1.4
DETECTOR RESOLUTION VERSUS READING RATE

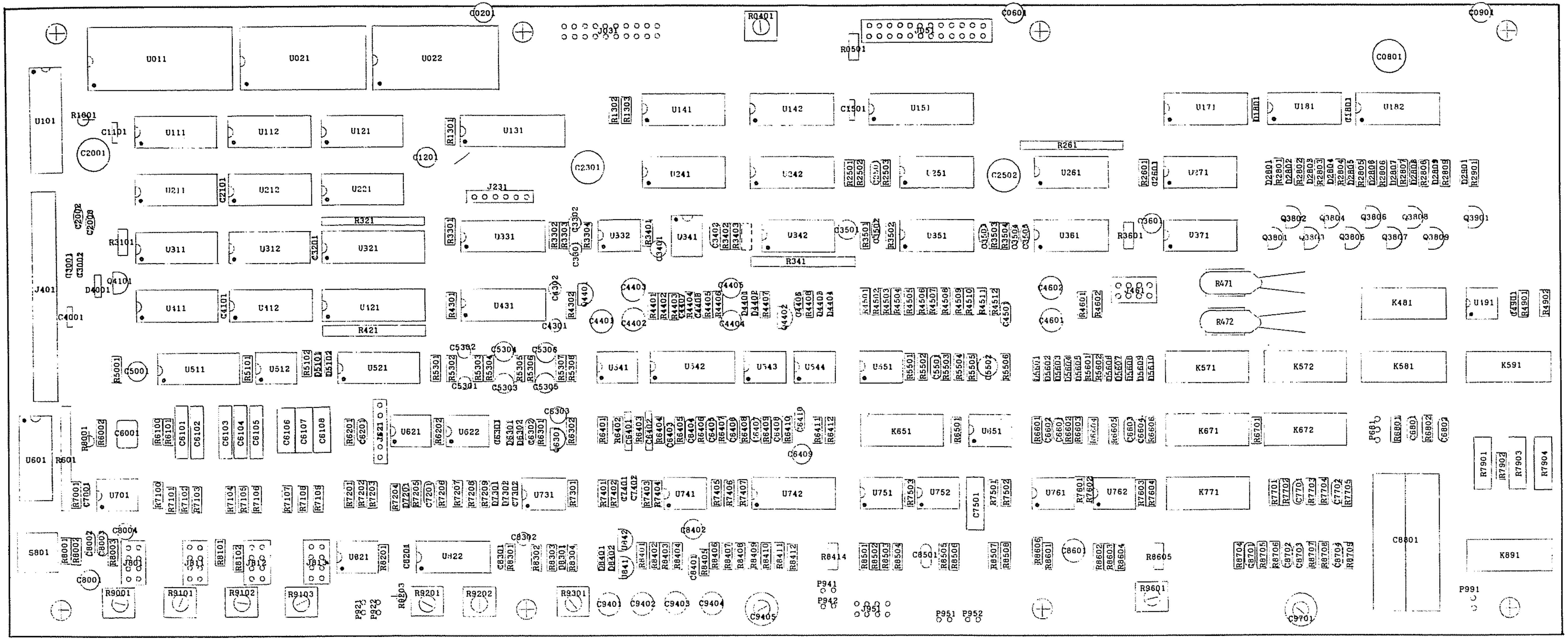
READING RATE	COUNTER INTERVAL	FULL SCALE RESOLUTION
32/sec	32.77 msec	1/3150
16/sec	65.5 msec	1/6300
8/sec	131.1 msec	1/12600
4/sec	262.1 msec	1/25200



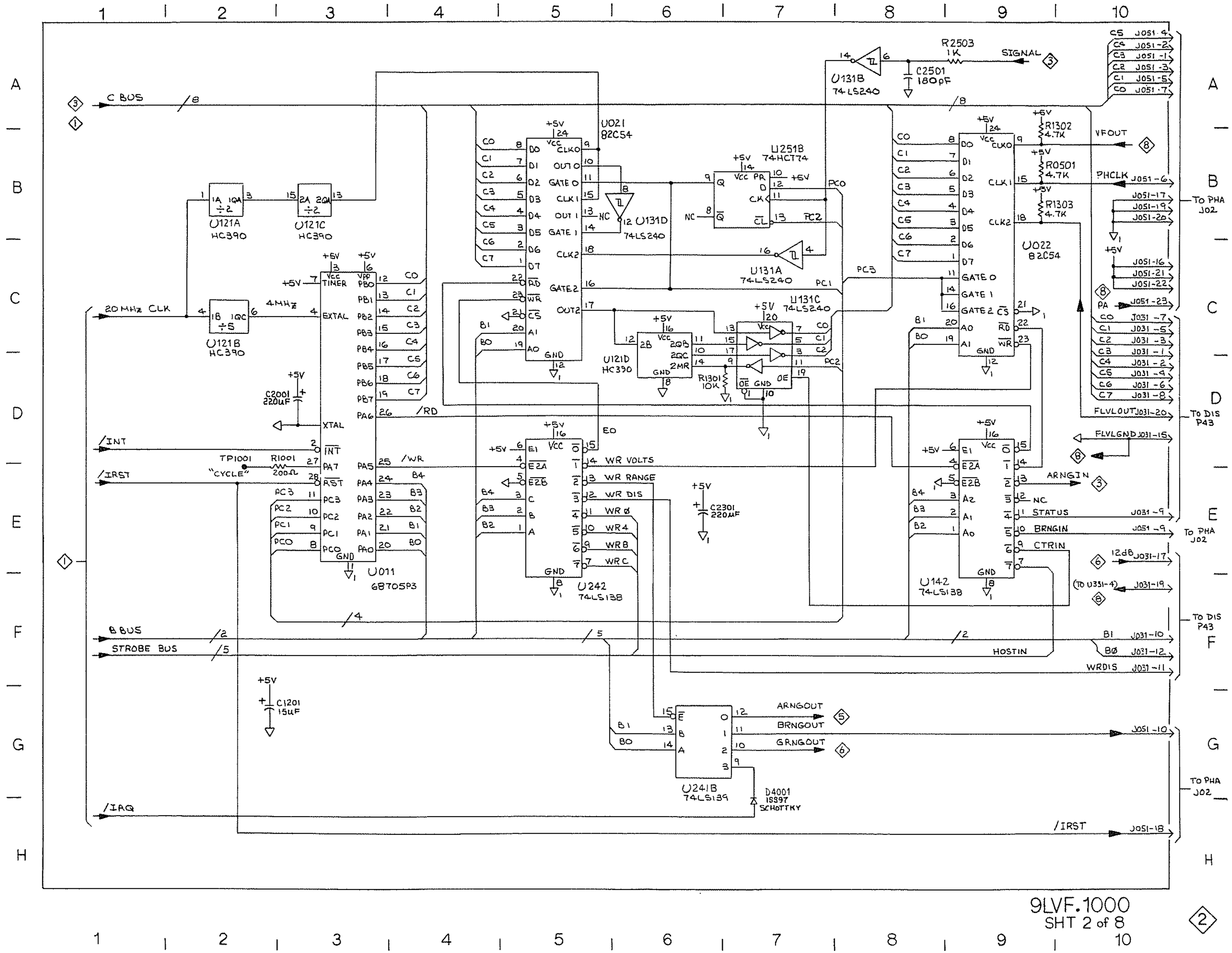
LEVEL FREQUENCY MEASUREMENT (LVF)



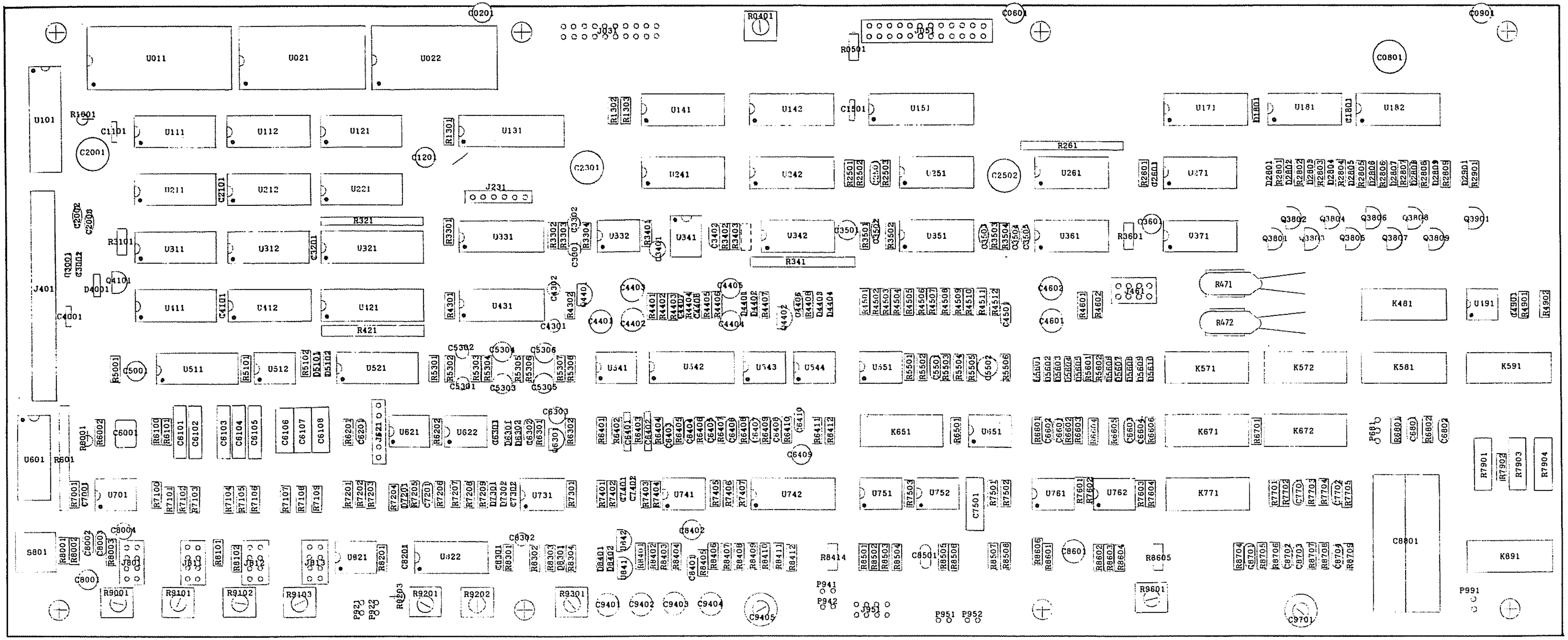
9LVF.1000
SHT 1 of 8



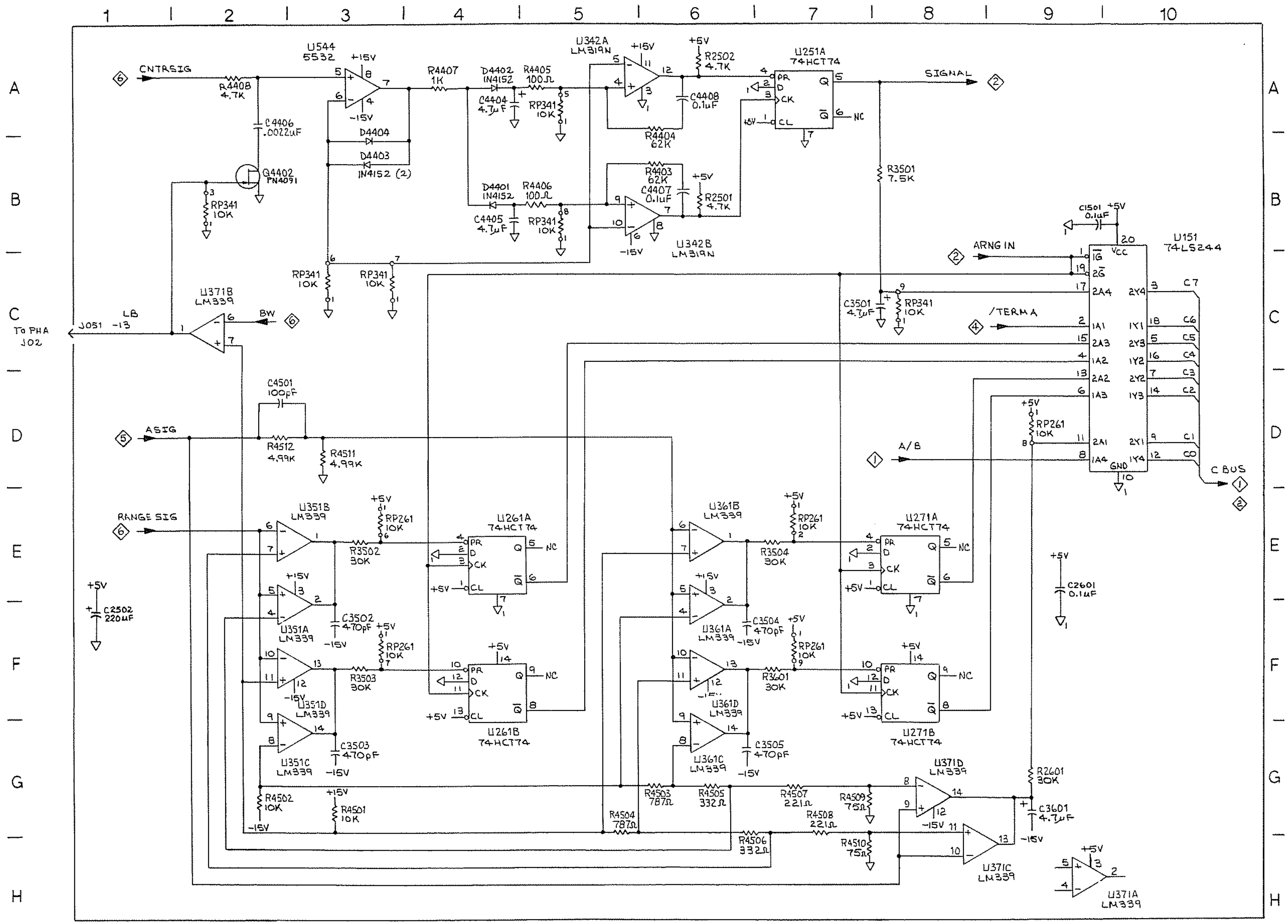
LEVEL FREQUENCY MEASUREMENT (LVF)



9LVF.1000
SHT 2 of 8

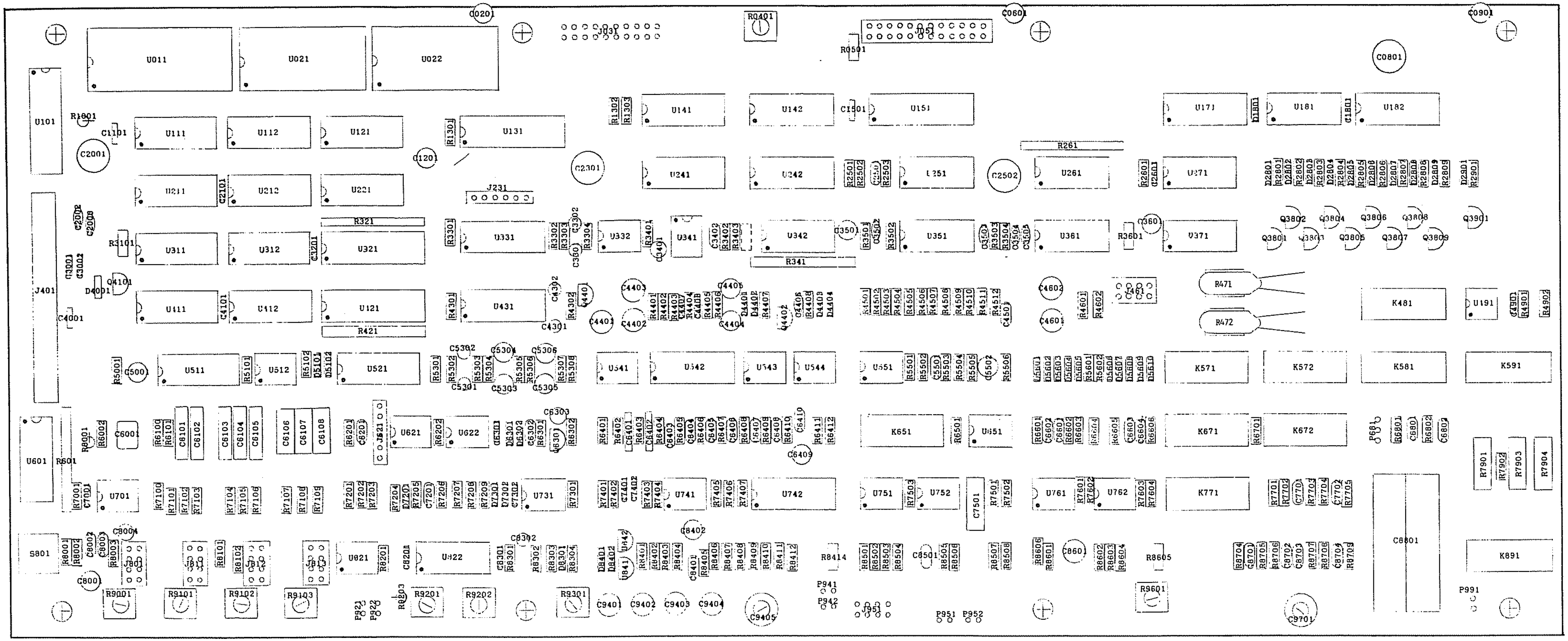


LEVEL FREQUENCY MEASUREMENT (LVF)

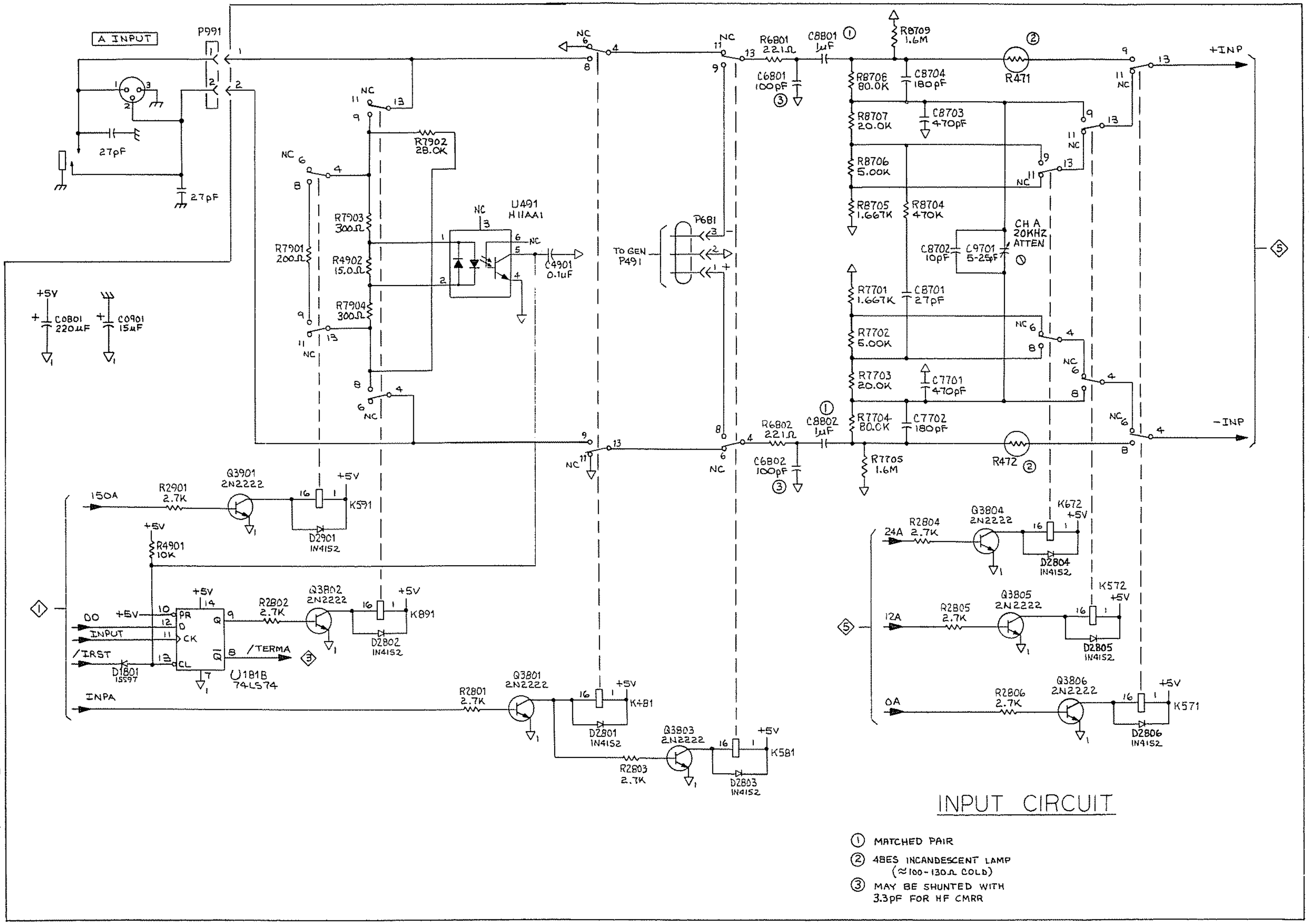


9LVF.1000
SHT 3 of 8

3



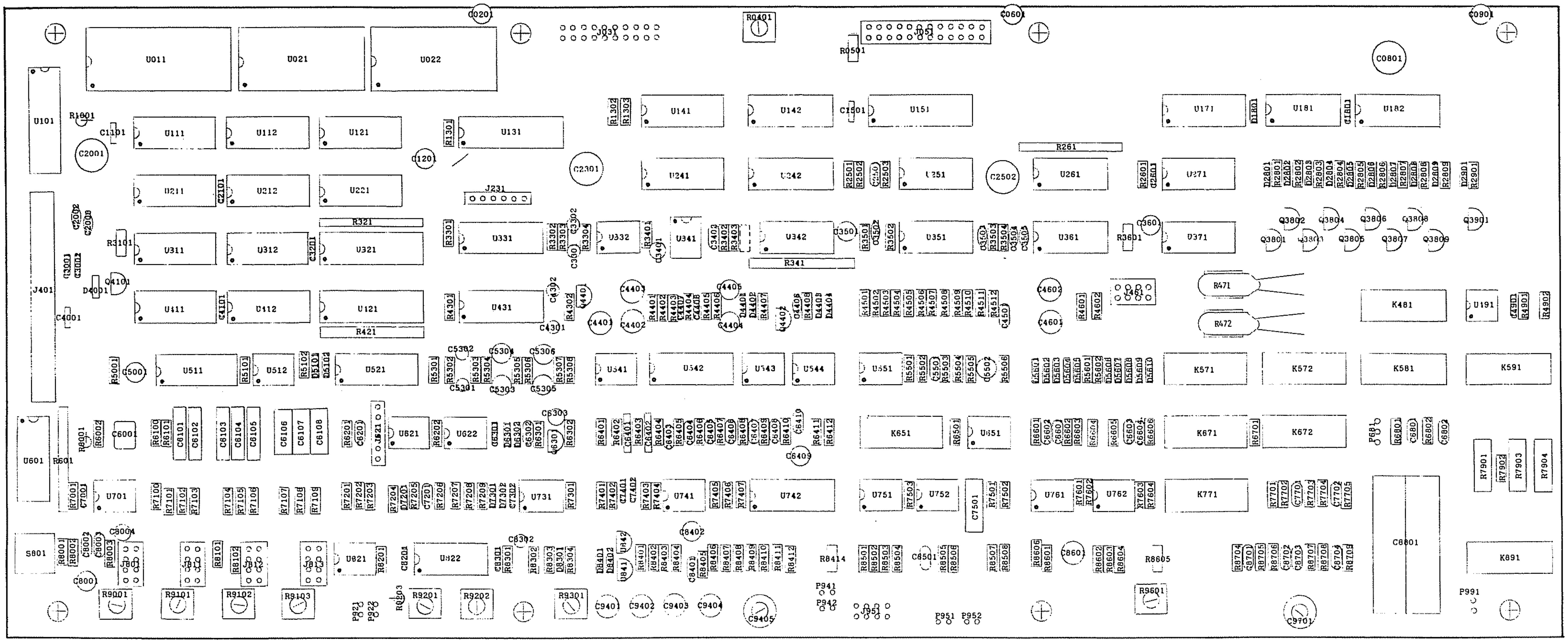
LEVEL FREQUENCY MEASUREMENT (LVF)



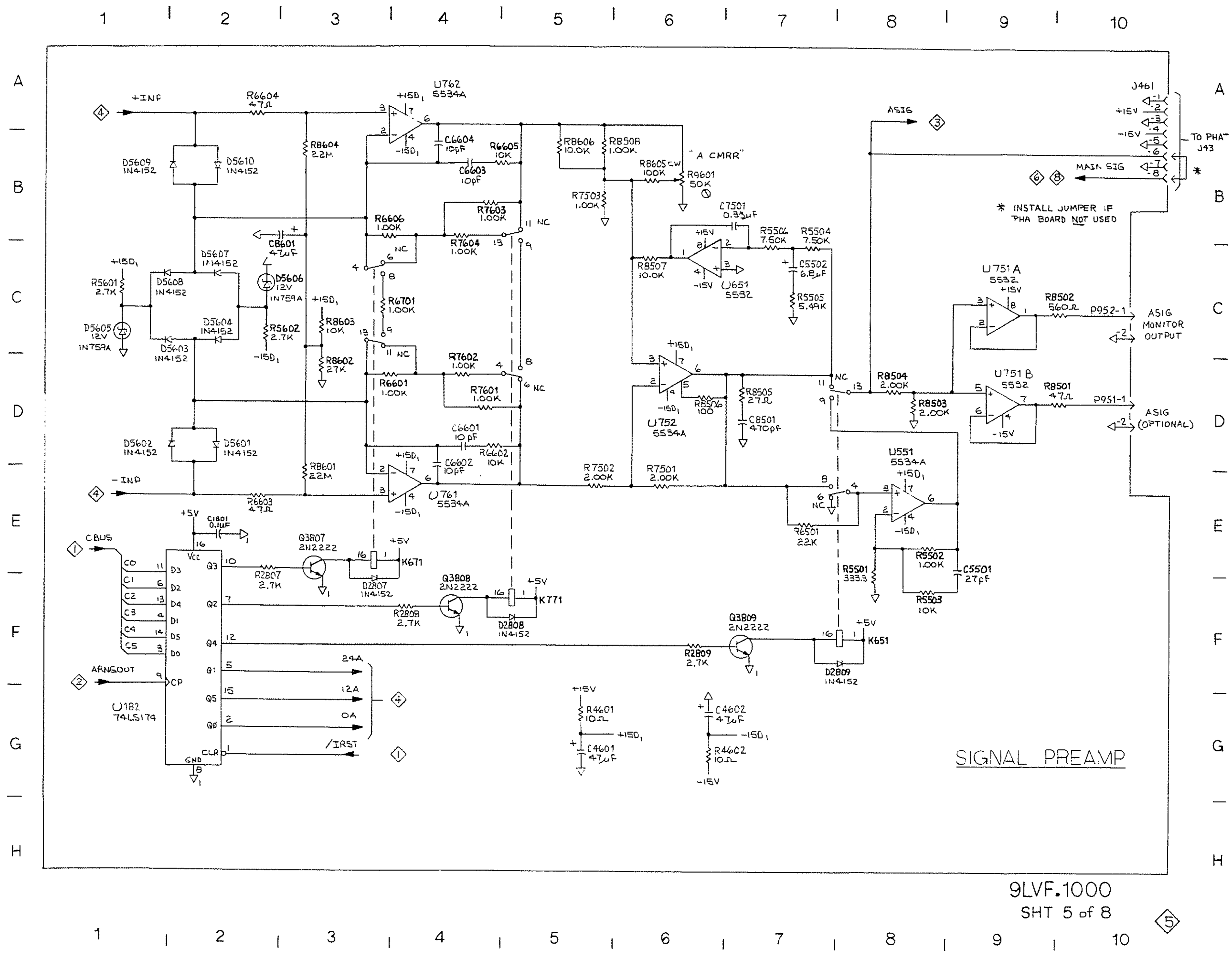
INPUT CIRCUIT

1. MATCHED PAIR
2. 48ES INCANDESCENT LAMP (≈100-130Ω COLD)
3. MAY BE SHUNTED WITH 3.3pF FOR HF CMRR

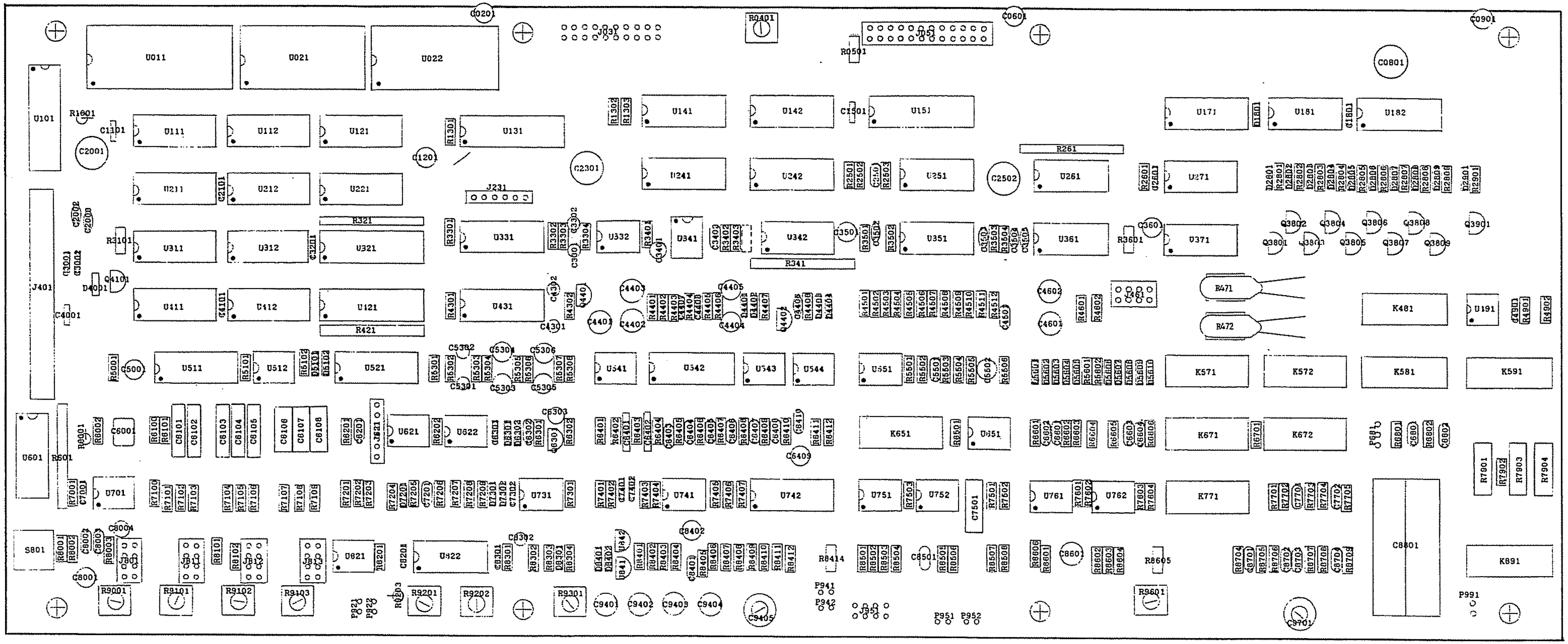
9LVF.1000
SHT 4 of 8



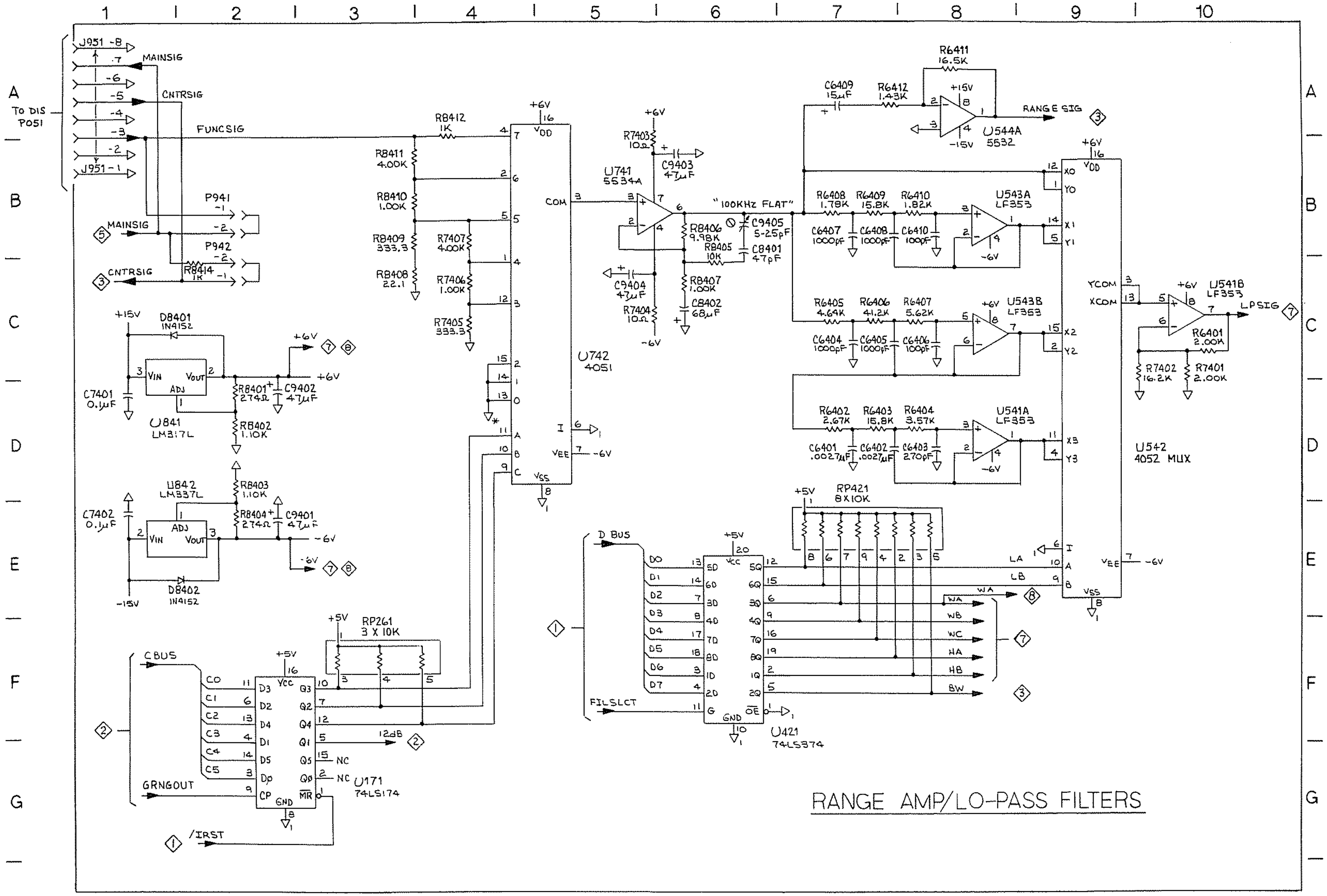
LEVEL FREQUENCY MEASUREMENT (LVF)



9LVF.1000
SHT 5 of 8

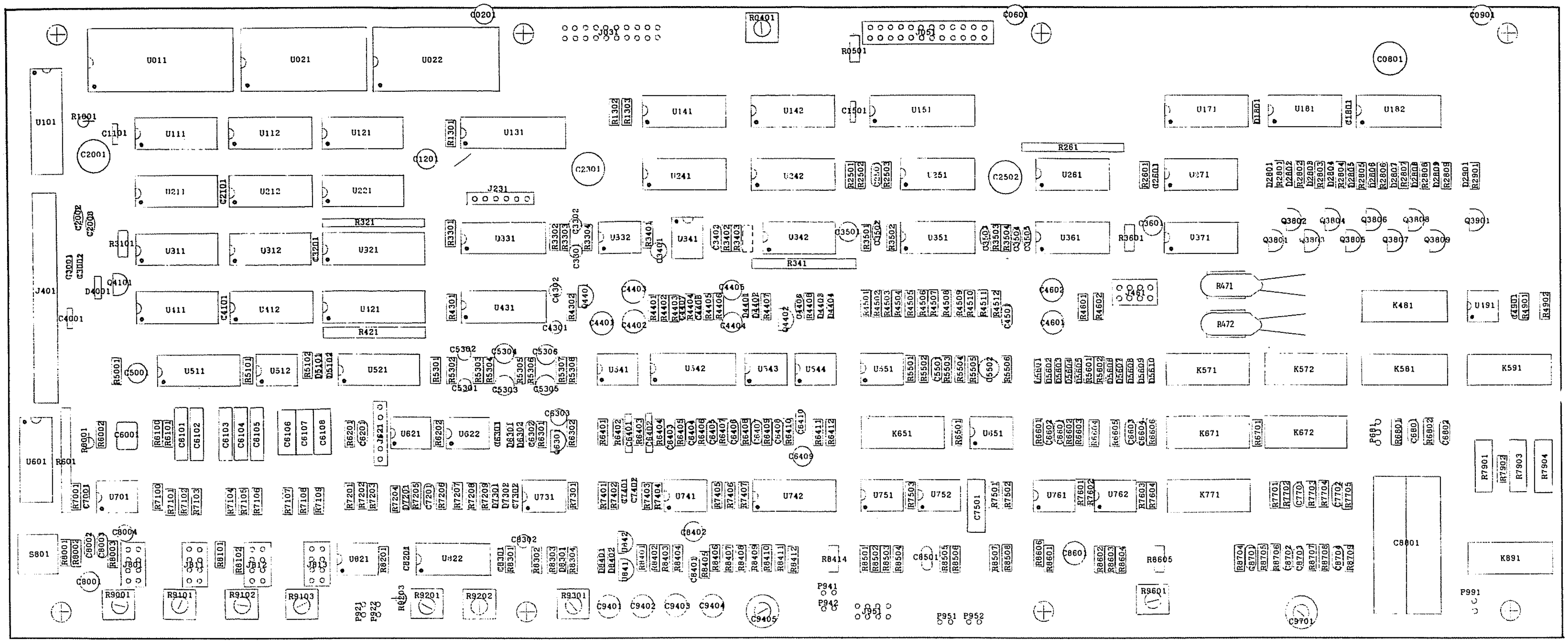


LEVEL FREQUENCY MEASUREMENT (LVF)

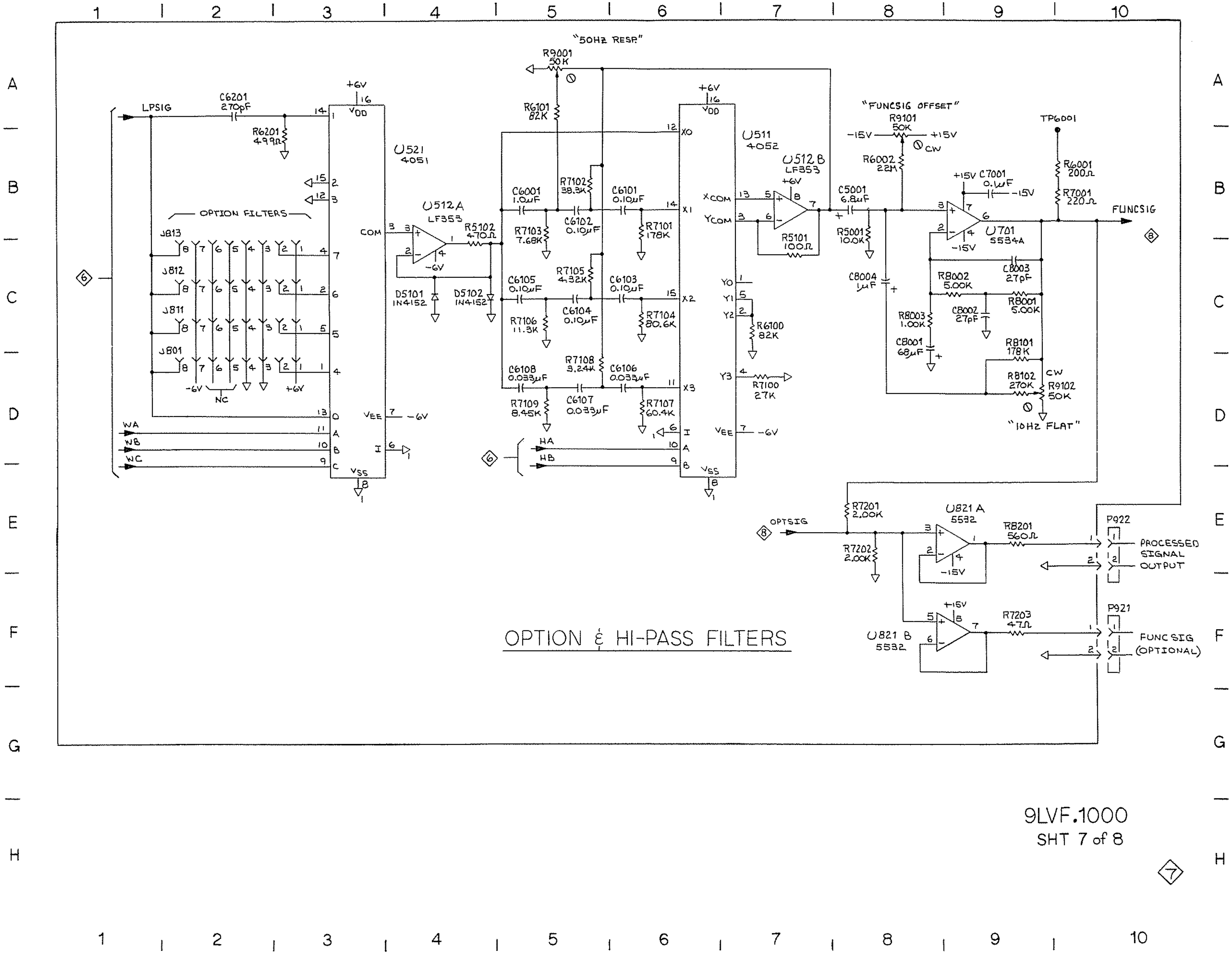


RANGE AMP/LO-PASS FILTERS

9LVF-1000
SHT 6 of 8

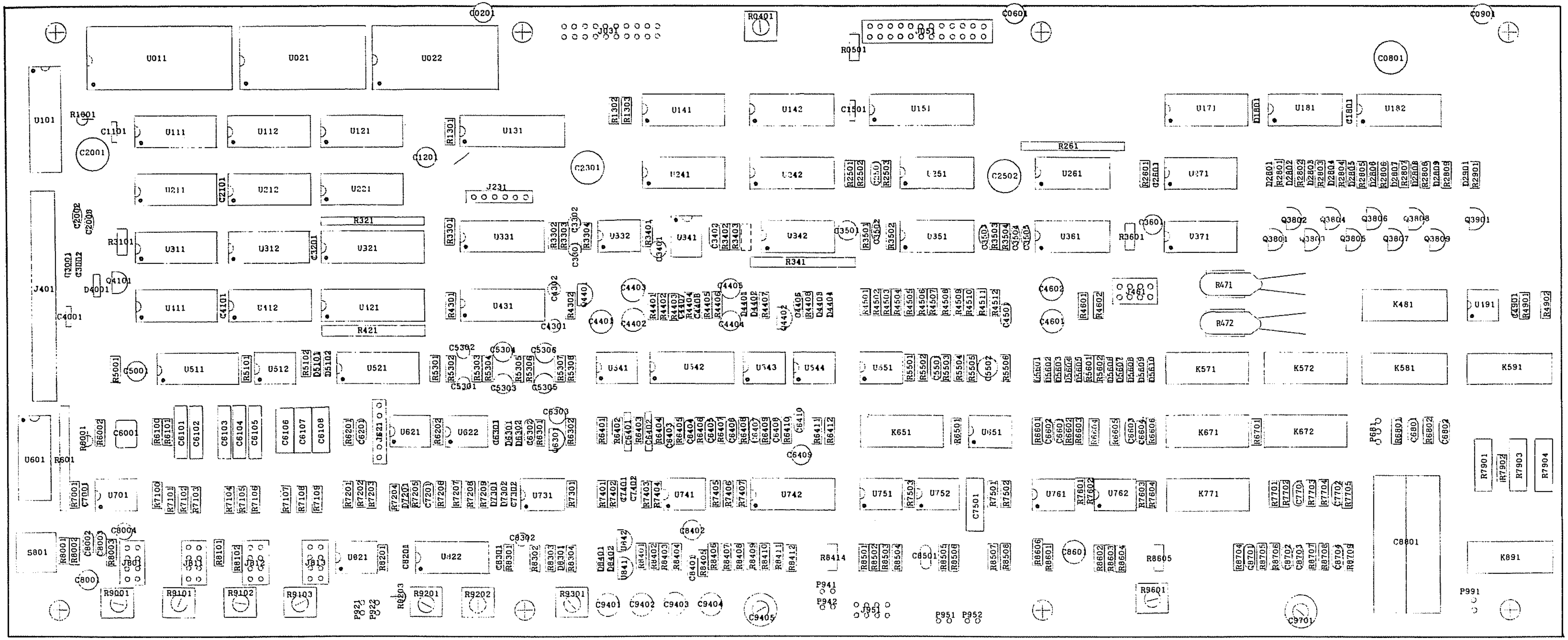


LEVEL FREQUENCY MEASUREMENT (LVF)

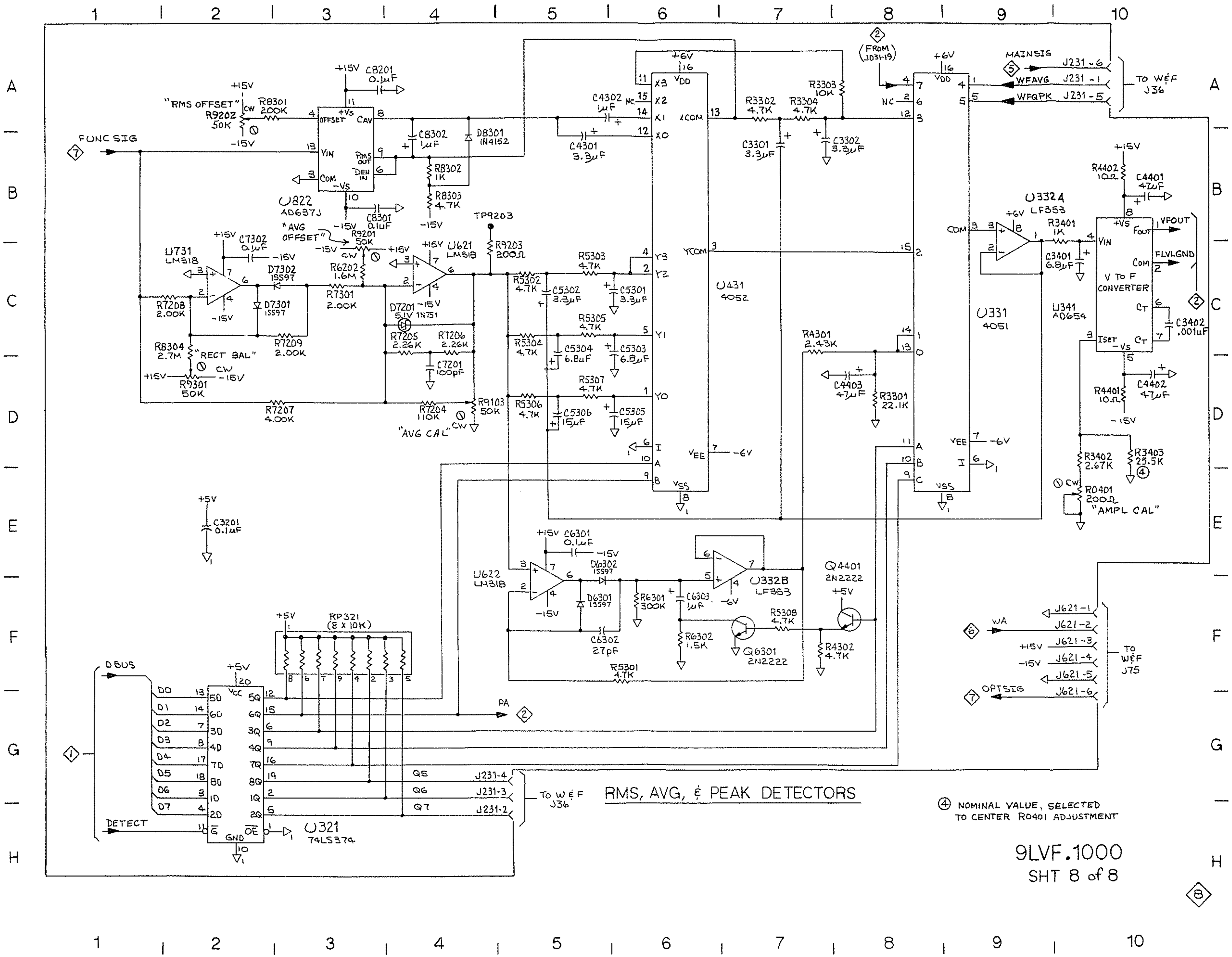


OPTION & HI-PASS FILTERS

9LVF.1000
SHT 7 of 8



LEVEL FREQUENCY MEASUREMENT (LVF)


RMS, AVG, & PEAK DETECTORS
9LVF.1000
SHT 8 of 8
④ NOMINAL VALUE, SELECTED TO CENTER R0401 ADJUSTMENT
"RMS OFFSET" R9202 50K
R8301 200K
U822 AD637J
C8201 0.1μF
C8302 1μF
D8301 IN4152
R8302 1K
R8303 4.7K
C8301 0.1μF
FUNC SIG
U731 LM318
C7302 0.1μF
D7302 1S597
D7301 1S597
R7208 2.00K
R8304 2.7M
"RECT BAL"
R9301 50K
R7209 2.00K
R7207 4.00K
"AVG OFFSET" R9201 50K
R6202 1.6M
R7301 2.00K
U621 LM318
D7201 5.1V 1N751
R7205 2.26K
R7206 2.26K
C7201 100pF
R7204 110K
R9103 50K
"AVG CAL"
TP9203
R9203 200Ω
C4302 1μF
C4301 3.3μF
U431 4052
R5302 4.7K
C5302 3.3μF
R5303 4.7K
C5301 3.3μF
R5304 4.7K
C5304 6.8μF
R5305 4.7K
C5303 6.8μF
R5306 4.7K
C5306 15μF
R5307 4.7K
C5305 15μF
R3302 4.7K
R3304 4.7K
R3303 10K
C3301 3.3μF
C3302 3.3μF
(FROM J031-19)
MAINSIG J231-6
WFAVG J231-1
WFQPK J231-5
TO W&F J36
U331 4051
R4301 2.43K
C4403 47μF
R3301 22.1K
U332A LF353
R3401 1K
C3401 6.8μF
U341 AD654
V TO F CONVERTER
VFOUT
FLVLGND
R4402 10Ω
C4401 47μF
C3402 .001μF
R4401 10Ω
C4402 47μF
R3402 2.67K
R3403 25.5K
R0401 200Ω "AMPL CAL"
C3201 0.1μF
U622 LM318
C6301 0.1μF
D6302 1S597
D6301 1S597
C6302 27pF
R6301 300K
C6303 1μF
R6302 1.5K
U332B LF353
Q6301 2N2222
R5308 4.7K
Q4401 2N2222
R4302 4.7K
R5301 4.7K
WA J621-1 J621-2
+15V J621-3
-15V J621-4
J621-5
OPTSIG J621-6
TO W&F J75
RP321 (8 X 10K)
DBUS
DETECT
U321 74LS374
PA
QS J231-4
Q6 J231-3
Q7 J231-2
TO W&F J36

Board Loc.	Schematic Loc.	Part Number	Description	
C0201	1A10	2832.0156	CAP TA-EL 25V 20%	15uF
C0601	1B10	2832.0156	CAP TA-EL 25V 20%	15uF
C0801	4C1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C0901	4C1	2832.0156	CAP TA-EL 25V 20%	15uF
C1101	1C2	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	2G2	2832.0156	CAP TA-EL 25V 20%	15uF
C1501	3B9	2172.0104	CAP CERAM 100V 20%	.1uF
C1801	5E2	2172.0104	CAP CERAM 100V 20%	.1uF
C2001	2D3	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2002	1C1	2172.0471	CAP CERAM 100V 20%	470pF
C2003	1D2	2172.0471	CAP CERAM 100V 20%	470pF
C2101	1C1	2172.0104	CAP CERAM 100V 20%	.1uF
C2301	2E6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2501	2A8	2296.0181	CAP MICA 500V 1%	180pF
C2502	3F1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C2601	3E9	2172.0104	CAP CERAM 100V 20%	.1uF
C3001	1G1	2172.0104	CAP CERAM 100V 20%	.1uF
C3002	1H2	2172.0104	CAP CERAM 100V 20%	.1uF
C3201	8E2	2172.0104	CAP CERAM 100V 20%	.1uF
C3301	8B7	2952.0335	CAP AL-EL 50V 20%	3.3uF
C3302	8B7	2952.0335	CAP AL-EL 50V 20%	3.3uF
C3401	8C10	2932.0685	CAP AL-EL 35V 20%	6.8uF
C3402	8C10	2296.0102	CAP MICA 500V 1%	.001uF
C3501	3C8	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3502	3F3	2172.0471	CAP CERAM 100V 20%	470pF
C3503	3G3	2172.0471	CAP CERAM 100V 20%	470pF
C3504	3F6	2172.0471	CAP CERAM 100V 20%	470pF
C3505	3G6	2172.0471	CAP CERAM 100V 20%	470pF
C3601	3G9	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4001	1H1	2172.0104	CAP CERAM 100V 20%	.1uF
C4101	1A10	2172.0104	CAP CERAM 100V 20%	.1uF
C4301	8B5	2952.0335	CAP AL-EL 50V 20%	3.3uF
C4302	8A5	2952.0105	CAP AL-EL 50V 20%	1uF
C4401	8B10	2932.0476	CAP AL-EL 25V 20%	47uF
C4402	8D10	2932.0476	CAP AL-EL 25V 20%	47uF
C4403	8D8	2932.0476	CAP AL-EL 25V 20%	47uF
C4404	3A4	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4405	3B4	2942.0475	CAP AL-EL 35V 20%	4.7uF
C4406	3A2	2172.0222	CAP CERAM 100V 20%	.0022uF
C4407	3B6	2172.0104	CAP CERAM 100V 20%	.1uF
C4408	3A6	2172.0104	CAP CERAM 100V 20%	.1uF
C4501	3D2	2296.0101	CAP MICA 500V 1%	100pF
C4601	5G5	2932.0476	CAP AL-EL 25V 20%	47uF
C4602	5G6	2932.0476	CAP AL-EL 25V 20%	47uF
C4901	4C5	2172.0104	CAP CERAM 100V 20%	.1uF
C5001	7B8	2932.0685	CAP AL-EL 35V 20%	6.8uF
C5301	8C6	2952.0335	CAP AL-EL 50V 20%	3.3uF
C5302	8C5	2952.0335	CAP AL-EL 50V 20%	3.3uF
C5303	8C6	2932.0685	CAP AL-EL 35V 20%	6.8uF
C5304	8C5	2932.0685	CAP AL-EL 35V 20%	6.8uF
C5305	8D6	2832.0156	CAP TA-EL 25V 20%	15uF
C5306	8D5	2832.0156	CAP TA-EL 25V 20%	15uF
C5501	5E9	2294.0270	CAP MICA 500V 5%	27pF
C5502	5C7	2932.0685	CAP AL-EL 35V 20%	6.8uF

Replaceable Electrical Parts List LVF-1

Board Loc.	Schematic Loc.	Part Number	Description	
C6001	7B5	2454.0105	CAP POLYE 50V 5%	1uF
C6101	7B6	2675.0104	CAP POLYC 100V 2%	.1uF
C6102	7B5	2675.0104	CAP POLYC 100V 2%	.1uF
C6103	7C6	2675.0104	CAP POLYC 100V 2%	.1uF
C6104	7C5	2675.0104	CAP POLYC 100V 2%	.1uF
C6105	7C5	2675.0104	CAP POLYC 100V 2%	.1uF
C6106	7D6	2675.0333	CAP POLYC 100V 2%	.033uF
C6107	7D5	2675.0333	CAP POLYC 100V 2%	.033uF
C6108	7D5	2675.0333	CAP POLYC 100V 2%	.033uF
C6201	7A2	2296.0271	CAP MICA 500V 1%	270pF
C6301	8E5	2172.0104	CAP CERAM 100V 20%	.1uF
C6302	8F5	2294.0270	CAP MICA 500V 5%	27pF
C6303	8F6	2952.0105	CAP AL-EL 50V 20%	1uF
C6401	6D7	2675.0272	CAP POLYC 100V 2%	.0027uF
C6402	6D7	2675.0272	CAP POLYC 100V 2%	.0027uF
C6403	6D8	2296.0271	CAP MICA 500V 1%	270pF
C6404	6C7	2296.0102	CAP MICA 500V 1%	.001uF
C6405	6C7	2296.0102	CAP MICA 500V 1%	.001uF
C6406	6C8	2296.0101	CAP MICA 500V 1%	100pF
C6407	6B7	2296.0102	CAP MICA 500V 1%	.001uF
C6408	6B7	2296.0102	CAP MICA 500V 1%	.001uF
C6409	6A7	2832.0156	CAP TA-EL 25V 20%	15uF
C6410	6B8	2296.0101	CAP MICA 500V 1%	100pF
C6601	5D4	2294.0100	CAP MICA 500V 5%	10pF
C6602	5D4	2294.0100	CAP MICA 500V 5%	10pF
C6603	5B4	2294.0100	CAP MICA 500V 5%	10pF
C6604	5B4	2294.0100	CAP MICA 500V 5%	10pF
C6801	4A7	2296.0101	CAP MICA 500V 1%	100pF
C6802	4E7	2296.0101	CAP MICA 500V 1%	100pF
C7001	7B9	2172.0104	CAP CERAM 100V 20%	.1uF
C7201	8D4	2296.0101	CAP MICA 500V 1%	100pF
C7302	8C2	2172.0104	CAP CERAM 100V 20%	.1uF
C7401	6D1	2172.0104	CAP CERAM 100V 20%	.1uF
C7402	6E1	2172.0104	CAP CERAM 100V 20%	.1uF
C7501	5B7	2675.0334	CAP POLYC 100V 2%	.33uF
C7701	4D8	2296.0471	CAP MICA 500V 1%	470pF
C7702	4D8	2296.0181	CAP MICA 500V 1%	180pF
C8001	7C8	2822.0686	CAP TA-EL 16V 20%	68uF
C8002	7C9	2294.0270	CAP MICA 500V 5%	27pF
C8003	7C9	2294.0270	CAP MICA 500V 5%	27pF
C8004	7C8	2952.0105	CAP AL-EL 50V 20%	1uF
C8201	8A3	2172.0104	CAP CERAM 100V 20%	.1uF
C8301	8B3	2172.0104	CAP CERAM 100V 20%	.1uF
C8302	8B4	2952.0105	CAP AL-EL 50V 20%	1uF
C8401	6B6	2294.0470	CAP MICA 500V 5%	47pF
C8402	6C6	2822.0686	CAP TA-EL 16V 20%	68uF
C8501	5D7	2296.0471	CAP MICA 500V 1%	470pF
C8601	5B3	2932.0476	CAP AL-EL 25V 20%	47uF
C8701	4C8	2294.0270	CAP MICA 500V 5%	27pF
C8702	4C8	2294.0100	CAP MICA 500V 5%	10pF
C8703	4B8	2296.0471	CAP MICA 500V 1%	470pF
C8704	4A8	2296.0181	CAP MICA 500V 1%	180pF
C8801	4A7,4D7	2694.0105.M	CAP POLYC 250V .25% MATCH	1uF
C9401	6E2	2932.0476	CAP AL-EL 25V 20%	47uF

Board Loc.	Schematic Loc.	Part Number	Description	
C9402	6D2	2932.0476	CAP AL-EL 25V 20%	47uF
C9403	6B6	2932.0476	CAP AL-EL 25V 20%	47uF
C9404	6C5	2932.0476	CAP AL-EL 25V 20%	47uF
C9405	6B6	4450.0250	VAR CAP PC	5-25pF
C9701	4C8	4450.0250	VAR CAP PC	5-25pF
D1801	4F1	3120.0000	DIODE SCHOTTKY	1SS97
D2801	4G5	3110.4152	DIODE SIGNAL	4152
D2802	4F3	3110.4152	DIODE SIGNAL	4152
D2803	4G6	3110.4152	DIODE SIGNAL	4152
D2804	4E9	3110.4152	DIODE SIGNAL	4152
D2805	4F9	3110.4152	DIODE SIGNAL	4152
D2806	4G10	3110.4152	DIODE SIGNAL	4152
D2807	5F3	3110.4152	DIODE SIGNAL	4152
D2808	5F5	3110.4152	DIODE SIGNAL	4152
D2809	5F8	3110.4152	DIODE SIGNAL	4152
D2901	4E3	3110.4152	DIODE SIGNAL	4152
D4001	2H7	3120.0000	DIODE SCHOTTKY	1SS97
D4401	3B4	3110.4152	DIODE SIGNAL	4152
D4402	3A4	3110.4152	DIODE SIGNAL	4152
D4403	3B3	3110.4152	DIODE SIGNAL	4152
D4404	3B3	3110.4152	DIODE SIGNAL	4152
D5101	7C4	3110.4152	DIODE SIGNAL	4152
D5102	7C4	3110.4152	DIODE SIGNAL	4152
D5601	5D2	3110.4152	DIODE SIGNAL	4152
D5602	5D2	3110.4152	DIODE SIGNAL	4152
D5603	5C1	3110.4152	DIODE SIGNAL	4152
D5604	5C2	3110.4152	DIODE SIGNAL	4152
D5605	5C1	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D5606	5C2	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D5607	5C2	3110.4152	DIODE SIGNAL	4152
D5608	5C1	3110.4152	DIODE SIGNAL	4152
D5609	5B2	3110.4152	DIODE SIGNAL	4152
D5610	5B2	3110.4152	DIODE SIGNAL	4152
D6301	8F5	3120.0000	DIODE SCHOTTKY	1SS97
D6302	8F5	3120.0000	DIODE SCHOTTKY	1SS97
D7201	8C4	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
D7301	8C2	3120.0000	DIODE SCHOTTKY	1SS97
D7302	8C3	3120.0000	DIODE SCHOTTKY	1SS97
D8301	8B4	3110.4152	DIODE SIGNAL	4152
D8401	6C1	3110.4152	DIODE SIGNAL	4152
D8402	6E2	3110.4152	DIODE SIGNAL	4152
E011	---	4232.1028	SOCKET IC WIDE	28 PIN
E471	---	4261.0001	FUSE CLIP PC	
E472	---	4261.0001	FUSE CLIP PC	
E681	---	4132.0155	CABLE 2 COND SHLD 15.5	3 PIN
E761	---	4232.0008	SOCKET IC DIP	8 PIN
E762	---	4232.0008	SOCKET IC DIP	8 PIN
E822	---	4232.0014	SOCKET IC DIP	14 PIN
ECB01	---	6200.LVF1	ECB 2 LAYER 6 X15	LVF
I471	4A9	4700.4840	LAMP INCANDESCENT 48V	40mA
I472	4D9	4700.4840	LAMP INCANDESCENT 48V	40mA

Replaceable Electrical Parts List LVF-1

Board Loc.	Schematic Loc.	Part Number	Description	
J031	2C10	4221.1020	JACK PC 2 X .1	20 PIN
J051	1A10,2A10,3C1	4221.1024	JACK PC 2 X .1	24 PIN
J231	8A10,8G5	4221.1006	JACK PC .1	6 PIN
J401	1A1	4151.1740	CABLE ASSY .05 RBN 17	40 COND
J461	5A10	4221.1008	JACK PC 2 X .1	8 PIN
J621	8F10	4221.1006	JACK PC .1	6 PIN
J801	7D2	4221.1008	JACK PC 2 X .1	8 PIN
J811	7C2	4221.1008	JACK PC 2 X .1	8 PIN
J812	7C2	4221.1008	JACK PC 2 X .1	8 PIN
J813	7C2	4221.1008	JACK PC 2 X .1	8 PIN
J951	6A1	4221.1008	JACK PC 2 X .1	8 PIN
K481	4F5	4530.0001	RELAY PC	DPDT
K571	4F10	4530.0001	RELAY PC	DPDT
K572	4F9	4530.0001	RELAY PC	DPDT
K581	4G6	4530.0001	RELAY PC	DPDT
K591	4E3	4530.0001	RELAY PC	DPDT
K651	5F8	4530.0001	RELAY PC	DPDT
K671	5E3	4530.0001	RELAY PC	DPDT
K672	4E9	4530.0001	RELAY PC	DPDT
K771	5F5	4530.0001	RELAY PC	DPDT
K891	4F3	4530.0001	RELAY PC	DPDT
P681	4C6	4221.0036	PLUG PC .1 X.43	36 PIN
P921	7F10	4221.0036	PLUG PC .1 X.43	36 PIN
P922	7E10	4221.0036	PLUG PC .1 X.43	36 PIN
P941	6B2	4221.0036	PLUG PC .1 X.43	36 PIN
P942	6C2	4221.0036	PLUG PC .1 X.43	36 PIN
P951	5D10	4221.0036	PLUG PC .1 X.43	36 PIN
P952	5C10	4221.0036	PLUG PC .1 X.43	36 PIN
P991	4A2	4221.0036	PLUG PC .1 X.43	36 PIN
Q3801	4G4	3211.2222	XSTR NPN TO92	PN2222A
Q3802	4F3	3211.2222	XSTR NPN TO92	PN2222A
Q3803	4G6	3211.2222	XSTR NPN TO92	PN2222A
Q3804	4E8	3211.2222	XSTR NPN TO92	PN2222A
Q3805	4F8	3211.2222	XSTR NPN TO92	PN2222A
Q3806	4G9	3211.2222	XSTR NPN TO92	PN2222A
Q3807	5E3	3211.2222	XSTR NPN TO92	PN2222A
Q3808	5F4	3211.2222	XSTR NPN TO92	PN2222A
Q3809	5F7	3211.2222	XSTR NPN TO92	PN2222A
Q3901	4E2	3211.2222	XSTR NPN TO92	PN2222A
Q4101	1F3	3211.2222	XSTR NPN TO92	PN2222A
Q4401	8F8	3211.2222	XSTR NPN TO92	PN2222A
Q4402	3B2	3214.4091	XSTR FET TO92	PN4091
Q6301	8F7	3211.2222	XSTR NPN TO92	PN2222A
R0401	8E10	4412.0201	POT TRIM PC ENC	200
R0501	2B9	1214.0472	RES 1/4W C FLM 5%	4.7K
R1001	2E3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R1301	2D7	1214.0103	RES 1/4W C FLM 5%	10K
R1302	2B9	1214.0472	RES 1/4W C FLM 5%	4.7K
R1303	2B9	1214.0472	RES 1/4W C FLM 5%	4.7K
R2501	3B6	1214.0472	RES 1/4W C FLM 5%	4.7K

Board Loc.	Schematic Loc.	Part Number	Description	
R2502	3A6	1214.0472	RES 1/4W C FLM 5%	4.7K
R2503	2A9	1214.0102	RES 1/4W C FLM 5%	1K
R2601	3G9	1214.0303	RES 1/4W C FLM 5%	30K
R261	3D9,3E3,3E7,6F3	1984.9103	RES NET SIP 5%	9 X 10K
R2801	4G4	1214.0272	RES 1/4W C FLM 5%	2.7K
R2802	4E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2803	4G5	1214.0272	RES 1/4W C FLM 5%	2.7K
R2804	4E8	1214.0272	RES 1/4W C FLM 5%	2.7K
R2805	4F8	1214.0272	RES 1/4W C FLM 5%	2.7K
R2806	4G8	1214.0272	RES 1/4W C FLM 5%	2.7K
R2807	5E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2808	5F4	1214.0272	RES 1/4W C FLM 5%	2.7K
R2809	5F6	1214.0272	RES 1/4W C FLM 5%	2.7K
R2901	4E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R3101	1F3	1214.0203	RES 1/4W C FLM 5%	20K
R321	8F3	1984.9103	RES NET SIP 5%	9 X 10K
R3301	8D8	1136.2212	RES 1/8W M FLM 1%	22.1K
R3302	8A7	1214.0472	RES 1/4W C FLM 5%	4.7K
R3303	8A8	1214.0103	RES 1/4W C FLM 5%	10K
R3304	8A7	1214.0472	RES 1/4W C FLM 5%	4.7K
R3401	8B10	1214.0102	RES 1/4W C FLM 5%	1K
R3402	8D10	1136.2671	RES 1/8W M FLM 1%	2.67K
R3403	8D10	1136.2552	RES 1/8W M FLM 1%	25.5K
R341	3A5,3B2,3B5,3C3,3C8	1984.9103	RES NET SIP 5%	9 X 10K
R3501	3B8	1214.0752	RES 1/4W C FLM 5%	7.5K
R3502	3E3	1214.0303	RES 1/4W C FLM 5%	30K
R3503	3F3	1214.0303	RES 1/4W C FLM 5%	30K
R3504	3E7	1214.0303	RES 1/4W C FLM 5%	30K
R3601	3F7	1214.0303	RES 1/4W C FLM 5%	30K
R421	6E7	1984.9103	RES NET SIP 5%	9 X 10K
R4301	8C7	1136.2431	RES 1/8W M FLM 1%	2.43K
R4302	8F7	1214.0472	RES 1/4W C FLM 5%	4.7K
R4401	8D10	1214.0100	RES 1/4W C FLM 5%	10
R4402	8B10	1214.0100	RES 1/4W C FLM 5%	10
R4403	3B6	1214.0623	RES 1/4W C FLM 5%	62K
R4404	3A6	1214.0623	RES 1/4W C FLM 5%	62K
R4405	3A5	1214.0101	RES 1/4W C FLM 5%	100
R4406	3B5	1214.0101	RES 1/4W C FLM 5%	100
R4407	3A4	1214.0102	RES 1/4W C FLM 5%	1K
R4408	3A2	1214.0472	RES 1/4W C FLM 5%	4.7K
R4501	3G3	1136.1002	RES 1/8W M FLM 1%	10.0K
R4502	3G2	1136.1002	RES 1/8W M FLM 1%	10.0K
R4503	3G6	1136.7870	RES 1/8W M FLM 1%	787
R4504	3G5	1136.7870	RES 1/8W M FLM 1%	787
R4505	3G6	1136.3320	RES 1/8W M FLM 1%	332
R4506	3G6	1136.3320	RES 1/8W M FLM 1%	332
R4507	3G7	1136.2210	RES 1/8W M FLM 1%	221
R4508	3G7	1136.2210	RES 1/8W M FLM 1%	221
R4509	3G7	1214.0750	RES 1/4W C FLM 5%	75
R4510	3H7	1214.0750	RES 1/4W C FLM 5%	75
R4511	3D3	1136.4991	RES 1/8W M FLM 1%	4.99K
R4512	3D2	1136.4991	RES 1/8W M FLM 1%	4.99K
R4601	5G5	1214.0100	RES 1/4W C FLM 5%	10
R4602	5G6	1214.0100	RES 1/4W C FLM 5%	10

Replaceable Electrical Parts List LVF-1

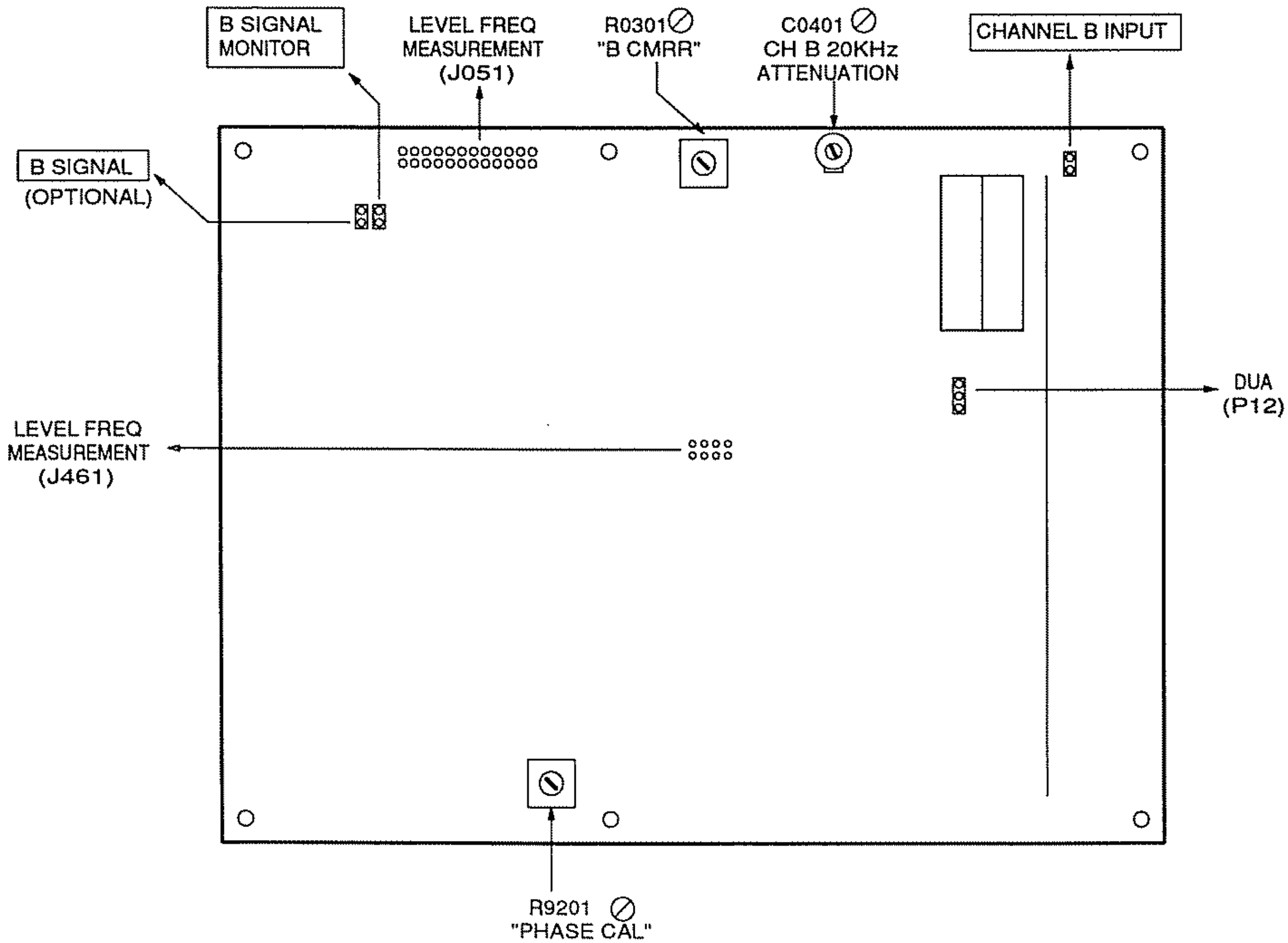
Board Loc.	Schematic Loc.	Part Number	Description	
R4901	4E1	1214.0103	RES 1/4W C FLM 5%	10K
R4902	4C3	1136.1509	RES 1/8W M FLM 1%	15.0
R5001	7B8	1136.1002	RES 1/8W M FLM 1%	10.0K
R5101	7C7	1214.0101	RES 1/4W C FLM 5%	100
R5102	7C4	1214.0471	RES 1/4W C FLM 5%	470
R5301	8F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R5302	8C5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5303	8C5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5304	8C5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5305	8C5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5306	8D5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5307	8D5	1214.0472	RES 1/4W C FLM 5%	4.7K
R5308	8F7	1214.0472	RES 1/4W C FLM 5%	4.7K
R5501	5E8	1139.3330	RES 1/8W M FLM .1%	333.3
R5502	5E8	1139.1001	RES 1/8W M FLM .1%	1.00K
R5503	5F8	1214.0103	RES 1/4W C FLM 5%	10K
R5504	5C7	1136.7501	RES 1/8W M FLM 1%	7.50K
R5505	5C7	1136.5491	RES 1/8W M FLM 1%	5.49K
R5506	5C7	1136.7501	RES 1/8W M FLM 1%	7.50K
R5601	5C1	1214.0272	RES 1/4W C FLM 5%	2.7K
R5602	5C2	1214.0272	RES 1/4W C FLM 5%	2.7K
R6001	7B10	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R6002	7B8	1214.0226	RES 1/4W C FLM 5%	22M
R601	1E3	1984.9472	RES NET SIP 5%	9 X 4.7K
R6100	7C7	1214.0823	RES 1/4W C FLM 5%	82K
R6101	7A5	1214.0823	RES 1/4W C FLM 5%	82K
R6201	7B3	1136.4990	RES 1/8W M FLM 1%	499
R6202	8C3	1214.0165	RES 1/4W C FLM 5%	1.6M
R6301	8F6	1214.0304	RES 1/4W C FLM 5%	300K
R6302	8F6	1214.0152	RES 1/4W C FLM 5%	1.5K
R6401	6C10	1139.2001	RES 1/8W M FLM .1%	2.00K
R6402	6D7	1136.2671	RES 1/8W M FLM 1%	2.67K
R6403	6D7	1136.1582	RES 1/8W M FLM 1%	15.8K
R6404	6D8	1136.3571	RES 1/8W M FLM 1%	3.57K
R6405	6C7	1136.4641	RES 1/8W M FLM 1%	4.64K
R6406	6C7	1136.4122	RES 1/8W M FLM 1%	41.2K
R6407	6C8	1136.5621	RES 1/8W M FLM 1%	5.62K
R6408	6B7	1136.1781	RES 1/8W M FLM 1%	1.78K
R6409	6B7	1136.1582	RES 1/8W M FLM 1%	15.8K
R6410	6B8	1136.1821	RES 1/8W M FLM 1%	1.82K
R6411	6A8	1136.1652	RES 1/8W M FLM 1%	16.5K
R6412	6A7	1136.1431	RES 1/8W M FLM 1%	1.43K
R6501	5E7	1214.0223	RES 1/4W C FLM 5%	22K
R6601	5D3	1139.1001	RES 1/8W M FLM .1%	1.00K
R6602	5D4	1214.0103	RES 1/4W C FLM 5%	10K
R6603	5E2	1214.0470	RES 1/4W C FLM 5%	47
R6604	5A2	1214.0470	RES 1/4W C FLM 5%	47
R6605	5B4	1214.0103	RES 1/4W C FLM 5%	10K
R6606	5B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R6701	5C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R6801	4A7	1136.2210	RES 1/8W M FLM 1%	221
R6802	4D7	1136.2210	RES 1/8W M FLM 1%	221
R7001	7B10	1214.0221	RES 1/4W C FLM 5%	220
R7100	7D7	1214.0273	RES 1/4W C FLM 5%	27K

Board Loc.	Schematic Loc.	Part Number	Description	
R7101	7B6	1136.1783	RES 1/8W M FLM 1%	178K
R7102	7B5	1136.3832	RES 1/8W M FLM 1%	38.3K
R7103	7B5	1136.7681	RES 1/8W M FLM 1%	7.68K
R7104	7C6	1136.8062	RES 1/8W M FLM 1%	80.6K
R7105	7C5	1136.4321	RES 1/8W M FLM 1%	4.32K
R7106	7C5	1136.1132	RES 1/8W M FLM 1%	11.3K
R7107	7D6	1136.6042	RES 1/8W M FLM 1%	60.4K
R7108	7D5	1136.3241	RES 1/8W M FLM 1%	3.24K
R7109	7D5	1136.8451	RES 1/8W M FLM 1%	8.45K
R7201	7E8	1139.2001	RES 1/8W M FLM .1%	2.00K
R7202	7E8	1139.2001	RES 1/8W M FLM .1%	2.00K
R7203	7F9	1214.0470	RES 1/4W C FLM 5%	47
R7204	8D4	1214.0114	RES 1/4W C FLM 5%	110K
R7205	8C4	1136.2261	RES 1/8W M FLM 1%	2.26K
R7206	8C4	1136.2261	RES 1/8W M FLM 1%	2.26K
R7207	8D3	1139.4001	RES 1/8W M FLM .1%	4.00K
R7208	8C2	1139.2001	RES 1/8W M FLM .1%	2.00K
R7209	8C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R7301	8C3	1139.2001	RES 1/8W M FLM .1%	2.00K
R7401	6C10	1139.2001	RES 1/8W M FLM .1%	2.00K
R7402	6C10	1136.1622	RES 1/8W M FLM 1%	16.2K
R7403	6B5	1214.0100	RES 1/4W C FLM 5%	10
R7404	6C5	1214.0100	RES 1/4W C FLM 5%	10
R7405	6C4	1139.3330	RES 1/8W M FLM .1%	333.3
R7406	6C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7407	6B4	1139.4001	RES 1/8W M FLM .1%	4.00K
R7501	5E6	1139.2001	RES 1/8W M FLM .1%	2.00K
R7502	5E5	1139.2001	RES 1/8W M FLM .1%	2.00K
R7503	5B5	1139.1001	RES 1/8W M FLM .1%	1.00K
R7601	5D4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7602	5D4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7603	5B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7604	5B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R7701	4C7	1139.1671	RES 1/8W M FLM .1%	1.667K
R7702	4D7	1139.5001	RES 1/8W M FLM .1%	5.00K
R7703	4D7	1139.2002	RES 1/8W M FLM .1%	20.0K
R7704	4D7	1139.8002	RES 1/8W M FLM .1%	80.0K
R7705	4E7	1214.0165	RES 1/4W C FLM 5%	1.6M
R7901	4C3	1656.2000	RES 3W W WND 1%	200
R7902	4B4	1136.2802	RES 1/8W M FLM 1%	28.0K
R7903	4C3	1656.3000	RES 3W W WND 1%	300
R7904	4C3	1656.3000	RES 3W W WND 1%	300
R8001	7C9	1139.5001	RES 1/8W M FLM .1%	5.00K
R8002	7C9	1139.5001	RES 1/8W M FLM .1%	5.00K
R8003	7C8	1139.1001	RES 1/8W M FLM .1%	1.00K
R8101	7D9	1136.1783	RES 1/8W M FLM 1%	178K
R8102	7D9	1214.0274	RES 1/4W C FLM 5%	270K
R8201	7E9	1214.0561	RES 1/4W C FLM 5%	560
R8301	8A2	1214.0204	RES 1/4W C FLM 5%	200K
R8302	8B4	1214.0102	RES 1/4W C FLM 5%	1K
R8303	8B4	1214.0472	RES 1/4W C FLM 5%	4.7K
R8304	8C2	1214.0275	RES 1/4W C FLM 5%	2.7M
R8401	6D2	1136.2740	RES 1/8W M FLM 1%	274
R8402	6D2	1136.1101	RES 1/8W M FLM 1%	1.10K

Replaceable Electrical Parts List LVF-1

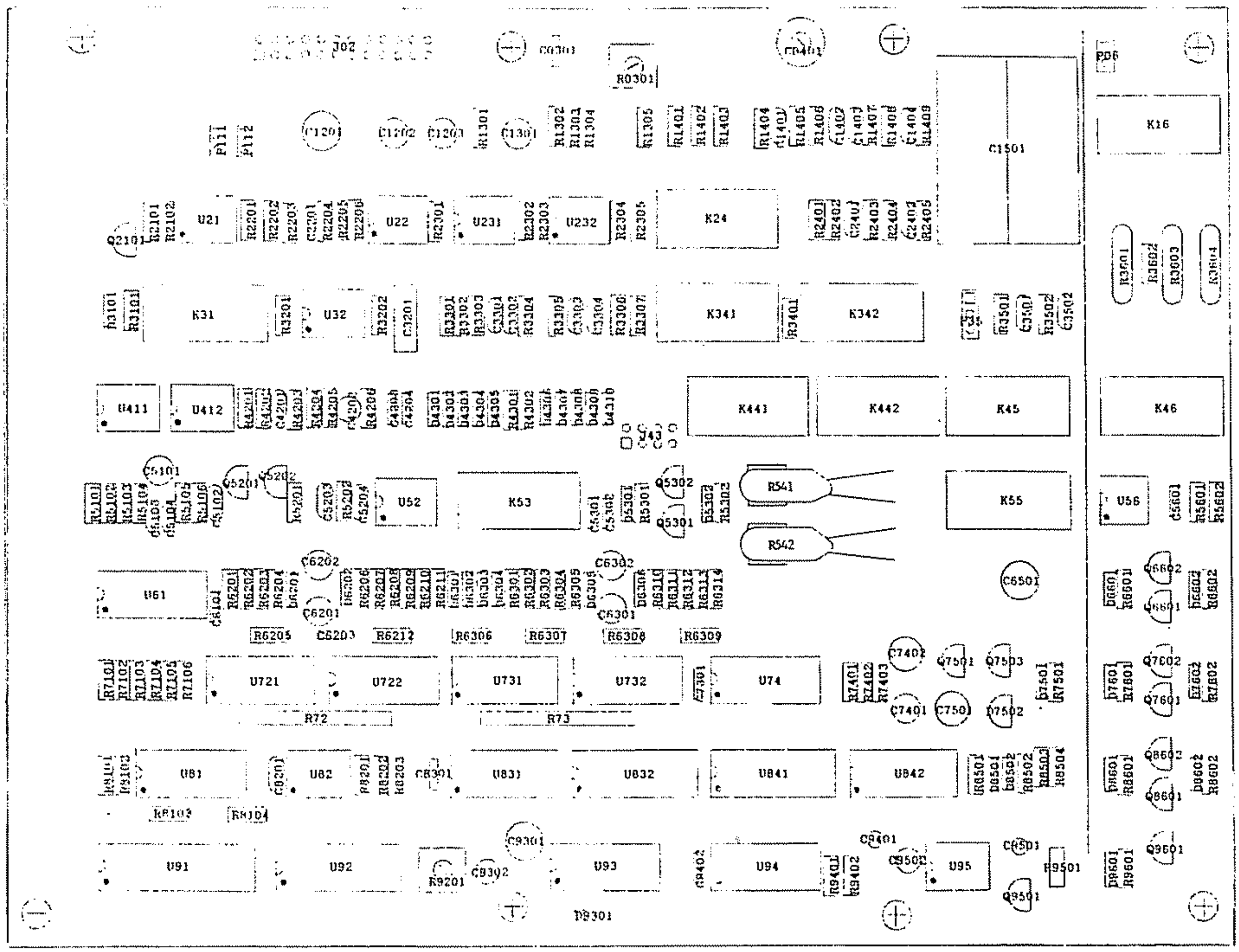
Board Loc.	Schematic Loc.	Part Number	Description	
R8403	6D2	1136.1101	RES 1/8W M FLM 1%	1.10K
R8404	6E2	1136.2740	RES 1/8W M FLM 1%	274
R8405	6C6	1214.0103	RES 1/4W C FLM 5%	10K
R8406	6B6	1139.9981	RES 1/8W M FLM .1%	9.98K
R8407	6C6	1139.1001	RES 1/8W M FLM .1%	1.00K
R8408	6C3	1136.2219	RES 1/8W M FLM 1%	22.1
R8409	6B3	1139.3330	RES 1/8W M FLM .1%	333.3
R8410	6B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R8411	6B3	1139.4001	RES 1/8W M FLM .1%	4.00K
R8412	6A4	1214.0102	RES 1/4W C FLM 5%	1K
R8414	6C2	1214.0102	RES 1/4W C FLM 5%	1K
R8501	5D10	1214.0470	RES 1/4W C FLM 5%	47
R8502	5C10	1214.0561	RES 1/4W C FLM 5%	560
R8503	5D8	1139.2001	RES 1/8W M FLM .1%	2.00K
R8504	5D8	1139.2001	RES 1/8W M FLM .1%	2.00K
R8505	5D7	1214.0270	RES 1/4W C FLM 5%	27
R8506	5D6	1214.0101	RES 1/4W C FLM 5%	100
R8507	5C6	1136.1002	RES 1/8W M FLM 1%	10.0K
R8508	5B5	1139.1001	RES 1/8W M FLM .1%	1.00K
R8601	5E3	1214.0226	RES 1/4W C FLM 5%	22M
R8602	5D3	1214.0273	RES 1/4W C FLM 5%	27K
R8603	5C3	1214.0103	RES 1/4W C FLM 5%	10K
R8604	5B3	1214.0226	RES 1/4W C FLM 5%	22M
R8605	5B6	1214.0104	RES 1/4W/C/FLM 5%	100K
R8606	5B5	1136.1002	RES 1/8W M FLM 1%	10.0K
R8704	4B8	1214.0474	RES 1/4W C FLM 5%	470K
R8705	4B7	1139.1671	RES 1/8W M FLM .1%	1.667K
R8706	4B7	1139.5001	RES 1/8W M FLM .1%	5.00K
R8707	4B7	1139.2002	RES 1/8W M FLM .1%	20.0K
R8708	4A7	1139.8002	RES 1/8W M FLM .1%	80.0K
R8709	4A8	1214.0165	RES 1/4W C FLM 5%	1.6M
R9001	7A5	4412.0503	POT TRIM PC ENC	50K
R9101	7B8	4412.0503	POT TRIM PC ENC	50K
R9102	7D9	4412.0503	POT TRIM PC ENC	50K
R9103	8D4	4412.0503	POT TRIM PC ENC	50K
R9201	8C3	4412.0503	POT TRIM PC ENC	50K
R9202	8A2	4412.0503	POT TRIM PC ENC	50K
R9203	8C4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R9301	8D2	4412.0503	POT TRIM PC ENC	50K
R9601	5B6	4412.0503	POT TRIM PC ENC	50K
S801	1F4	4310.0004	SWITCH DIP	4 POLE
U011	2C3	3331.6805	uPROCESSOR EPROM	68705P3
U021	2B5	3332.8254	TIMER INTERVAL PROG	82C54
U022	2B9	3332.8254	TIMER INTERVAL PROG	82C54
U101	1B2	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U111	1B3	3313.0670	REGISTER FILE 4X4	74LS670
U112	1B9	3313.0670	REGISTER FILE 4X4	74LS670
U121	2B2,2B3,2C2,2C6	3323.0390	COUNTER 2 X 4-BIT DEC	74HC390
U131	1E5,2A8,2B6,2C7	3324.0240	BUFFER 8X INV TRI-ST	74HCT240
U141	1E9	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U142	2E9	3313.0138	DECODER 3-LINE/8-LINE	74LS138
U151	3C10	3313.0244	BUFFER 8X TRI-STATE	74LS244

Board Loc.	Schematic Loc.	Part Number	Description	
U171	6F2	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U181	1G9,4F2	3313.0074	FLIP-FLOP 2X J-K	74LS74
U182	5F2	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U211	1B5	3313.0670	REGISTER FILE 4X4	74LS670
U212	1C3	3313.0670	REGISTER FILE 4X4	74LS670
U221	1E6	3313.0155	DECODER 2 X 2-LN/4-LN	74LS155
U241	1F8,2G6	3313.0139	DECODER 2 X 2-LN/4-LN	74LS139
U242	2E5	3313.0138	DECODER 3-LINE/8-LINE	74LS138
U251	2B7,3A7	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U261	3E4,3F4	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U271	3E8,3F8	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U311	1B7	3313.0670	REGISTER FILE 4X4	74LS670
U312	1C5	3313.0670	REGISTER FILE 4X4	74LS670
U321	8G2	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U331	8B8	3321.4051	MULTIPLEX 8X	4051
U332	8B9	3412.0353	OP AMP DUAL	TL072/LF353
U341	8C10	3441.0654	CONVERTER VOLT TO FREQ	AD654J
U342	3A5,3B5	3422.0319	COMPARATOR DUAL HI-SPD	LM319
U351	3E2,3F2,3G2	3424.0339	COMPARATOR QUAD	LM339
U361	3E6,3F6,3G6	3424.0339	COMPARATOR QUAD	LM339
U371	3C2,3G8,3H8,3H9	3424.0339	COMPARATOR QUAD	LM339
U411	1C9	3313.0670	REGISTER FILE 4X4	74LS670
U412	1C7	3313.0670	REGISTER FILE 4X4	74LS670
U421	6E6	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U431	8A6	3321.4052	MULTIPLEX 4X DIFF	4052
U491	4C4	3630.0001	OPTO-ISOLATOR	H11AA1
U511	7B6	3321.4052	MULTIPLEX 4X DIFF	4052
U512	7B4,7B7	3412.0353	OP AMP DUAL	TL072/LF353
U521	7B3	3321.4051	MULTIPLEX 8X	4051
U541	6C10,6D8	3412.0353	OP AMP DUAL	TL072/LF353
U542	6B9	3321.4052	MULTIPLEX 4X DIFF	4052
U543	6B8,6C8	3412.0353	OP AMP DUAL	TL072/LF353
U544	3A3,6A8	3412.5532	OP AMP DUAL	5532
U551	5E8	3411.5534	OP AMP SINGLE	5534A
U601	1E2	3313.0085	COMPARATOR 4-BIT MAG	74LS85
U621	8C4	3411.0318	OP AMP SINGLE	LM318
U622	8F5	3411.0318	OP AMP SINGLE	LM318
U651	5C6	3412.5532	OP AMP DUAL	5532
U701	7B9	3411.5534	OP AMP SINGLE	5534A
U731	8C2	3411.0318	OP AMP SINGLE	LM318
U741	6B5	3411.5534	OP AMP SINGLE	5534A
U742	6B5	3321.4051	MULTIPLEX 8X	4051
U751	5C9,5D9	3412.5532	OP AMP DUAL	5532
U752	5D6	3411.5534	OP AMP SINGLE	5534A
U761	5E4	3411.5534	OP AMP SINGLE	5534A
U762	5A4	3411.5534	OP AMP SINGLE	5534A
U821	7E9,7F9	3412.5532	OP AMP DUAL	5532
U822	8B3	3441.0637	CONVERTER RMS TO DC	AD637J
U841	6C1	3430.1317	VOLT REG POS VAR TO92	LM317L
U842	6E1	3431.1337	VOLT REG NEG VAR TO92	LM337L
X90	---	7160.0002	SHIELD ECB INPUT	



PHA-1

DUAL INPUT/PHASEMETER
(S/N 10001-10299 ONLY)



DUAL INPUT ANALYZER & PHASE OPTION 9PHA.1000 (6200.PHA1.6)

PHA-1, DUAL INPUT / PHASEMETER

The PHA-1 circuit board mounts to the LVF-1 module and adds a second autoranging input channel and phasemeter to the System One analyzer. The functional circuits on the board include the input attenuators, input preamplifier, range comparators, and phasemeter.

Input Circuit <1>

The input signal is derived from the front panel connectors or the internal generator monitor interconnection via relays K45 and K55. Relays K45 and K55 are ganged together to provide optimum input isolation when monitoring the generator output. P35 connects to a shielded cable originating on the B output of the generator.

Relay K16 selects the 600 Ohm and 150 Ohm terminations. Its control bit originates from the Q output of flip-flop U93A. When a termination is selected the flip-flop Q output clocks high and causes relay K16 to be energized through Q6601. Relay K46 provides 600/150 Ohm selection. In the 600 Ohm selection, relay K46 is open and the termination is composed of resistors R3602-R3604 and R5602. R3601 shunts the 600 Ohm termination to obtain the 150 Ohm termination (300 Ohms if option **EURZ** is installed). The terminations are protected against excessive power dissipation by sensing a small portion of the total input voltage through the divider action of R3603, R3604, and R5602 and the ac optocoupler U56. An input level greater than approximately +32 dBu (30 Vrms) will forward bias the light-emitting diodes inside U56. This causes the phototransistor inside U56 to conduct, clearing the control flip-flop U93A and de-energizing relay K16.

The selected input signal passes through RF suppression filters composed of R3501, C3501, R3502, and C3502. In some units C3501 or C3502 may be shunted with a small capacitor to balance the total input capacitance. The signal is then ac-coupled to the input attenuators through C1501 and C1502. C1501 and C1502 are ratio matched for optimum low frequency common mode rejection.

The input attenuators provide four 12 dB steps from 0 dB to -36 dB. Relay K441 is energized in the 0 dB state, K442 for -12 dB, and K342 for -24 dB. -36 dB is the default state with all three relays off. Refer to TABLE PHA1.1 more information concerning attenuator step selection versus input voltage. C0401 adjusts the attenuator high frequency flatness above approximately 10 kHz. R1409 and R2405 trim the total input resistance to be 100 kOhms, each side to ground.

Signal Preamp <2>

The selected and attenuated input signal is buffered and amplified by U232, U231, U22, and U412. Diodes D4301-4304, and D4307-4310 provide overload protection by clamping the op-amp input voltage to approximately ±13 V, determined by zener diodes D4305 and D4306. High frequency distortion due to the non-linear capacitance of the diodes is minimized by the inherent bootstrap action of this configuration.

NOTE: The residual leakage current of the input clamping diodes can exhibit significant optical modulation. Exposure to fluorescent lighting with the top cover removed may cause an increase in input hum products due to this effect!

When no attenuation has been selected the incandescent lamps R541 and R542, located on schematic <1>, limit input current during an overload condition. Normally the lamps are cold and present a low resistance (typically 100-130 Ohms) to the input circuit. During an overload the lamp resistance rises dramatically.

The pre-amplifier gain is controlled by relays K341 and K24, providing +12 dB and +6 dB steps respectively. If both are energized the preamp gain is +18 dB. K31 switches an additional +12 dB gain stage comprising U412, R4201, and R4202 for higher sensitivity. See TABLE PHA1.1 or more information concerning pre-amplifier gain states versus input voltage.

U22 is a unity gain differential input to single ended output amplifier. Common mode rejection is trimmed by R0301 which balances the + and - input signal path gains. U32A and its related components comprise a dc servo that maintains a near zero dc offset condition at the output of U22 under all gain conditions. The output of the servo integrator is feedback through R3202 into the + signal path. C4202 and R4205 provide low frequency compensation that corrects for the input ac coupling rolloff below about 30 Hz.

The output signal from relay K31 is labeled BSIG and is routed several places. It is connected to the channel B input ranging comparators shown on schematic <3>, to K53, and to the BSIG monitor buffers U21A and U21B. The output from U21A is coupled through R2102 and a shielded cable to the front panel CHANNEL B MONITOR connector. Note that there is a 6 dB loss introduced by R2201 and R2202. U21B provides the buffered BSIG for routing to the DSP module in SYS-2xx and SYS-3xx configurations. Under normal autoranging conditions BSIG will vary over a 6-7 dB window between approximately 1.60-3.75 Vpeak.

TABLE PHA1.1
CHANNEL-B INPUT RANGES & SYSTEM GAIN

RANGE[1]	ATTENUATION	K441	K442	K342	PREAMP GAIN	K24	K341	K31	TOTAL GAIN[2]
160 V[3]	-36dB	0	0	0	0dB	0	0	0	-36dB
80 V	-36dB	0	0	0	+6dB	1	0	0	-30dB
40 V	-24dB	0	0	1	0dB	0	0	0	-24dB
20 V	-24dB	0	0	1	+6dB	1	0	0	-18dB
10 V	-12dB	0	1	0	0dB	0	0	0	-12dB
5 V	-12dB	0	1	0	+6dB	1	0	0	-6dB
2.5 V	0dB	1	0	0	0dB	0	0	0	0dB
1.2 V	0dB	1	0	0	+6dB	1	0	0	+6dB
600 mV	0dB	1	0	0	+12dB	0	1	0	+12dB
300 mV	0dB	1	0	0	+18dB	1	1	0	+18dB
160 mV	0dB	1	0	0	+24dB	0	1	1	+24dB
80 mV	0dB	1	0	0	+30dB	1	1	1	+30dB

1 Maximum rms sinewave amplitude for linear operation.
2 INPUT to BSIG
3 140 Vrms is the maximum rated input voltage

K53 controls whether ASIG (supplied through J43-6) or BSIG is routed to J43-8 to become the MAINSIG. K53 is off for channel A, on for channel B.

Autorange Comparators <3>

The signal from the B channel input amplifier is fed through the preemphasis network R5101, R5106, C5102. This compensates for the slew rate limitations of the op-amps in the preamplifier, reducing amplitude of signal at high frequencies before an up-range occurs. This signal feeds four comparators, two sense the need to up-range and two sense the need to downrange. The two comparators in each pair are used to sense the positive peak value and negative peak value of the signal.

Consider the operation of U61A. Its negative input is connected to the signal input and its positive input is connected to a +1.75V reference. The output of the comparator will go low when positive signal peak exceeds this reference. U61B performs the same comparison function for negative peaks. The outputs of the two comparators are wired together. Since these are open collector outputs, if either comparator senses too large a peak value the output line will go low. R8101 and R8104 level shift the -15 V output of the comparators to the +5 V logic of U81. When the comparator output goes low it will set the flip-flop U81A. The microprocessor on the LVF-1 board reads the output of this flip-flop through tri-state buffer U91 and knows if an overrange condition occurred. When the microprocessor reads this information the clock input of U81 is strobed, clearing the overrange indication. The flip-flop allows momentary signal overloads to be detected with infrequent monitoring by the microprocessor.

Comparators U61C and U61D perform the same comparison function on the signal at a 6 dB lower amplitude. If the signal is below this level the microprocessor knows that the input gain must be increased. When the correct input range is achieved the upper comparator output will be high and the lower comparator output will be low. Any change of state in the comparators causes an uprange or downrange as appropriate.

Comparators U411A and U411B monitor the signal level against a 100 mV reference. This is used to sense when the signal is of insufficient amplitude to guarantee accurate phasemeter operation. When this occurs the output of the comparators will rise. This signal must remain under this minimum level until C5101 charges for the processor to shut down the phasemeter reading.

Tri-state buffer U91 allows the microprocessor to read the state of various logic signals on the phasemeter board. In addition to the three range comparison signals described above, the state of the Channel B input termination resistors (/TERM B) and a ranging signal (PHASEN) from the phasemeter are monitored.

Phasemeter <4>

The phasemeter is shown in FIGURE PHA1.1. The Channel A and Channel B signals enter through R5202 and R5201. When line LB goes to 0 V, JFET switches Q5202 and Q5201 connect the capacitors C5203 and C5204 to ground. These form lowpass filter circuits which reduce the interfering effects of noise components greater than approximately 100 kHz. These signals are buffered by U52 which drives the comparators and peak detectors. The operation of the Channel A circuits will be described, the channel B circuits are identical.

Diodes D6301 and D6302 cause the output of U62A to be offset from the input by one diode drop. For positive signal voltages the output will be 0.6 V higher than the input, for negative voltages the output will be 0.6 V lower than the input. This output signal is rectified by diodes D6201 and D6202. The positive voltage from D6201 is stored on capacitor C6201 and serves as the positive threshold reference for the comparators. The negative voltage from D6202 is stored on capacitor C6202 and serves as the negative reference for the comparators. The input signal is developed across R6306 and fed to the four comparators in U721 and U722. Each comparator compares the signal to a different reference, one to each of the two references discussed above and two at zero.

Series resistor capacitor networks R6203-C6101 and R6207-C6203 provide hysteresis to prevent oscillation on the comparator transitions without disturbing the dc value of the reference voltage. Since U721A and U722B are comparing to ground the hysteresis is provided with resistors only. R6208 offsets the hysteresis voltage so that the comparison point of U722B for positive going zero crossings is 0 V. The outputs of the comparators are used to drive dual flip-flop U831. The waveforms for all of the comparator outputs and the flip-flop outputs are shown in FIGURE PHA1.1. The resulting flip-flop outputs are square waves in which the rising edge represents one zero crossing of the input signal. The use of separate comparators to compare the zero crossing and the peak provides a large amount of hysteresis and reduces the sensitivity of the phasemeter to interfering noise.

Dual flip-flop U94 and data selectors U841 and U832 form a pair of edge triggered flip-flops. The data selectors also implement the 0-360° or ±180° range selection. Consider the operation of U841 and U94B. Consider the operation when the range select line /180 is low. U841 is an electronic switch which selects the input to the flip-flop. Its position is selected by the logic level at its A input. Suppose the flip-flop U94 is cleared so that the /Q output is high. This forces the D input high and sets the switch to the 1 position. The squared version of the channel B input is fed to the clock input of the flip-flop. When the next positive transition of this signal occurs the flip-flop will be clocked and the outputs will change state. This will set the switch to its 0 input, connecting the squared version of the channel A signal to the clock input. The next positive transition of the channel A signal will cause the flip flop to change state back again.

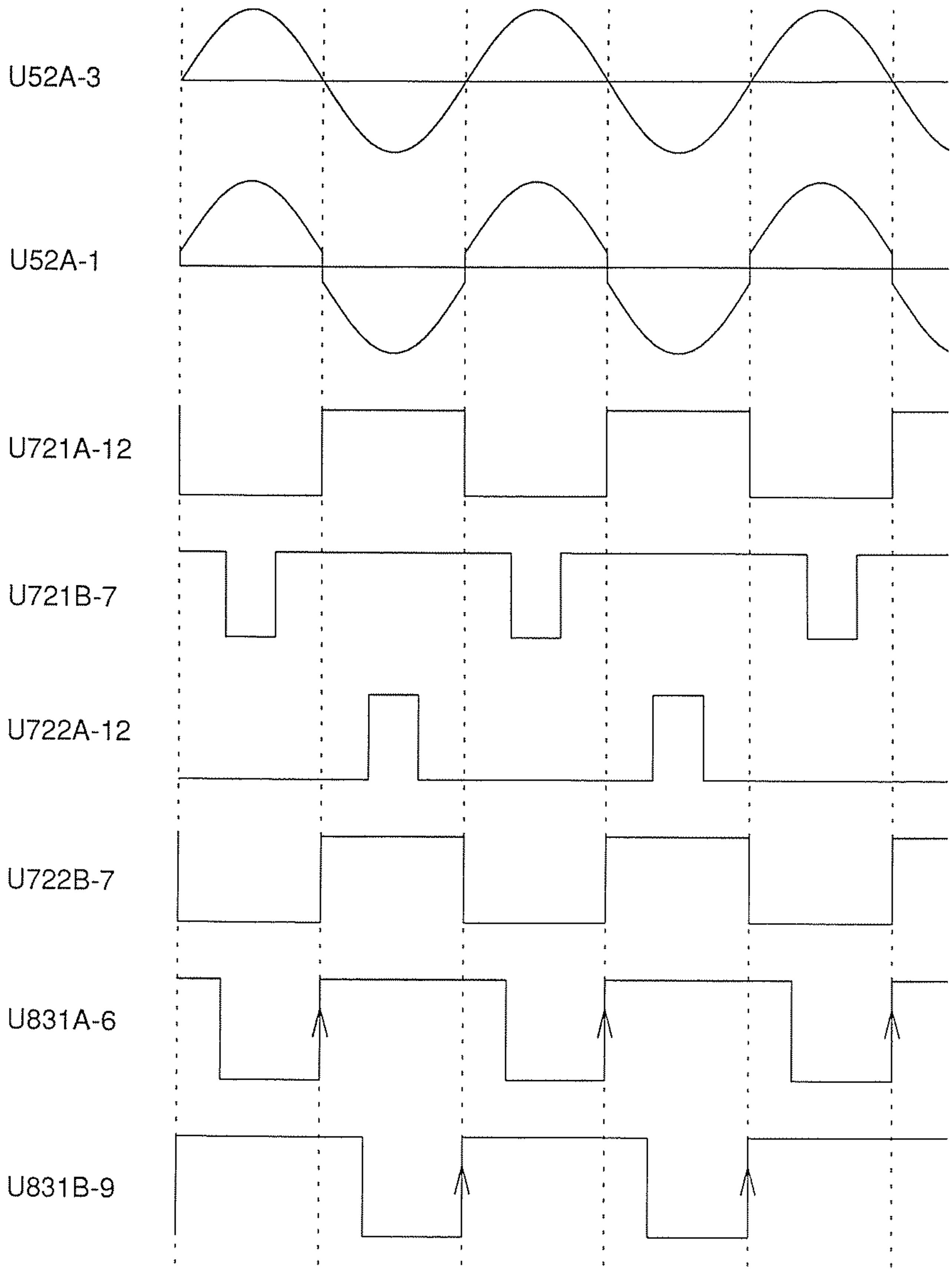
The output of the flip-flop will then represent the time difference between the two channels. The average voltage of this waveform is proportional to the phase difference between the two channels. R9401 and C9401 perform this averaging. The result is fed to the voltage to frequency converter U82. The output frequency is sent to the LVF-1 board for counting by the microprocessor circuits. An identical data switch and flip-flop circuit comprising U832 and U94A measures the phase shift between the negative going zero crossings. This is averaged through R9402 into the same capacitor (C9401) as the previous circuit. This reduces errors on the measurement due to asymmetry on the signal waveforms. At low frequencies the averaging provided by C9401 is not enough to suppress ripple. Q9501 switches in C9501 to increase the filtering.

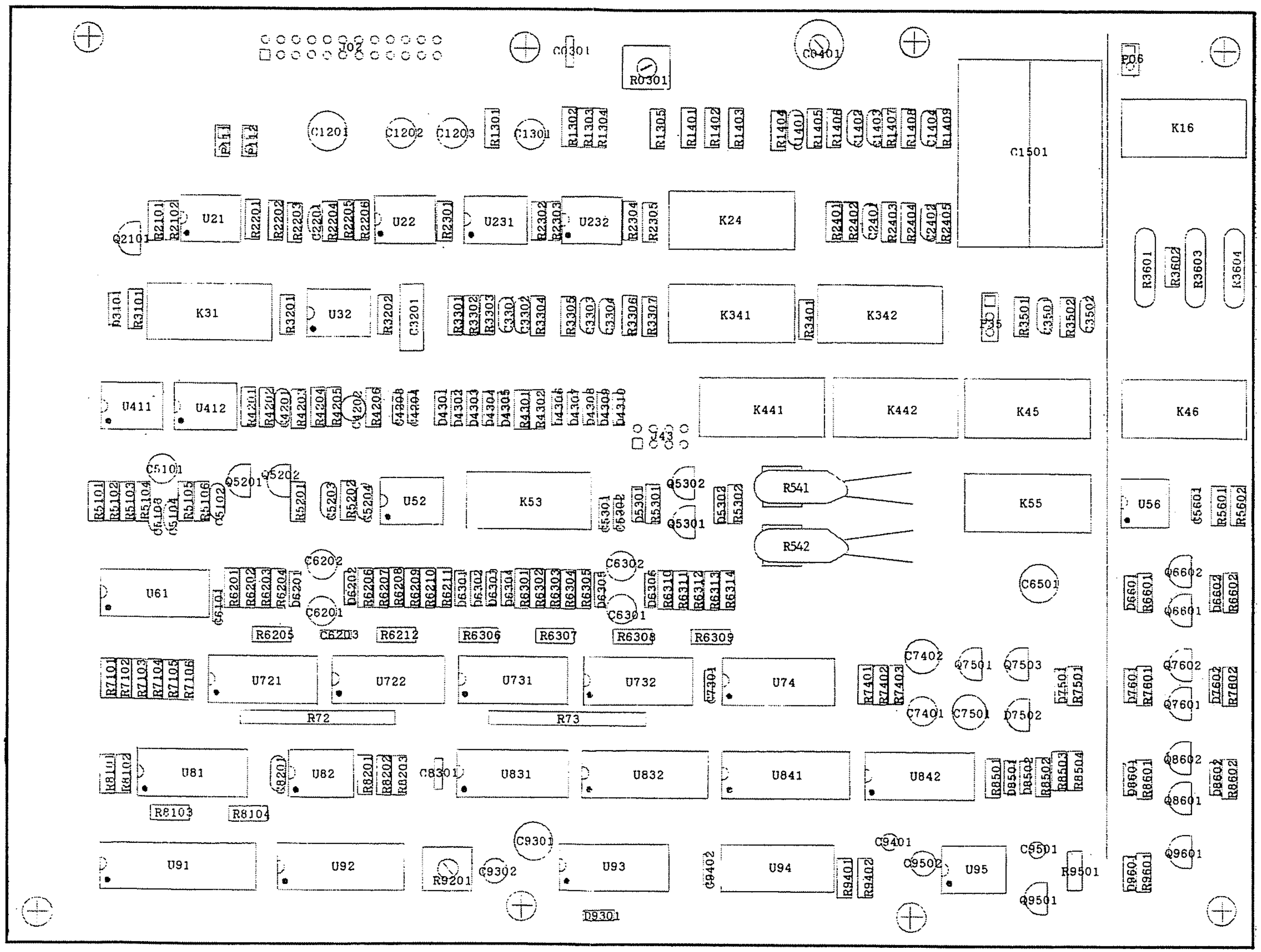
Since the phase measurement is the average value of the voltage pulse from U94 it is important that the amplitude of this pulse be well controlled and noise free. This is provided by a separate +5V power supply, regulated by U95A. This is an open collector comparator which compares its output to a reference voltage obtained from D7502.

The discussion so far has assumed the phasemeter is operating with a 0-360° range. If the signals being measured are in phase, the phasemeter may read 0° or 360°. If the circuit bounces back and forth between these values quickly the display will read the average, or something near 180°. By comparing the rising edge of one signal to the falling edge of the other signal a ±180° range is achieved. This is accomplished by using the 2 and 3 inputs of the data selectors U841 and U832. When the 180 line is high the A input of the data selectors will select between the 2 and 3 inputs instead of the 0 and 1 inputs.

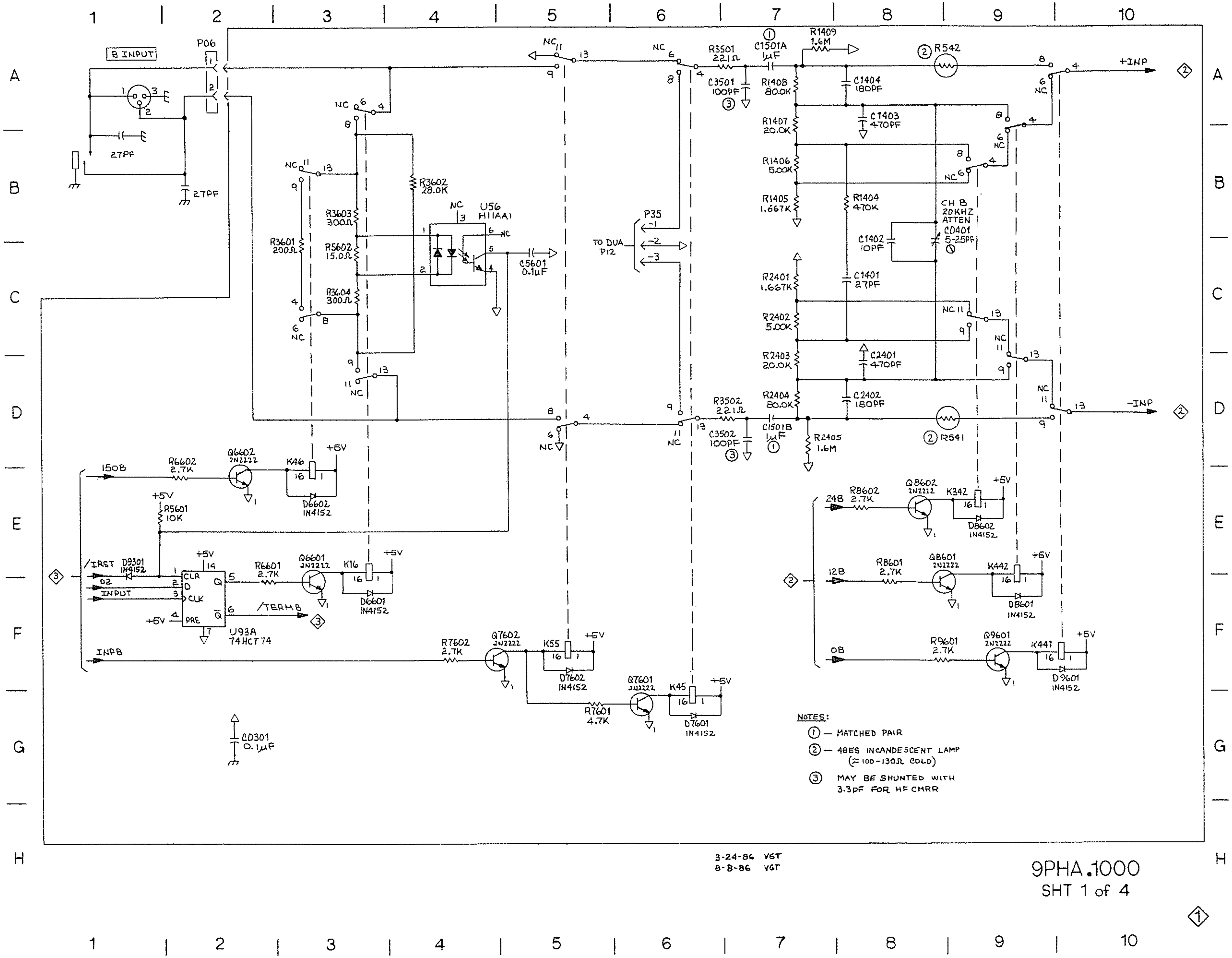
A simple phase comparison between the two input channels is performed by the exclusive-OR gate U842A. The comparison pulses at its output are averaged by R7401 and C7401. If the signals are within ±90° this voltage will be low. If the signals are within 90-270° the voltage will be high. This is fed into U842B and U842C which are used as a comparator at approximately +2.5 V. The logic output PHASEN is then fed to the tri-state buffer U61 for reading by the microprocessor. This information is passed to the host computer with the phase reading. C7402 and Q7501 increase the averaging at low frequencies to reduce the ripple on the comparison voltage. R7403 provides hysteresis to prevent oscillation at comparison voltages near the 2.5 V threshold.

Figure PHA1.1 PHASEMETER OPERATION





DUAL INPUT ANALYZER & PHASE OPTION 9PHA.1000

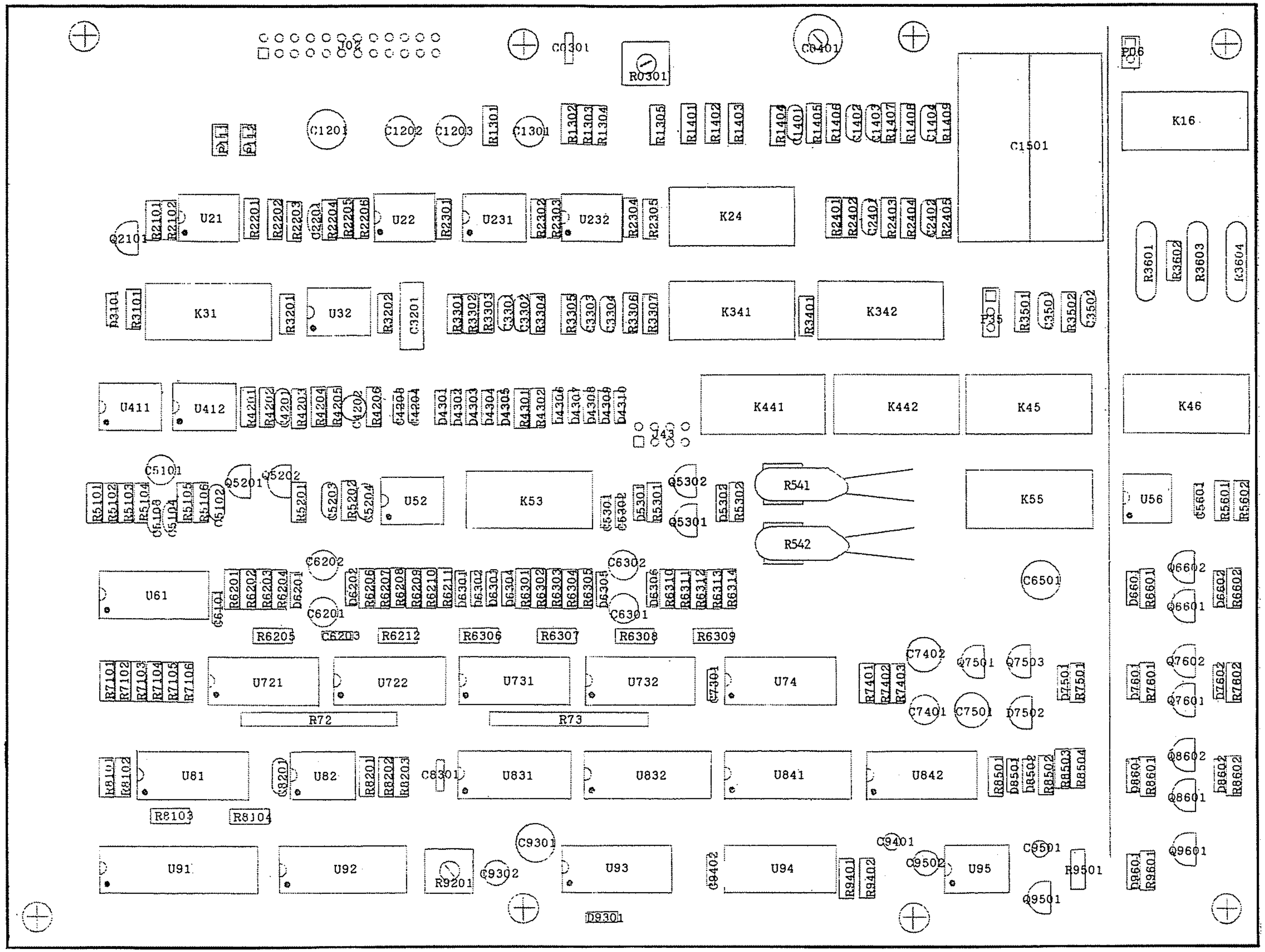


NOTES:

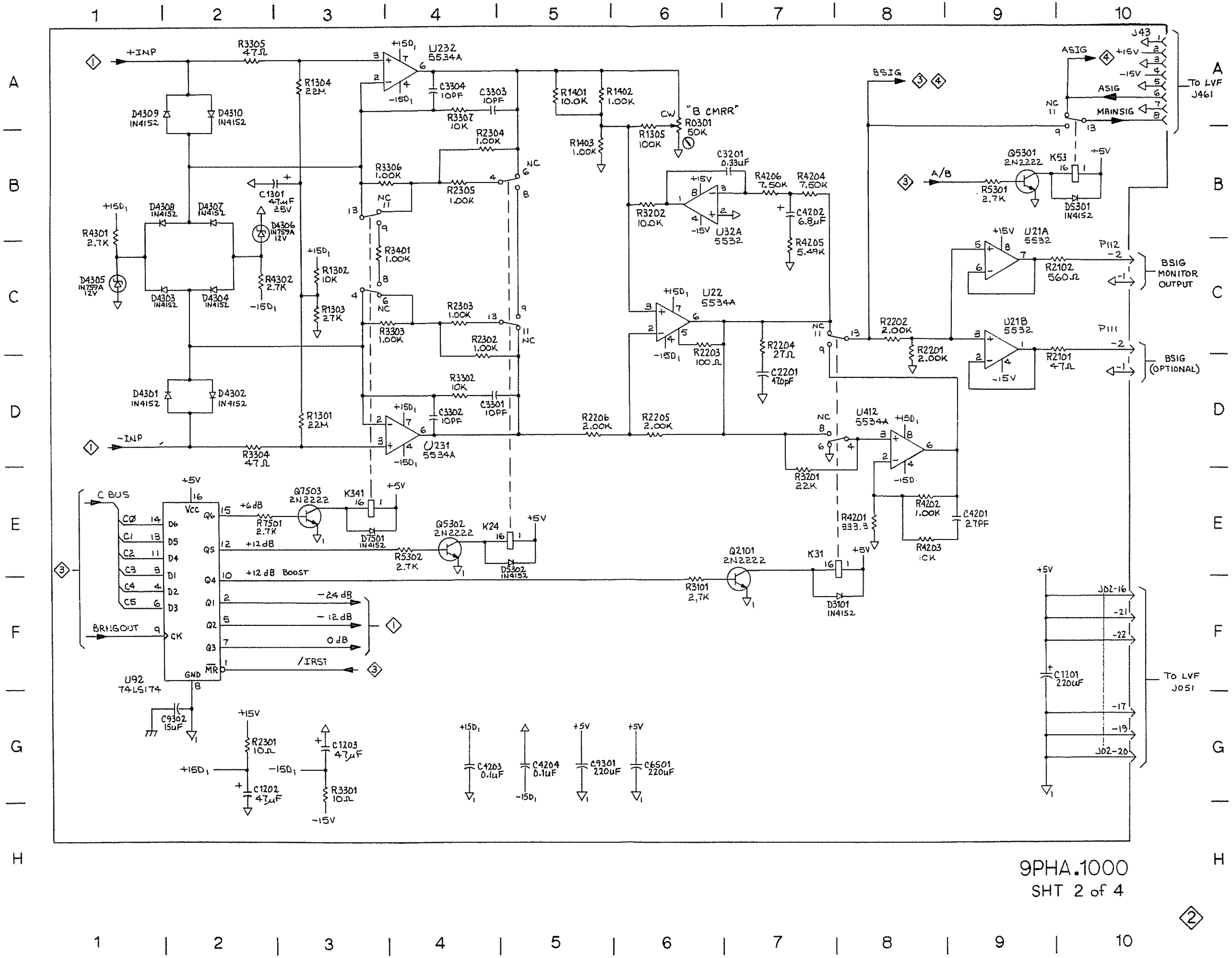
1. — MATCHED PAIR
2. — 48ES INCANDESCENT LAMP (≈ 100-130Ω COLD)
3. MAY BE SHUNTED WITH 3.3pF FOR HF CMRR

3-24-86 VGT
8-8-86 VGT

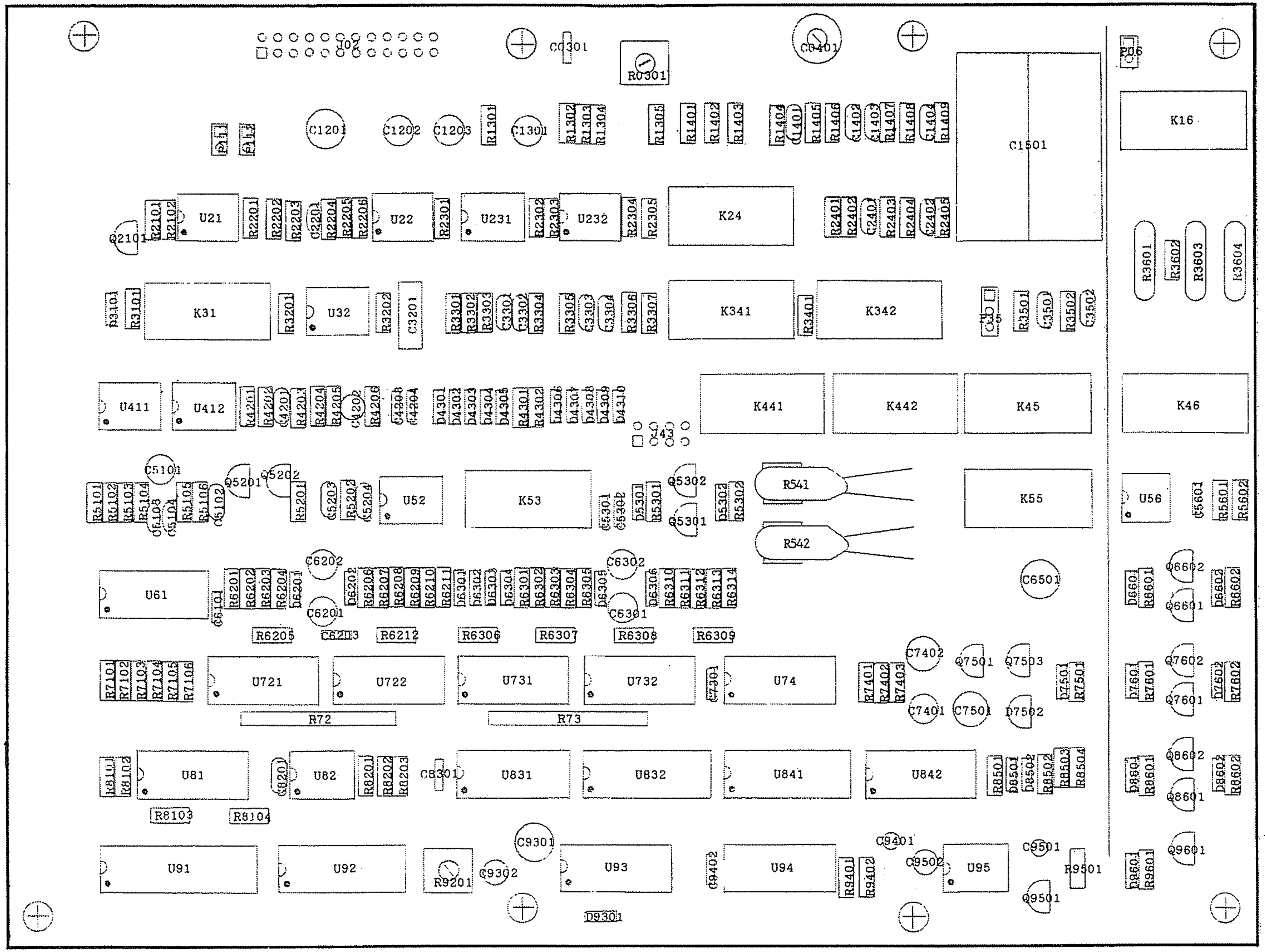
9PHA.1000
SHT 1 of 4



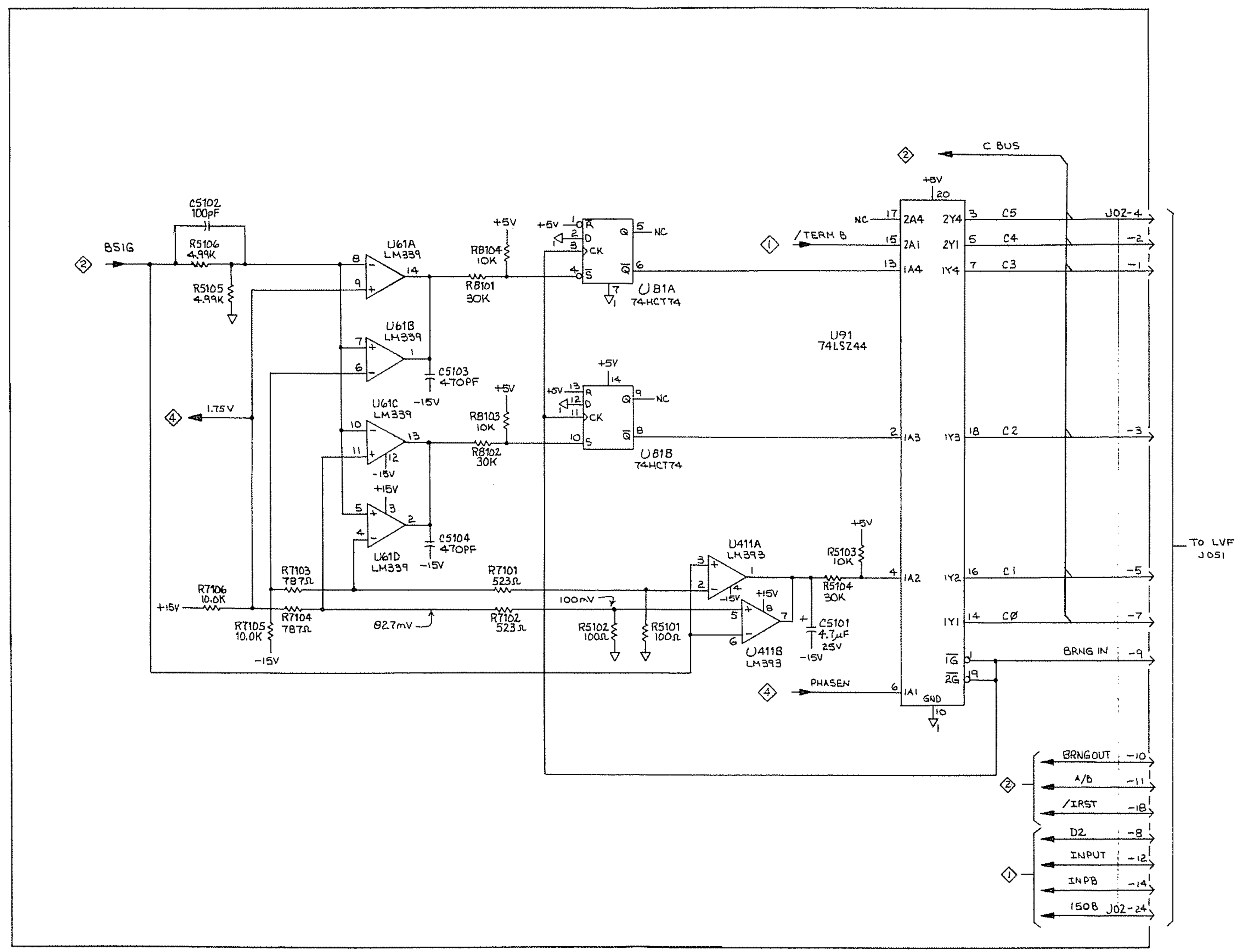
DUAL INPUT ANALYZER & PHASE OPTION 9PHA.1000



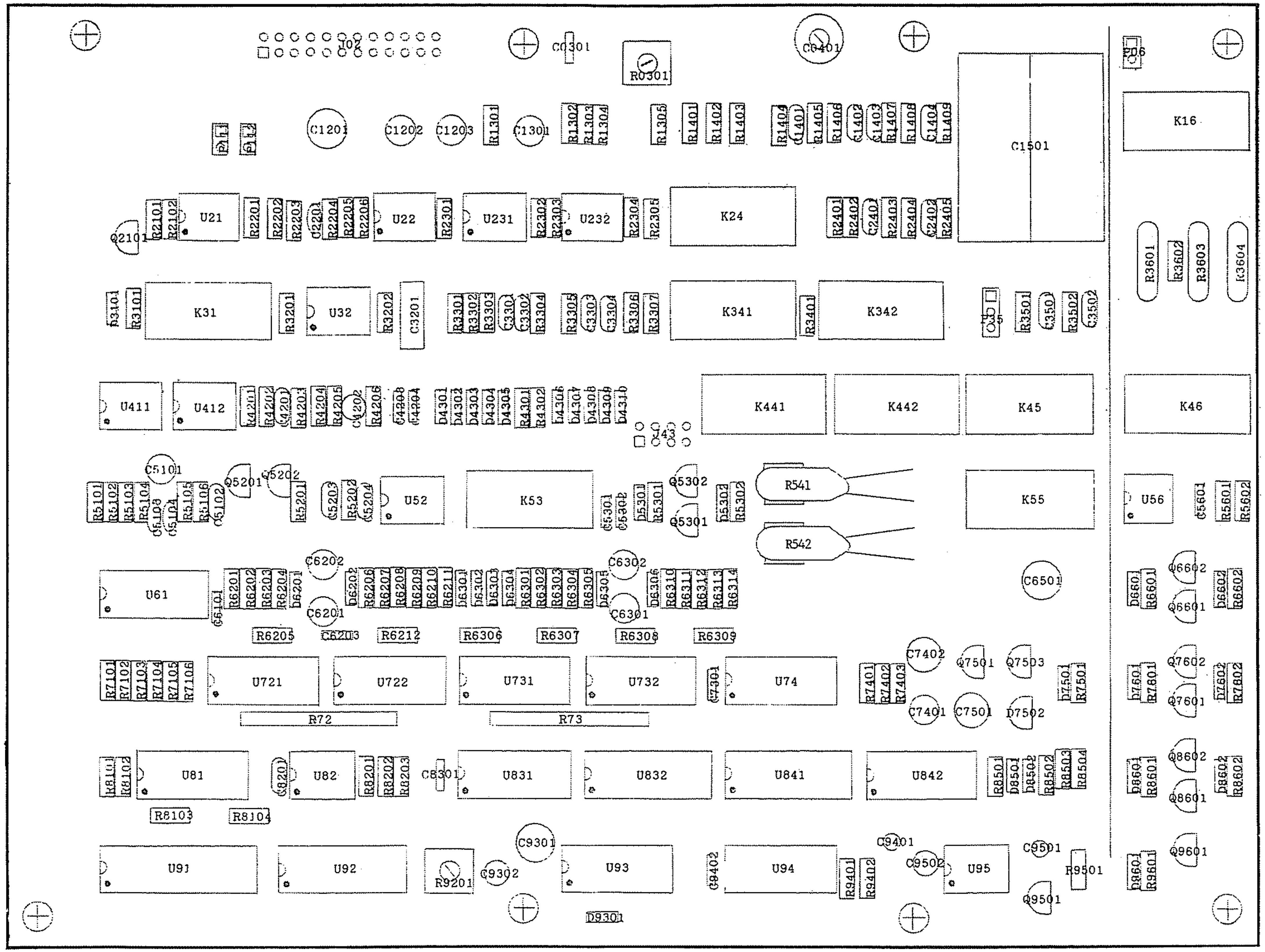
9PHA.1000
SHT 2 of 4



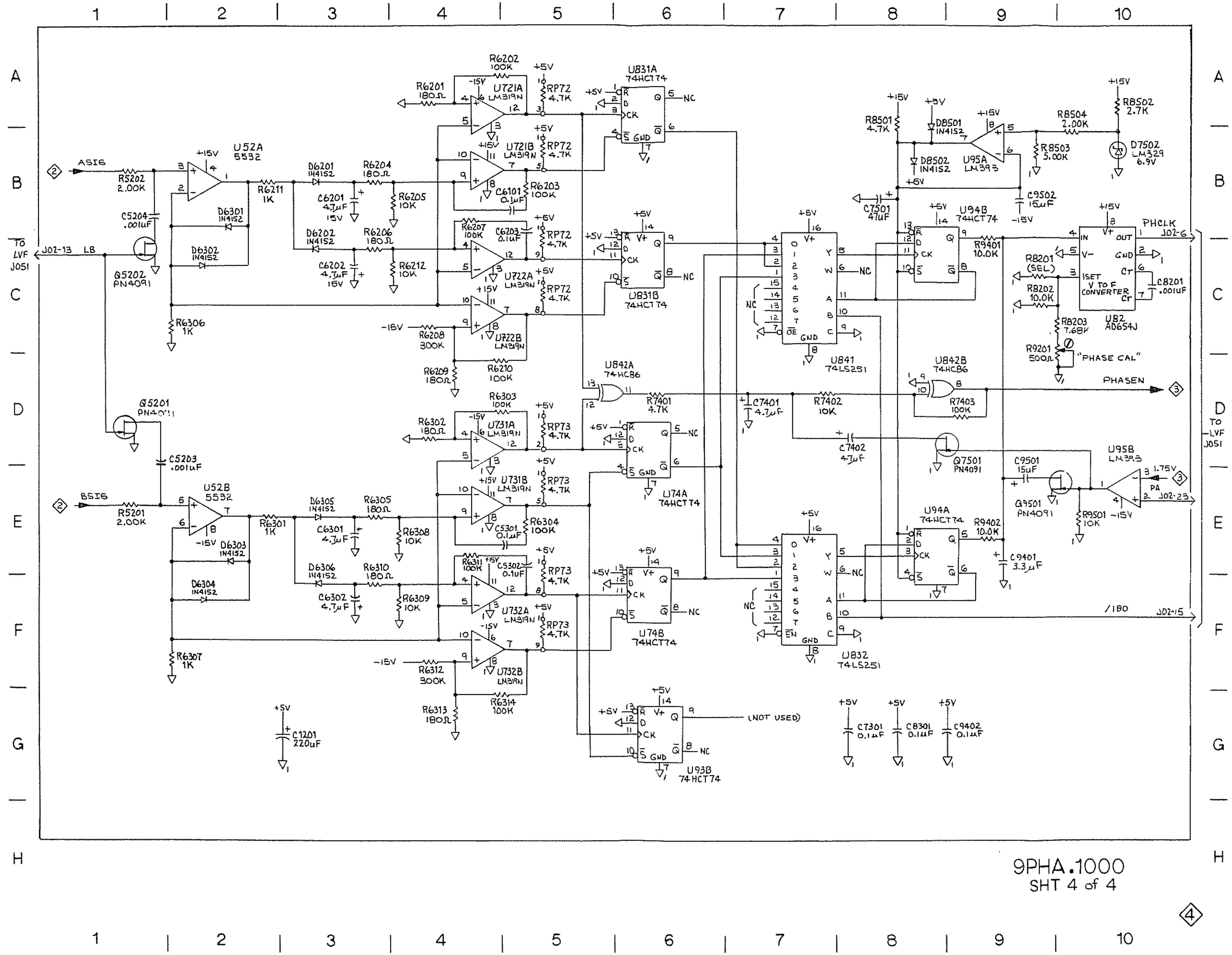
DUAL INPUT ANALYZER & PHASE OPTION 9PHA.1000



9PHA.1000
SHT 3 of 4



DUAL INPUT ANALYZER & PHASE OPTION 9PHA.1000



9PHA.1000
SHT 4 of 4

Board Loc.	Schematic Loc.	Part Number	Description	
C0301	1G2	2172.0104	CAP CERAM 100V 20%	.1uF
C0401	1C8	4450.0250	VAR CAP PC	5-25pF
C1201	4G3	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1202	2G2	2932.0476	CAP AL-EL 25V 20%	47uF
C1203	2G3	2932.0476	CAP AL-EL 25V 20%	47uF
C1301	2B2	2932.0476	CAP AL-EL 25V 20%	47uF
C1401	1C8	2294.0270	CAP MICA 500V 5%	27pF
C1402	1C8	2294.0100	CAP MICA 500V 5%	10pF
C1403	1A8	2296.0471	CAP MICA 500V 1%	470pF
C1404	1A8	2296.0181	CAP MICA 500V 1%	180pF
C1501	1A7,1D7	2694.0105.M	CAP POLYC 250V .25% MATCH	1uF
C2201	2D7	2172.0471	CAP CERAM 100V 20%	470pF
C2401	1D8	2296.0471	CAP MICA 500V 1%	470pF
C2402	1D8	2296.0181	CAP MICA 500V 1%	180pF
C3201	2B7	2675.0334	CAP POLYC 100V 2%	.33uF
C3301	2D4	2294.0100	CAP MICA 500V 5%	10pF
C3302	2D4	2294.0100	CAP MICA 500V 5%	10pF
C3303	2A4	2294.0100	CAP MICA 500V 5%	10pF
C3304	2A4	2294.0100	CAP MICA 500V 5%	10pF
C3501	1A7	2296.0101	CAP MICA 500V 1%	100pF
C3502	1D7	2296.0101	CAP MICA 500V 1%	100pF
C4201	2E9	2294.0270	CAP MICA 500V 5%	27pF
C4202	2B7	2932.0685	CAP AL-EL 35V 20%	6.8uF
C4203	2G4	2172.0104	CAP CERAM 100V 20%	.1uF
C4204	2G5	2172.0104	CAP CERAM 100V 20%	.1uF
C5101	3F7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C5102	3C2	2296.0101	CAP MICA 500V 1%	100pF
C5103	3D4	2172.0471	CAP CERAM 100V 20%	470pF
C5104	3E4	2172.0471	CAP CERAM 100V 20%	470pF
C5203	4D1	2296.0102	CAP MICA 500V 1%	.001uF
C5204	4B1	2296.0102	CAP MICA 500V 1%	.001uF
C5301	4E5	2172.0104	CAP CERAM 100V 20%	.1uF
C5302	4E5	2172.0104	CAP CERAM 100V 20%	.1uF
C5601	1C5	2172.0104	CAP CERAM 100V 20%	.1uF
C6101	4B5	2172.0104	CAP CERAM 100V 20%	.1uF
C6201	4B3	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6202	4C3	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6203	4B5	2172.0104	CAP CERAM 100V 20%	.1uF
C6301	4E3	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6302	4F3	2942.0475	CAP AL-EL 35V 20%	4.7uF
C6501	2G6	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C7301	4G8	2172.0104	CAP CERAM 100V 20%	.1uF
C7401	4D7	2942.0475	CAP AL-EL 35V 20%	4.7uF
C7402	4D8	2932.0476	CAP AL-EL 25V 20%	47uF
C7501	4B8	2932.0476	CAP AL-EL 25V 20%	47uF
C8201	4C10	2296.0102	CAP MICA 500V 1%	.001uF
C8301	4G8	2172.0104	CAP CERAM 100V 20%	.1uF
C9301	2G5	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C9302	2G2	2832.0156	CAP TA-EL 25V 20%	15uF
C9401	4E9	2952.0335	CAP AL-EL 50V 20%	3.3uF
C9402	4G9	2172.0104	CAP CERAM 100V 20%	.1uF
C9501	4E9	2832.0156	CAP TA-EL 25V 20%	15uF
C9502	4B9	2832.0156	CAP TA-EL 25V 20%	15uF

Replaceable Electrical Parts List PHA-1

Board Loc.	Schematic Loc.	Part Number	Description	
D3101	2F8	3110.4152	DIODE SIGNAL	4152
D4301	2D2	3110.4152	DIODE SIGNAL	4152
D4302	2D2	3110.4152	DIODE SIGNAL	4152
D4303	2C1	3110.4152	DIODE SIGNAL	4152
D4304	2C2	3110.4152	DIODE SIGNAL	4152
D4305	2C1	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D4306	2B2	3130.0120	DIODE ZEN 1/2W 5% 12V	1N759
D4307	2B2	3110.4152	DIODE SIGNAL	4152
D4308	2B1	3110.4152	DIODE SIGNAL	4152
D4309	2A2	3110.4152	DIODE SIGNAL	4152
D4310	2A2	3110.4152	DIODE SIGNAL	4152
D5301	2B10	3110.4152	DIODE SIGNAL	4152
D5302	2E5	3110.4152	DIODE SIGNAL	4152
D6201	4B3	3110.4152	DIODE SIGNAL	4152
D6202	4C3	3110.4152	DIODE SIGNAL	4152
D6301	4B2	3110.4152	DIODE SIGNAL	4152
D6302	4C2	3110.4152	DIODE SIGNAL	4152
D6303	4E2	3110.4152	DIODE SIGNAL	4152
D6304	4F2	3110.4152	DIODE SIGNAL	4152
D6305	4E3	3110.4152	DIODE SIGNAL	4152
D6306	4F3	3110.4152	DIODE SIGNAL	4152
D6601	1F3	3110.4152	DIODE SIGNAL	4152
D6602	1E3	3110.4152	DIODE SIGNAL	4152
D7501	2E3	3110.4152	DIODE SIGNAL	4152
D7502	4B10	3131.0069	DIODE PREC REF ZEN 6.9V	LM329
D7601	1G6	3110.4152	DIODE SIGNAL	4152
D7602	1F5	3110.4152	DIODE SIGNAL	4152
D8501	4B8	3110.4152	DIODE SIGNAL	4152
D8502	4B8	3110.4152	DIODE SIGNAL	4152
D8601	1F9	3110.4152	DIODE SIGNAL	4152
D8602	1E9	3110.4152	DIODE SIGNAL	4152
D9301	1E1	3110.4152	DIODE SIGNAL	4152
D9601	1F10	3110.4152	DIODE SIGNAL	4152
E231	---	4232.0008	SOCKET IC DIP	8 PIN
E232	---	4232.0008	SOCKET IC DIP	8 PIN
E35	---	4132.0155	CABLE 2 COND SHLD 15.5	3 PIN
E541	---	4261.0001	FUSE CLIP PC	
E542	---	4261.0001	FUSE CLIP PC	
ECB01	---	6200.PHA1	ECB 2 LAYER 6 X8	DUAL IN/PHAS
HN03	---	5532.1240	STANDOFF HEX M/F	1/4 X1.25
HN06	---	5532.1240	STANDOFF HEX M/F	1/4 X1.25
HN93	---	5532.1240	STANDOFF HEX M/F	1/4 X1.25
HN96	---	5532.1240	STANDOFF HEX M/F	1/4 X1.25
I541	1D9	4700.4840	LAMP INCANDESCENT 48V	40mA
I542	1A9	4700.4840	LAMP INCANDESCENT 48V	40mA
J02	2F10,3C10,4B10,4C1	4221.1024	JACK PC 2 X .1	24 PIN
J43	2A10	4221.1008	JACK PC 2 X .1	8 PIN
K16	1E3	4530.0001	RELAY PC	DPDT

Board Loc.	Schematic Loc.	Part Number	Description	
K24	2E5	4530.0001	RELAY PC	DPDT
K31	2E8	4530.0001	RELAY PC	DPDT
K341	2E3	4530.0001	RELAY PC	DPDT
K342	1E9	4530.0001	RELAY PC	DPDT
K441	1F10	4530.0001	RELAY PC	DPDT
K442	1E9	4530.0001	RELAY PC	DPDT
K45	1G6	4530.0001	RELAY PC	DPDT
K46	1E3	4530.0001	RELAY PC	DPDT
K53	2B10	4530.0001	RELAY PC	DPDT
K55	1F5	4530.0001	RELAY PC	DPDT
P02	—	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
P06	1A2	4221.0036	PLUG PC .1 X.43	36 PIN
P111	2C10	4221.0036	PLUG PC .1 X.43	36 PIN
P112	2C10	4221.0036	PLUG PC .1 X.43	36 PIN
P35	1B6	4221.0036	PLUG PC .1 X.43	36 PIN
P43	—	4221.0072.2	PLUG PC 2X.1 X1.03	72 PIN
Q2101	2E7	3211.2222	XSTR NPN TO92	PN2222A
Q5201	4D1	3214.4091	XSTR FET TO92	PN4091
Q5202	4C1	3214.4091	XSTR FET TO92	PN4091
Q5301	2B9	3211.2222	XSTR NPN TO92	PN2222A
Q5302	2E4	3211.2222	XSTR NPN TO92	PN2222A
Q6601	1F3	3211.2222	XSTR NPN TO92	PN2222A
Q6602	1E2	3211.2222	XSTR NPN TO92	PN2222A
Q7501	4D9	3214.4091	XSTR FET TO92	PN4091
Q7503	2E3	3211.2222	XSTR NPN TO92	PN2222A
Q7601	1G6	3211.2222	XSTR NPN TO92	PN2222A
Q7602	1F5	3211.2222	XSTR NPN TO92	PN2222A
Q8601	1F8	3211.2222	XSTR NPN TO92	PN2222A
Q8602	1E8	3211.2222	XSTR NPN TO92	PN2222A
Q9501	4E10	3214.4091	XSTR FET TO92	PN4091
Q9601	1F9	3211.2222	XSTR NPN TO92	PN2222A
R0301	2A6	4412.0503	POT TRIM PC ENC	50K
R1301	2D3	1214.0226	RES 1/4W C FLM 5%	22M
R1302	2C3	1214.0103	RES 1/4W C FLM 5%	10K
R1303	2C3	1214.0273	RES 1/4W C FLM 5%	27K
R1304	2A3	1214.0226	RES 1/4W C FLM 5%	22M
R1305	2B6	1214.0104	RES 1/4W/C/FLM 5%	100K
R1401	2A5	1136.1002	RES 1/8W M FLM 1%	10.0K
R1402	2A5	1139.1001	RES 1/8W M FLM .1%	1.00K
R1403	2B5	1139.1001	RES 1/8W M FLM .1%	1.00K
R1404	1B8	1214.0434	RES 1/4W C FLM 5%	430K
R1405	1B7	1139.1671	RES 1/8W M FLM .1%	1.667K
R1406	1B7	1139.5001	RES 1/8W M FLM .1%	5.00K
R1407	1A7	1139.2002	RES 1/8W M FLM .1%	20.0K
R1408	1A7	1139.8002	RES 1/8W M FLM .1%	80.0K
R1409	1A7	1214.0165	RES 1/4W C FLM 5%	1.6M
R2101	2C9	1214.0470	RES 1/4W C FLM 5%	47
R2102	2C9	1214.0561	RES 1/4W C FLM 5%	560
R2201	2C8	1139.2001	RES 1/8W M FLM .1%	2.00K
R2202	2C8	1139.2001	RES 1/8W M FLM .1%	2.00K
R2203	2C6	1214.0101	RES 1/4W C FLM 5%	100

Replaceable Electrical Parts List PHA-1

Board Loc.	Schematic Loc.	Part Number	Description	
R2204	2C7	1214.0270	RES 1/4W C FLM 5%	27
R2205	2D6	1139.2001	RES 1/8W M FLM .1%	2.00K
R2206	2D5	1139.2001	RES 1/8W M FLM .1%	2.00K
R2301	2G2	1214.0100	RES 1/4W C FLM 5%	10
R2302	2D4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2303	2C4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2304	2B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2305	2B4	1139.1001	RES 1/8W M FLM .1%	1.00K
R2401	1C7	1139.1671	RES 1/8W M FLM .1%	1.667K
R2402	1C7	1139.5001	RES 1/8W M FLM .1%	5.00K
R2403	1D7	1139.2002	RES 1/8W M FLM .1%	20.0K
R2404	1D7	1139.8002	RES 1/8W M FLM .1%	80.0K
R2405	1D7	1214.0165	RES 1/4W C FLM 5%	1.6M
R3101	2F6	1214.0272	RES 1/4W C FLM 5%	2.7K
R3201	2E7	1214.0223	RES 1/4W C FLM 5%	22K
R3202	2B6	1136.1002	RES 1/8W M FLM 1%	10.0K
R3301	2G3	1214.0100	RES 1/4W C FLM 5%	10
R3302	2D4	1214.0470	RES 1/4W C FLM 5%	47
R3303	2C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3304	2D2	1214.0103	RES 1/4W C FLM 5%	10K
R3305	2A2	1214.0103	RES 1/4W C FLM 5%	10K
R3306	2B3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3307	2A4	1214.0470	RES 1/4W C FLM 5%	47
R3401	2C3	1139.1001	RES 1/8W M FLM .1%	1.00K
R3501	1A7	1136.2210	RES 1/8W M FLM 1%	221
R3502	1D7	1136.2210	RES 1/8W M FLM 1%	221
R3601	1C3	1656.2000	RES 3W W WND 1%	200
R3602	1B4	1136.2802	RES 1/8W M FLM 1%	28.0K
R3603	1B3	1656.3000	RES 3W W WND 1%	300
R3604	1C3	1656.3000	RES 3W W WND 1%	300
R4201	2E8	1139.3330	RES 1/8W M FLM .1%	333.3
R4202	2E8	1139.1001	RES 1/8W M FLM .1%	1.00K
R4203	2E8	1214.0103	RES 1/4W C FLM 5%	10K
R4204	2B7	1136.7501	RES 1/8W M FLM 1%	7.50K
R4205	2C7	1136.5491	RES 1/8W M FLM 1%	5.49K
R4206	2B7	1136.7501	RES 1/8W M FLM 1%	7.50K
R4301	2B1	1214.0272	RES 1/4W C FLM 5%	2.7K
R4302	2C2	1214.0272	RES 1/4W C FLM 5%	2.7K
R5101	3F6	1214.0101	RES 1/4W C FLM 5%	100
R5102	3F5	1214.0101	RES 1/4W C FLM 5%	100
R5103	3E7	1214.0103	RES 1/4W C FLM 5%	10K
R5104	3E7	1214.0303	RES 1/4W C FLM 5%	30K
R5105	3C2	1136.4991	RES 1/8W M FLM 1%	4.99K
R5106	3C2	1136.4991	RES 1/8W M FLM 1%	4.99K
R5201	4E1	1139.2001	RES 1/8W M FLM .1%	2.00K
R5202	4B1	1139.2001	RES 1/8W M FLM .1%	2.00K
R5301	2B9	1214.0272	RES 1/4W C FLM 5%	2.7K
R5302	2E4	1214.0272	RES 1/4W C FLM 5%	2.7K
R5601	1E1	1214.0103	RES 1/4W C FLM 5%	10K
R5602	1C3	1136.1509	RES 1/8W M FLM 1%	15.0
R6201	4A4	1214.0181	RES 1/4W C FLM 5%	180
R6202	4A5	1214.0104	RES 1/4W/C/FLM 5%	100K
R6203	4B5	1214.0104	RES 1/4W/C/FLM 5%	100K
R6204	4B3	1214.0181	RES 1/4W C FLM 5%	180

Board Loc.	Schematic Loc.	Part Number	Description	
R6205	4B4	1214.0103	RES 1/4W C FLM 5%	10K
R6206	4C3	1214.0181	RES 1/4W C FLM 5%	180
R6207	4B4	1214.0104	RES 1/4W/C/FLM 5%	100K
R6208	4C4	1214.0304	RES 1/4W C FLM 5%	300K
R6209	4D4	1214.0181	RES 1/4W C FLM 5%	180
R6210	4D5	1214.0104	RES 1/4W/C/FLM 5%	100K
R6211	4B2	1214.0102	RES 1/4W C FLM 5%	1K
R6212	4C4	1214.0103	RES 1/4W C FLM 5%	10K
R6301	4E2	1214.0102	RES 1/4W C FLM 5%	1K
R6302	4D4	1214.0181	RES 1/4W C FLM 5%	180
R6303	4D5	1214.0104	RES 1/4W/C/FLM 5%	100K
R6304	4E5	1214.0104	RES 1/4W/C/FLM 5%	100K
R6305	4E3	1214.0181	RES 1/4W C FLM 5%	180
R6306	4C2	1214.0102	RES 1/4W C FLM 5%	1K
R6307	4F2	1214.0102	RES 1/4W C FLM 5%	1K
R6308	4E4	1214.0103	RES 1/4W C FLM 5%	10K
R6309	4F4	1214.0103	RES 1/4W C FLM 5%	10K
R6310	4F3	1214.0181	RES 1/4W C FLM 5%	180
R6311	4E4	1214.0104	RES 1/4W/C/FLM 5%	100K
R6312	4F4	1214.0304	RES 1/4W C FLM 5%	300K
R6313	4G4	1214.0181	RES 1/4W C FLM 5%	180
R6314	4G4	1214.0104	RES 1/4W/C/FLM 5%	100K
R6601	1F2	1214.0272	RES 1/4W C FLM 5%	2.7K
R6602	1E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R7101	3E5	1136.5230	RES 1/8W M FLM 1%	523
R7102	3F5	1136.5230	RES 1/8W M FLM 1%	523
R7103	3E3	1136.7870	RES 1/8W M FLM 1%	787
R7104	3F3	1136.7870	RES 1/8W M FLM 1%	787
R7105	3F3	1136.1002	RES 1/8W M FLM 1%	10.0K
R7106	3F2	1136.1002	RES 1/8W M FLM 1%	10.0K
R72	4A5,4B5,4C5	1984.9472	RES NET SIP 5%	9 X 4.7K
R73	4D5,4E5,4F5	1984.9472	RES NET SIP 5%	9 X 4.7K
R7401	4D6	1214.0472	RES 1/4W C FLM 5%	4.7K
R7402	4D7	1214.0103	RES 1/4W C FLM 5%	10K
R7403	4D9	1214.0104	RES 1/4W/C/FLM 5%	100K
R7501	2E2	1214.0272	RES 1/4W C FLM 5%	2.7K
R7601	1G5	1214.0472	RES 1/4W C FLM 5%	4.7K
R7602	1F4	1214.0272	RES 1/4W C FLM 5%	2.7K
R8101	3C4	1214.0303	RES 1/4W C FLM 5%	30K
R8102	3D4	1214.0303	RES 1/4W C FLM 5%	30K
R8103	3D5	1214.0103	RES 1/4W C FLM 5%	10K
R8104	3C5	1214.0103	RES 1/4W C FLM 5%	10K
R8201	4C9	1136.4122	RES 1/8W M FLM 1%	41.2K
R8202	4C9	1136.1002	RES 1/8W M FLM 1%	10.0K
R8203	4C10	1136.7681	RES 1/8W M FLM 1%	7.68K
R8501	4A8	1214.0472	RES 1/4W C FLM 5%	4.7K
R8502	4A10	1214.0272	RES 1/4W C FLM 5%	2.7K
R8503	4B9	1139.5001	RES 1/8W M FLM .1%	5.00K
R8504	4B10	1139.2001	RES 1/8W M FLM .1%	2.00K
R8601	1F8	1214.0272	RES 1/4W C FLM 5%	2.7K
R8602	1E8	1214.0272	RES 1/4W C FLM 5%	2.7K
R9201	4C10	4412.0202	POT TRIM PC ENC	2K
R9401	4C9	1136.1002	RES 1/8W M FLM 1%	10.0K
R9402	4E9	1136.1002	RES 1/8W M FLM 1%	10.0K

Replaceable Electrical Parts List PHA-1

Board Loc.	Schematic Loc.	Part Number	Description	
R9501	4E10	1214.0103	RES 1/4W C FLM 5%	10K
R9601	1F8	1214.0272	RES 1/4W C FLM 5%	2.7K
U21	2C9	3412.5532	OP AMP DUAL	5532
U22	2C6	3411.5534	OP AMP SINGLE	5534A
U231	2D4	3411.5534	OP AMP SINGLE	5534A
U232	2A4	3411.5534	OP AMP SINGLE	5534A
U32	2B6	3412.5532	OP AMP DUAL	5532
U411	3E6,3F7	3422.0393	COMPARATOR DUAL	LM393
U412	2D8	3411.5534	OP AMP SINGLE	5534A
U52	4B2,4E2	3412.5532	OP AMP DUAL	5532
U56	1C4	3630.0001	OPTO-ISOLATOR	H11AA1
U61	3C4,3D4,3F4	3424.0339	COMPARATOR QUAD	LM339
U721	4A4,4B4	3422.0319	COMPARATOR DUAL HI-SPEED	LM319
U722	4C4	3422.0319	COMPARATOR DUAL HI-SPEED	LM319
U731	4D4,4E4	3422.0319	COMPARATOR DUAL HI-SPEED	LM319
U732	4F4	3422.0319	COMPARATOR DUAL HI-SPEED	LM319
U74	4D6,4F6	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U81	3C5,3D5	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U82	4C10	3441.0654	CONVERTER VOLT TO FREQ	AD654J
U831	4A6,4C6	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U832	4F7	3313.0251	MULTIPLEXER TRI-ST	74LS251
U841	4C7	3313.0251	MULTIPLEXER TRI-ST	74LS251
U842	4D5,4D8	3323.0086	GATE 4-IN EXCL OR	74HC86
U91	3C8	3313.0244	BUFFER 8X TRI-STATE	74LS244
U92	2E2	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U93	1F2	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U94	4C8,4E8	3324.0074	FLIP-FLOP 2X J-K	74HCT74
U95	4B9,4E10	3422.0393	COMPARATOR DUAL	LM393
X96	---	7160.0002	SHIELD ECB INPUT	

DIS-1 DISTORTION MEASUREMENT (S/N 10001-10299 ONLY)

DIS-1, DISTORTION MEASUREMENT MODULE

Logic Interface <1>

The logic on the DIS-1 module performs three functions: tuning of the bandpass/bandreject filter, setting of mode control bits, and buffering data between the control microprocessor located on the LVF-1 module and the host computer.

Address and data information from the host computer enter the module via the 40-pin ribbon cable P20. Data is buffered by U101 to form the "D" bus. This bus drives four octal data latches and two 4-bit dual port RAMs. The operation of these devices is identical to that of the RAMs on the LVF-1 module. They contain the input level meter reading (the "LEVEL" display on the LVF panel) and the current frequency sent to the notch filter by the LVF-1 microprocessor. The module address (normally 1, and always 1 higher than the corresponding LVF-1 board) is recognized by 4-bit comparator U301. Its output is used to drive the /ATT line via Q4001 and to enable address decoder U302. U302 decodes the address information to provide write and read strobes for the RAM and the data latches. U201 further decodes the write strobes into individual addresses for the data latches on the D bus.

Information from the control microprocessor located on the LVF-1 module enters the DIS-1 board via connector P43. The data is sent on the C bus while address information is provided by B0 and B1 and strobe lines STATUS and WRDIS. These are decoded by U311A to provide write strobes for the data latches on the C bus. The dual port RAMs are also on the C bus and buffer communication between the microprocessor and the host computer.

The selectable bandpass-bandreject filter can be tuned by either the host computer or the LVF-1 microprocessor. The outputs from latch pairs U121-U221 and U112-U212 are wired in parallel, with the tri-state control pins driven by inverter U312B. The state of bit 7 in U222 determines which pair of latches is used to tune the filter. When this pin is low the host computer tunes the filter and when it is high the microprocessor tunes the filter. The setting of the notch loop compensation is handled in a similar way. Control bits are sent by the host via U222 and by the LVF-1 microprocessor via U421. U232 provides the source selection based on the state of U222 bit 6.

Signal Switching & Level Voltmeter <2>

Schematic <2> contains the input and output signal switching for the DIS-1 module along with the LEVEL voltmeter. The preamplified signal from the selected A or B channel input (MAINSIG) enters the module through P051-7 and is routed through socket J052 pins 2 and 4. This socket is reserved for possible future use. All units will normally be shipped with a shorting jumper between pins 2 and 4.

MAINSIG is then routed to the module bypass relay K04 and to LEVEL voltmeter. K04 returns MAINSIG directly back to the LVF-1 module through P051-3 as FUNCSIG whenever the LVF Reading Mode is AMPLITUDE. Relay K04 is energized for all other measurement modes.

From relay K25, MAINSIG is routed to the intermodulation distortion analyzer socket J031-7 to become IMAIN. The output from the IMD analyzer option (J031-8) is routed to the tunable bandpass-bandreject filter as BPBRIN. If the IM analyzer option is not installed a shorting jumper between pins 7 and 8 of J031 will continue routing MAINSIG to the bandpass/bandreject filter shown on schematics <3> and <4>.

MAINSIG is fed into the LEVEL voltmeter buffer U022A which also serves as a highpass filter to limit low frequency response below approximately 5 Hz. R0403 adjusts the dc offset of this buffer which feeds the RMS detector IC, U021. U021 has an integration time constant determined by C0203, C0102, C0103, and CMOS switch U011. R0404 trims the offset error term of the converter. D0201, R0201, and R0202 clamp the dc output voltage to provide rapid recovery from auto-ranging transients.

The output of the detector is filtered through the internal buffer integral of U022B to reduce the ac ripple content. The V-F converter, U441, converts the dc voltage to a frequency which is routed to the LVF-1 module for counting through P43-20. R4503 adjusts calibration of the V-F conversion and R4501 is factory selected to approximately center R4503. Replacement of U441 may also require changing R4501 to center adjustment R4503. The operation of U441 is otherwise identical to U341 on schematic <8> of the LVF-1 module and will not be repeated here.

The dc output from U022B pin 7 is also routed to J41-1 for use with the intermodulation distortion analyzer option, and to schematic <5> as "VCOMP" for use in the notch filter control loops.

D1301 and D1302 provide low voltage supplies required by the CMOS switches on schematics <2> and <5>.

MUX U001 selects the main frequency counter source signal and returns it to the LVF-1 module through P051 pin 5.

Bandpass/Bandreject Filter <3,4>

The bandpass-bandreject filter is a two stage, 4-pole, design with programmable center frequency control from 10 Hz to over 200 kHz. Schematic <3> contains the first stage and schematic <4> contains the second stage. Figure DIS1.1 shows a simplified diagram of the filter and is helpful in understanding its basic operation.

Each stage consists of a state variable topology containing four op-amps: two integrators, an inverter, and an amplifier stage. The four op-amp outputs provide all possible 2-pole minimum-phase filter responses. <3>-U371 and <4>-U381A are integrators whose outputs exhibit a bandpass response. <3>-U372 and <4>-U381B also function as integrators providing a low-pass output. <3>-U063 and <4>-U092 are inverters that complete the basic state variable loops. <3>-U062 and <4>-U091 sum the bandpass outputs (which are inverted polarity) with the respective inputs to obtain bandreject outputs. <3>-R0600 and <4>-R0803 determine the Q's of the individual state variable filter sections. <3>-R0608 and <4>-R0906 (switched by relay K09) provide interstage feedback to optimize the filter response shape. This feedback path can be disabled when troubleshooting filter tuning problems by temporarily unsoldering one end of R0608.

NOTE: Certain aspects of this filter design are protected by US patent 4,563,652.

Relay K08 selects bandpass or bandreject filter operation. In the bandpass mode, relay K08 is energized cascading the bandpass output of the first stage with the bandpass output of the second stage. The output of K08 is coupled through C0401 to become DISTSIG which is returned to the LVF-1 module through relay K04 on schematic <2>. In the bandreject mode, relay K08 is off and cascades the bandreject output of the first stage with the bandreject output of the second stage.

Filter tuning is accomplished in four decade bands by switching the integrator capacitors and varying the integrator resistors. The timing capacitors are switched by JFETs (for example Q1601 switches C1601 on schematic <3>) and both sections are ganged. Lines R1-R3 control the JFET switches with logical 0 being approximately -15 V and logical 1 being 0 V.

TABLE DIS1.1
BP/BR FILTER TUNING CAPACITOR SWITCHING

FREQUENCY BAND	R1	R2	R3	CAPACITANCE
10.00-204.775 Hz	-15	-15	0	333 nF + 330 pF
205.0-2047.75 Hz	-15	0	-15	33 nF + 330 pF
2.050-20.4775 kHz	0	-15	-15	3 nF + 330 pF
20.50-204.775 kHz	-15	-15	-15	330 pF

The JFET switching circuits are different in the two filter sections. On schematic <3>, the JFETs are switched through diode connected transistors (for example Q1603 switches Q1601). Diode connected transistors are used in the first stage because they offer a lower dynamic on-resistance than comparable discrete diodes. This reduces gate-source junction capacitance modulation from the residual ac gate voltage which contributes distortion at high frequencies. R1603 is necessary to provide a dc return to keep the drain of the JFET near 0 Volts so that it can be pinched-off by pulling its gate to approximately -14 Volts. R1601 and R1602 apply 1/2 of the Ac signal across the JFET to its gate when it is turned on for the most linear resistance characteristic. Typical JFET on-resistance is ≤5 Ohms. On schematic <4>, C0801, C2902, and C2903 decouple the three range control lines to prevent high frequency crosstalk between the two stages.

TABLE DIS1.2
BP/BR TUNING RESISTANCE VS FREQUENCY

F15-F3 (MSB-LSB)	MDAC RESISTANCE	FREQUENCY
0 000 000 000 000	2.500 kOhms	204.775 Hz
0 000 010 111 111	2.560 kOhms	200.00 Hz
0 111 111 111 111	5.000 kOhms	102.40 Hz
1 000 001 011 111	5.120 kOhms	100.00 Hz
1 011 111 111 111	10.00 kOhms	51.20 Hz
1 101 111 111 111	20.00 kOhms	25.60 Hz
1 110 011 001 011	24.98 kOhms	20.50 Hz
1 111 001 101 111	51.20 kOhms	10.00 Hz

Modules A36-A39 function as ganged 2.50 kOhm variable tuning resistors with programmable 13-bit resolution. Lines F3-F15 control the resistors with F15 = MSB and F3 = LSB. These control lines are TTL compatible, inverted logic, with logical 0 being high and logical 1 being low. TABLE DIS1.2 lists tuning resistor values and control bit patterns for selected frequencies in the lowest 10-200 Hz decade.

Relay K09 provides an additional +12 dB gain step by switching the input resistance to <4>-U091. It also switches the interstage feedback (YSIG) resistance, R0906, to maintain constant filter shape in both gain states. K09 works in conjunction with the range amplifier on the LVF-1 module to provide 0 dB to +60 dB of gain, in 12 dB steps, to the bandpass-bandreject filter output signal. TABLE DIS1.3 shows the ranging logic for the BANDPASS and BANDREJECT modes only. It is slightly different than the AMPLITUDE mode logic because of the additional +12 dB gain state that permits a more sensitive 75 uV range.

TABLE DIS1.3
K09 & LVF RANGE AMPLIFIER SWITCHING
BANDPASS/BANDREJECT MODES

BP/BR RANGE	K28	ATTEN	U742 A	U742 B	U742 C	GAIN
≥80 mV	Off	-48 dB	0	1	1	0 dB
20 mV	On	-48 dB	0	1	1	+12 dB
5 mV	On	-36 dB	1	0	0	+24 dB
1.2 mV	On	-24 dB	1	0	1	+36 dB
300 uV	On	-12 dB	1	1	0	+48 dB
75 uV	On	0 dB	1	1	1	+60 dB

The first stage of the filter also contains fine tuning and nulling circuits for use in the THD+N mode. These are driven by servo loops located on schematic <5> and cause the bandreject filter to precisely tune and null out the fundamental component. U061 is a trans-conductance amplifier that feeds a potion of the input signal provided by R0605 and R0606 into the first state variable filter's inverter summing node, U063. This corrects for the effects of capacitor dissipation factor, op-amp bandwidth, and stray capacitance that prevent a perfect null of the notch output. R0601 and R2404 convert the NULL control voltage into a current applied to pin 5 of U061.

C0701 provides phase compensation for the effects of op-amp finite gain at high frequencies. It is selected to maintain the null control loop near the center of its range at high frequencies.

U071, Q0701, and related components form a variable gain stage that provides fine tuning of the state variable filter frequency. The output of the second integrator, LP1SIG, is coupled into U071 through the attenuator R0704 and R0706. The voltage gain of U071 is determined by R0703 and JFET Q0701, operated as a voltage-variable-resistor. Q0701 is selected for high pinch-off voltage to improve its linearity. R0705 feeds the variable signal back into the inverter stage summing node and effectively parallels R0702. R0707, R0708, and R0710 offset and scale the TUNE control voltage to the gate of JFET Q0701. As the TUNE voltage goes more positive, Q0701 becomes more conductive, increasing the gain of U071, thus increasing the frequency of the state variable filter. R0709 feeds a portion of the ac signal into the gate for the most linear JFET resistance characteristic.

Tuning/Nulling Control Loops <5>

In the THD+N mode it is necessary to continuously correct the notch frequency and nulling to maintain high degrees of fundamental rejection. Keeping in mind that the bandreject filter is actually a two stage filter, it is necessary to servo the first section only to obtain excellent fundamental rejection. The second stage can possess several percent tuning error without affecting the shape of the notch characteristic. The basic operation of the loops is to demodulate the residual fundamental content in the notch output and generate control voltages corresponding to the in-phase and 90 degree phase components. It can be shown that the in-phase component represents a null error and a 90 degree phase component represents a slight tuning error. Both must be minimized for optimum performance.

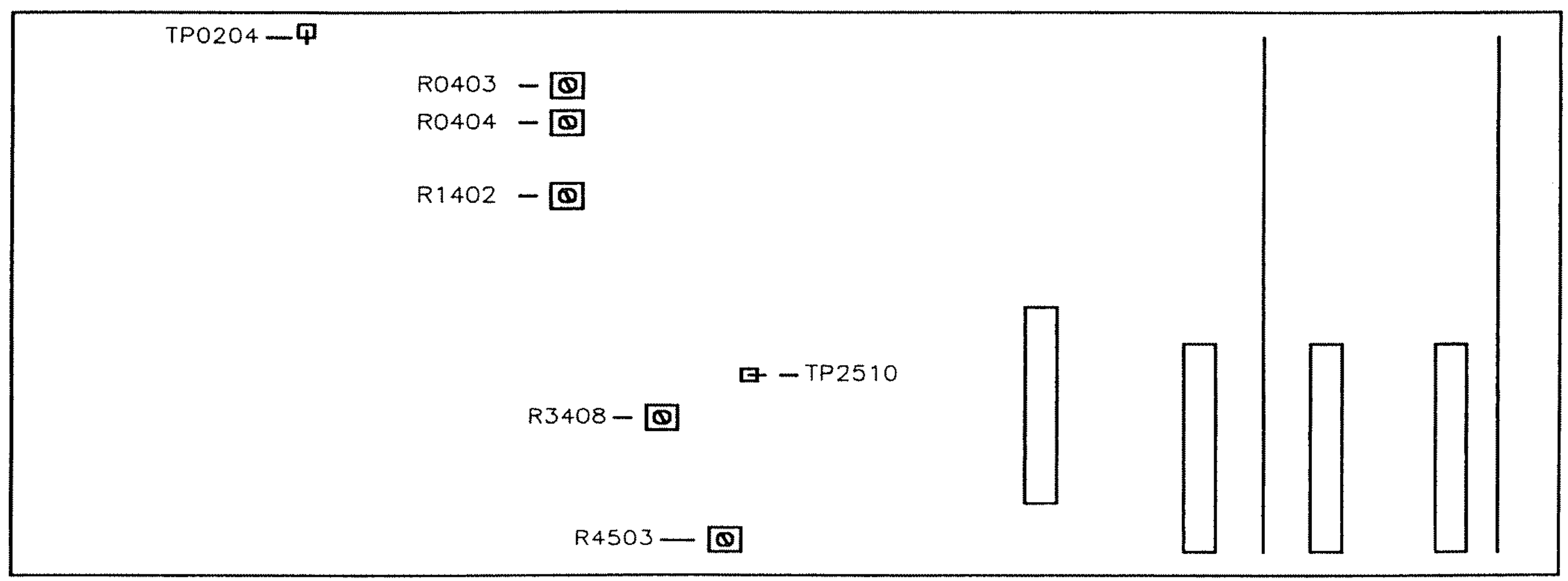
The servo loops derive their information from BP2SIG, which is the bandpass output of the second stage cascaded with the first stage bandreject output in the THD+N mode. BP2SIG contains fundamental information only with very little interference from signal harmonics that may be present. BP2SIG is fed into the inverting amplifier U252, and a gain compensation circuit composed of U243, R2502, and R2504. The dc output from the LEVEL detector, VCOMP, is converted into a control current through R2501 and Q2501 and modulates the transconductance amplifier U243. As the signal level increases within a given range, VCOMP increases. This increases the bias current of U243 which cause more signal to be subtracted from the fixed gain path through R2503. This technique provides approximately constant servo loop gain as the signal varies over 6-7 dB within each input range. D2501, D2502, and R2514 clamp the output of U252 to keep the op-amp within its linear region.

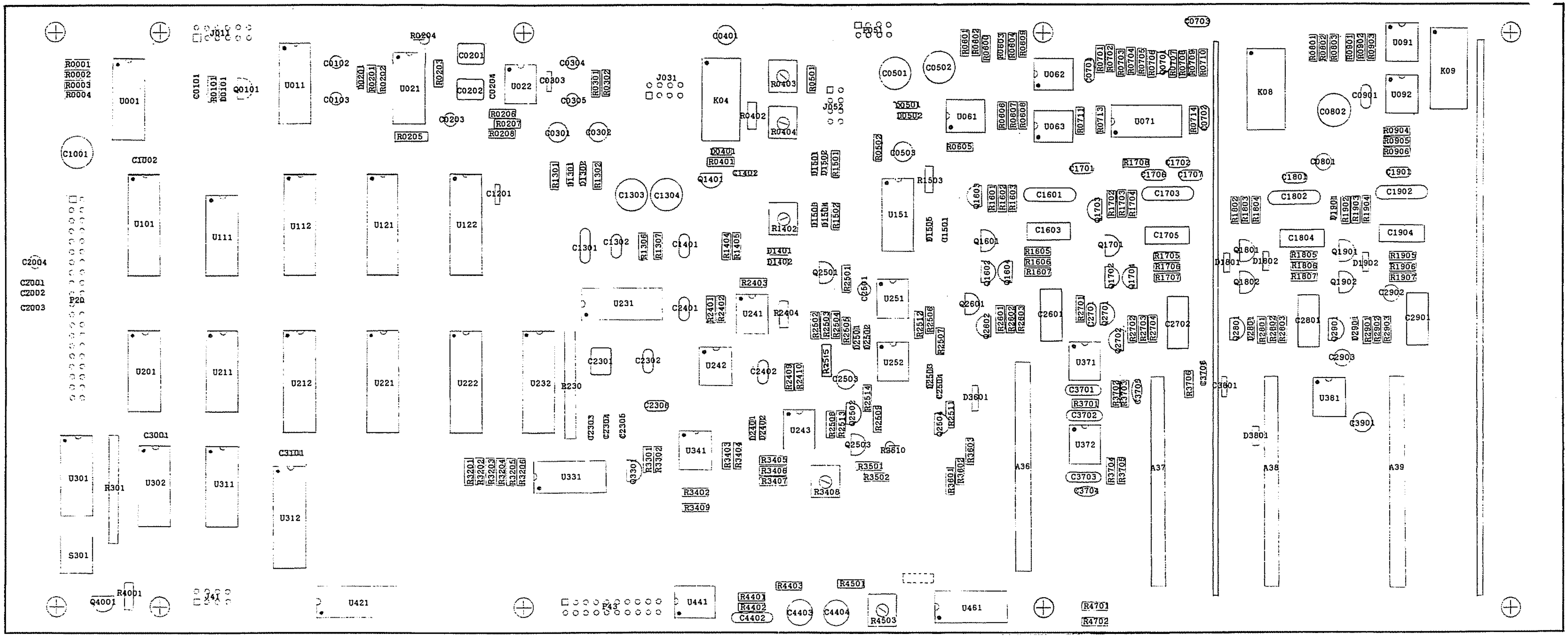
The output of U252 represents an amplified version of the first stage fundamental tuning and nulling errors. U252 is connected to two synchronous demodulators consisting of inverted-mode switching transistors Q2502 and Q3301. Q2502 is driven by a squarewave derived from the BP1SIG which provides the 0 degree phase reference. Q3301 is driven by a square wave derived from LP1SIG which provides the 90 degree phase reference. Quad comparator U151 is used to process the input signals into the demodulator control squarewaves.

Q2502 functions with U241B, R2508, R2510, and R2513 to form the null-loop demodulator. U241B is an integrator amplifying the dc component demodulated from the output of U252. U231 provides switching of the integration time constant to optimize loop speed as a function of fundamental frequency. COMPA and COMPB are the two control lines for this CMOS switch. When both lines are low the switch shorts out the integrator disabling the null loop for the normal bandpass and bandreject modes. Similarly, Q3301 functions with U341A, R3301, R3302, and R3309 to form the tune-loop demodulator. U341A is also an integrator with controllable time constants via U231; and is disabled if both COMPA and COMPB are low.

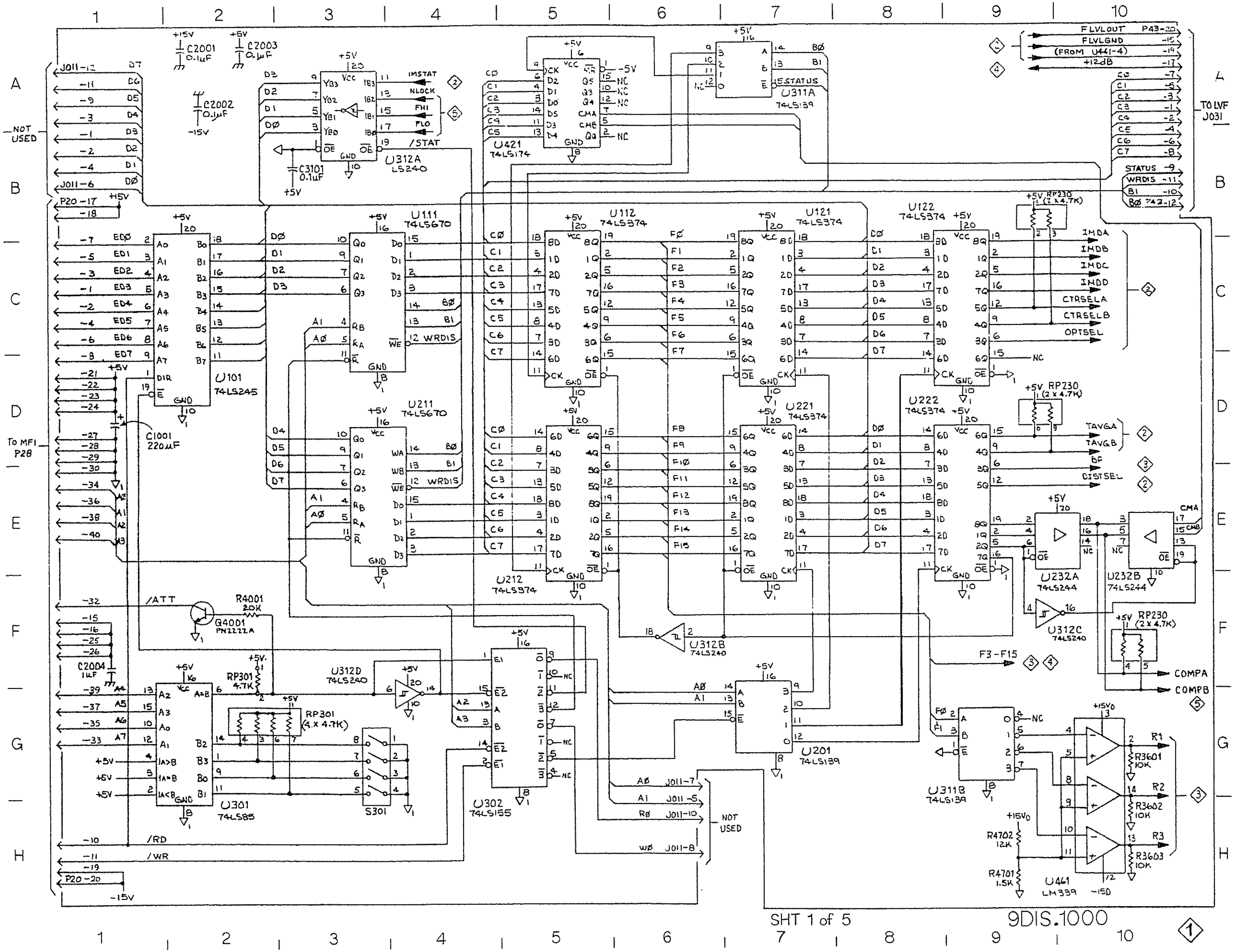
The outputs of the two loop integrators are fed into sample-hold circuits consisting of U251, U241A and U242, U341B respectively. The transconductance amplifiers U251 and U242 are pulsed on by the action of Q2503 and its related components every cycle of the fundamental to sample the respective loop error voltages across C2401 and C2306. This technique results in virtually no ripple in the NULL and TUNE control voltages that could cause THD products in the notch filter.

In the THD+N mode, the NULL and TUNE control voltages vary from approximately -8 to +8 Volts. In the BANDPASS and BANDREJECT modes, the control voltages are maintained near 0 V due to the shorting selection of U231. R1402 and R3408 adjust for op-amp offsets to minimize the fundamental content seen at TP2510 in the THD+N mode.


TP0204
R0403
R0404
R1402
TP2510
R3408
R4503

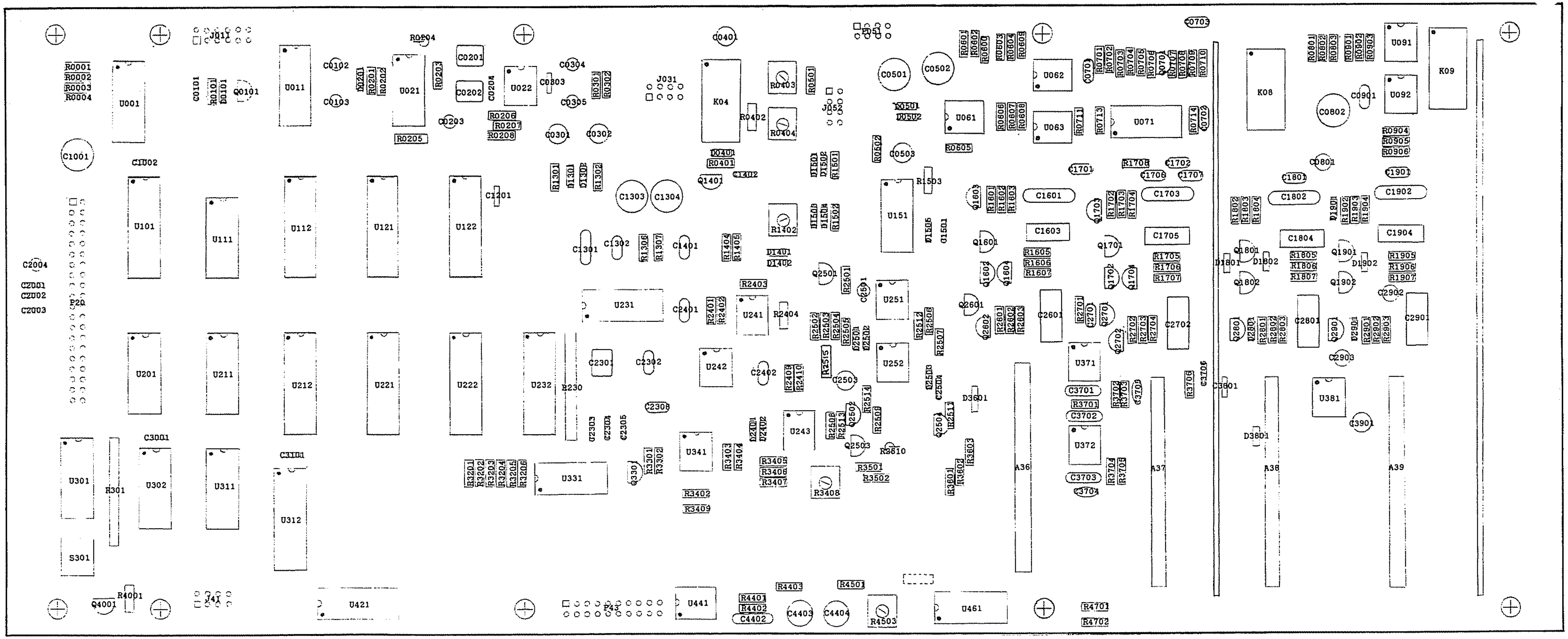


DISTORTION ANALYZER (DIS)

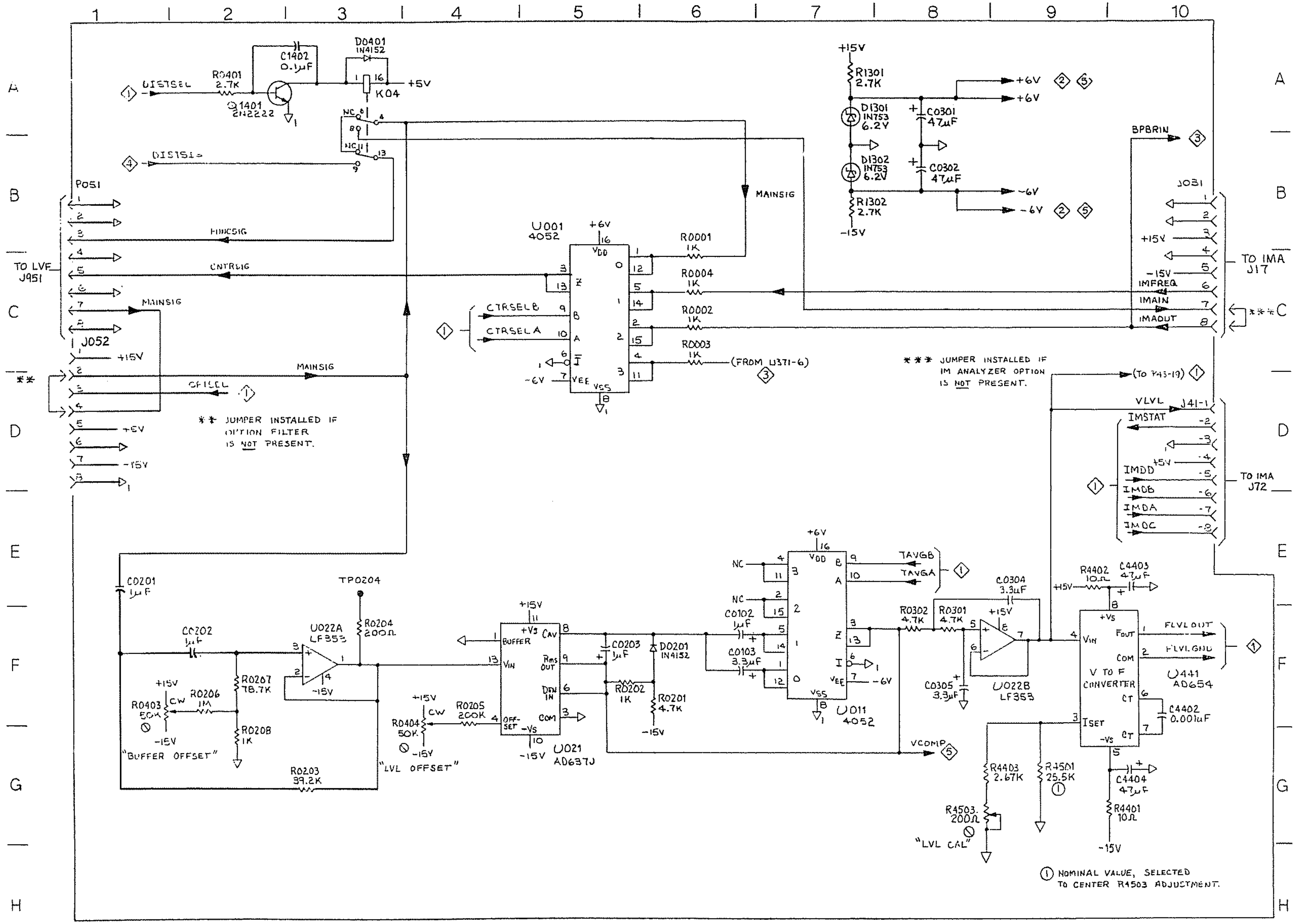


SHT 1 of 5

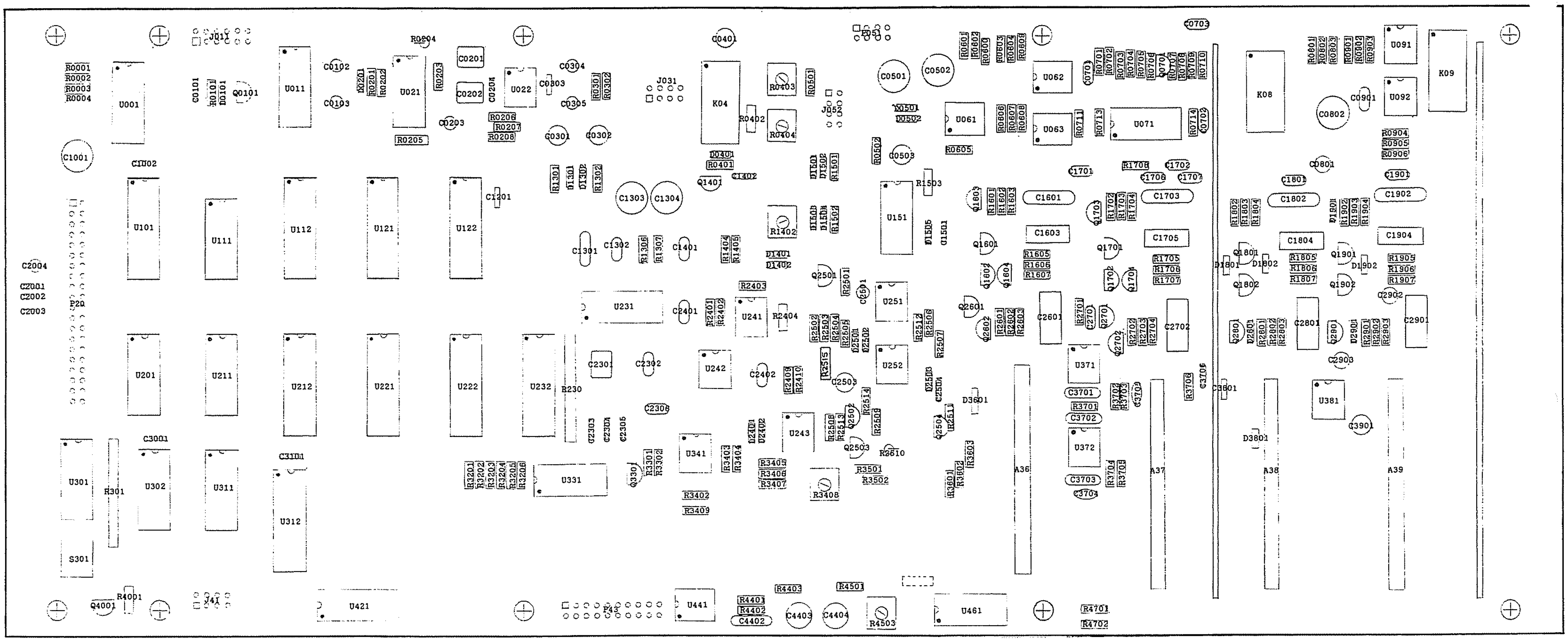
9DIS.1000



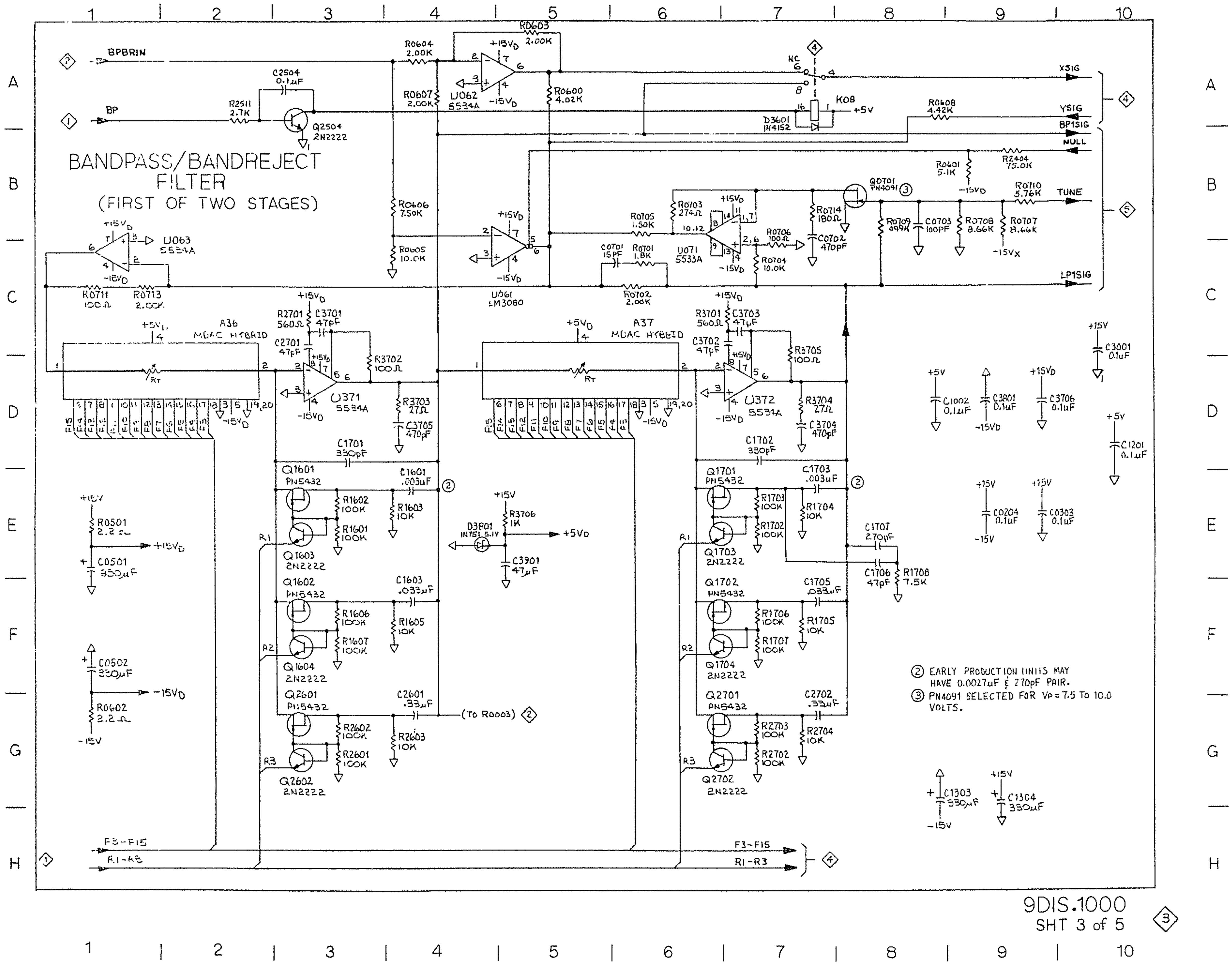
DISTORTION ANALYZER (DIS)



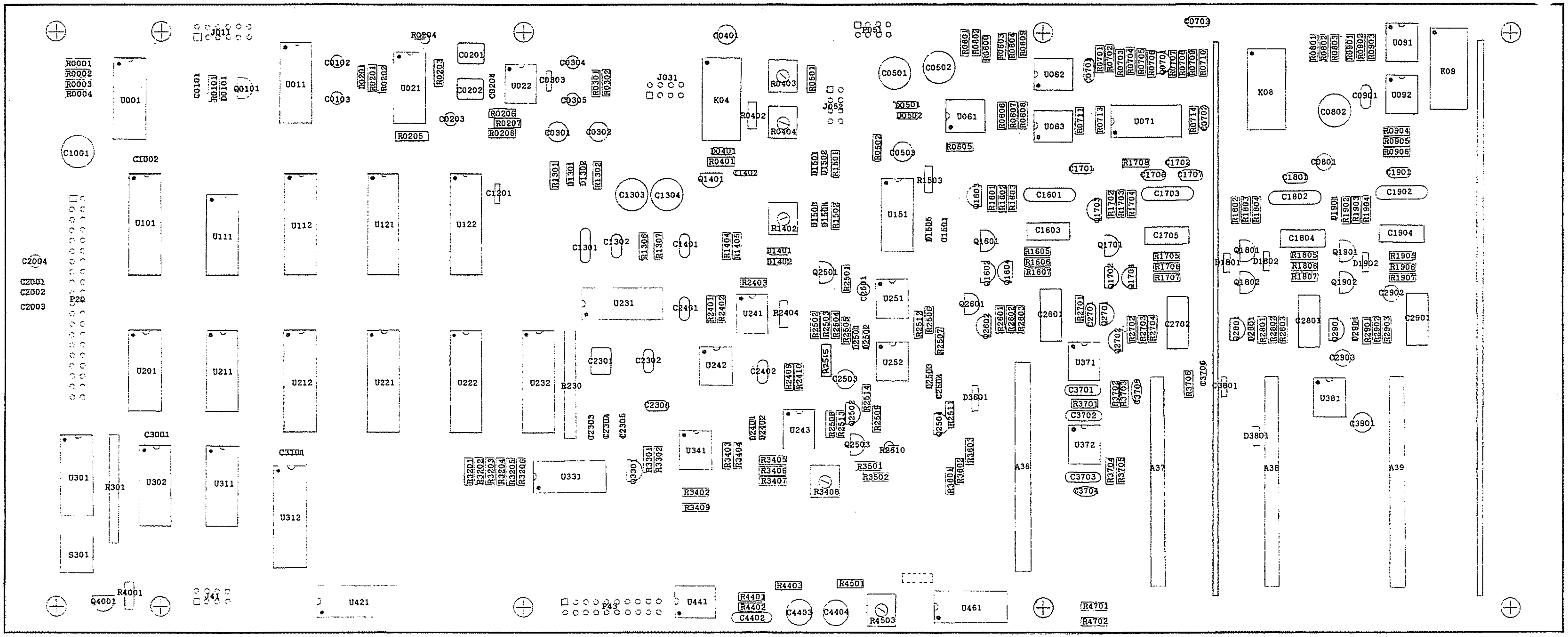
9DIS.1000
SHT 2 of 5



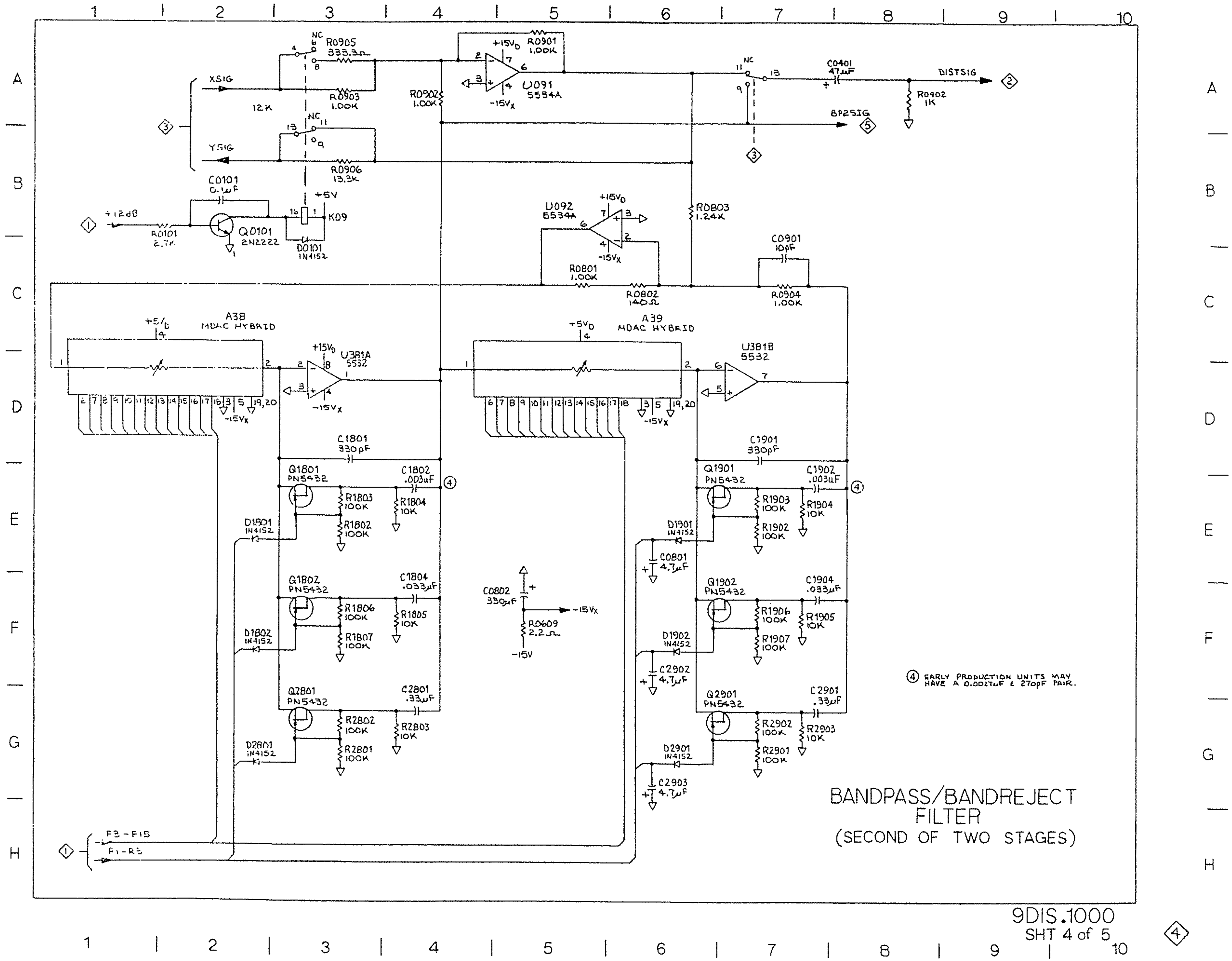
DISTORTION ANALYZER (DIS)



9DIS.1000
SHT 3 of 5

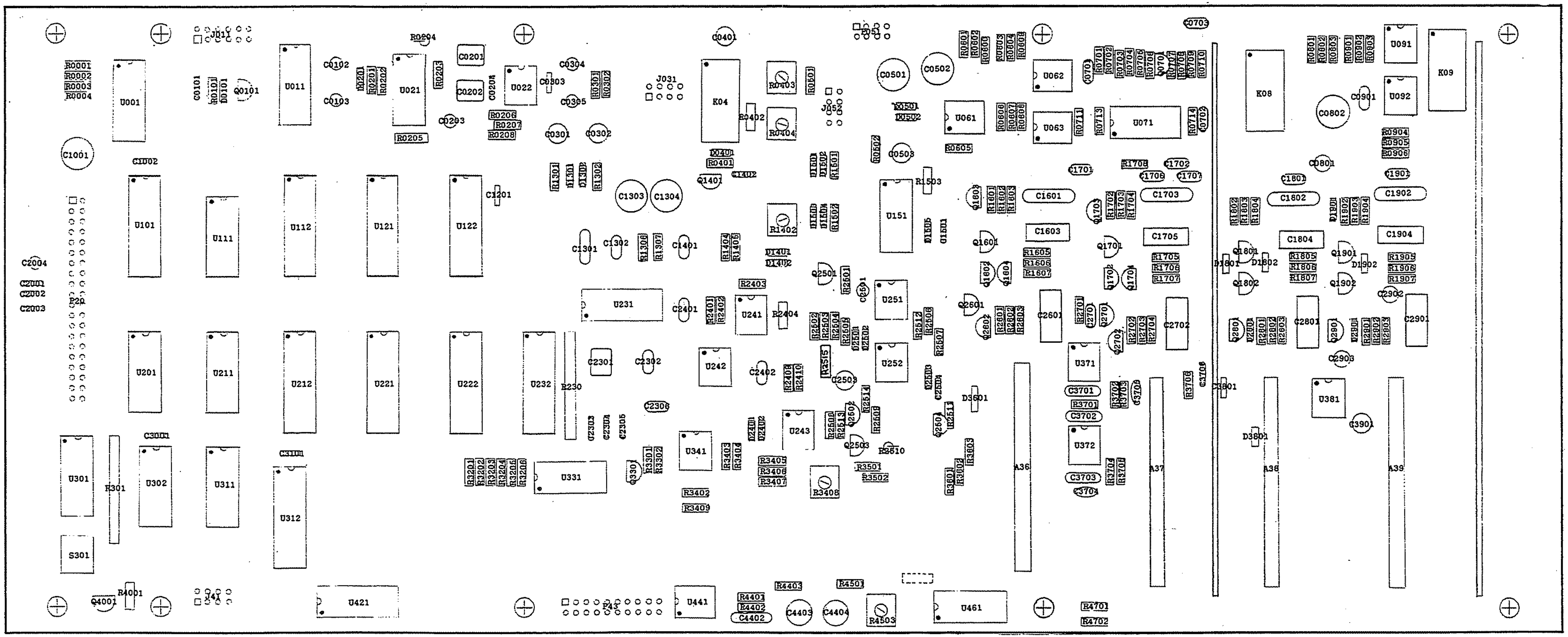


DISTORTION ANALYZER (DIS)

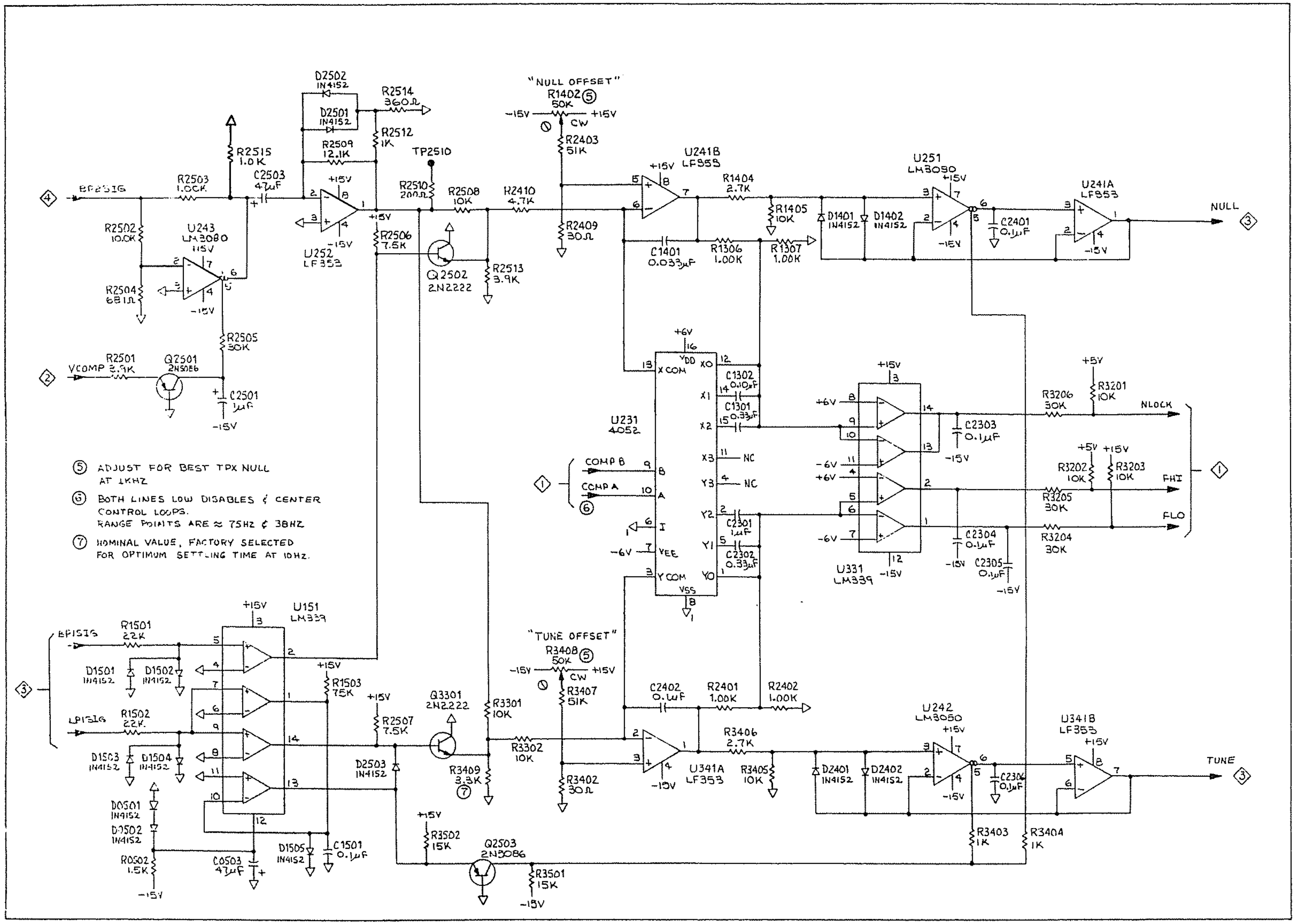


BANDPASS/BANDREJECT FILTER
(SECOND OF TWO STAGES)

9DIS.1000
SHT 4 of 5



DISTORTION ANALYZER (DIS)



9DIS.1000
SHT 5 of 5

Board Loc.	Schematic Loc.	Part Number	Description	
A36	3D1	9DAC.1000	MDAC ECB ASSEMBLY	
A37	3D5	9DAC.1000	MDAC ECB ASSEMBLY	
A38	4C2	9DAC.1000	MDAC ECB ASSEMBLY	
A39	4C5	9DAC.1000	MDAC ECB ASSEMBLY	
C0101	4B2	2172.0104	CAP CERAM 100V 20%	.1uF
C0102	2F6	2952.0105	CAP AL-EL 50V 20%	1uF
C0103	2F6	2952.0335	CAP AL-EL 50V 20%	3.3uF
C0201	2E1	2454.0105	CAP POLYE 50V 5%	1uF
C0202	2F2	2454.0105	CAP POLYE 50V 5%	1uF
C0203	2F5	2952.0105	CAP AL-EL 50V 20%	1uF
C0204	3E9	2172.0104	CAP CERAM 100V 20%	.1uF
C0301	2A8	2932.0476	CAP AL-EL 25V 20%	47uF
C0302	2B8	2932.0476	CAP AL-EL 25V 20%	47uF
C0303	3E9	2172.0104	CAP CERAM 100V 20%	.1uF
C0304	2E9	2952.0335	CAP AL-EL 50V 20%	3.3uF
C0305	2F8	2952.0335	CAP AL-EL 50V 20%	3.3uF
C0401	4A8	2932.0476	CAP AL-EL 25V 20%	47uF
C0501	3E1	2932.0337	CAP AL-EL 25V 20%	330uF
C0502	3F1	2932.0337	CAP AL-EL 25V 20%	330uF
C0503	5H2	2932.0476	CAP AL-EL 25V 20%	47uF
C0701	3C6	2294.0150	CAP MICA 500V 5%	15pF
C0702	3B7	2296.0471	CAP MICA 500V 1%	470pF
C0703	3B8	2296.0101	CAP MICA 500V 1%	100pF
C0801	4E6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C0802	4F5	2932.0337	CAP AL-EL 25V 20%	330uF
C0901	4C7	2294.0100	CAP MICA 500V 5%	10pF
C1001	1D1	2911.0227	CAP AL-EL 10V +80/-20%	220uF
C1002	3D8	2172.0104	CAP CERAM 100V 20%	.1uF
C1201	3D10	2172.0104	CAP CERAM 100V 20%	.1uF
C1301	5D6	2454.0334	CAP POLYE 50V 5%	.33uF
C1302	5D6	2454.0104	CAP POLYE 50V 5%	.1uF
C1303	3G8	2932.0337	CAP AL-EL 25V 20%	330uF
C1304	3G9	2932.0337	CAP AL-EL 25V 20%	330uF
C1401	5C6	2454.0333	CAP POLYE 50V 5%	.033uF
C1402	2A3	2172.0104	CAP CERAM 100V 20%	.1uF
C1501	5H3	2172.0104	CAP CERAM 100V 20%	.1uF
C1601	3E4	2296.0302	CAP MICA 500V 1%	.003uF
C1603	3F4	2675.0333	CAP POLYC 100V 2%	.033uF
C1701	3D3	2296.0331	CAP MICA 500V 1%	330pF
C1702	3D7	2296.0331	CAP MICA 500V 1%	330pF
C1703	3E7	2296.0302	CAP MICA 500V 1%	.003uF
C1705	3F7	2675.0333	CAP POLYC 100V 2%	.033uF
C1706	3E8	2294.0470	CAP MICA 500V 5%	47pF
C1707	3E8	2296.0271	CAP MICA 500V 1%	270pF
C1801	4D3	2296.0331	CAP MICA 500V 1%	330pF
C1802	4E4	2296.0302	CAP MICA 500V 1%	.003uF
C1804	4F4	2675.0333	CAP POLYC 100V 2%	.033uF
C1901	4D7	2296.0331	CAP MICA 500V 1%	330pF
C1902	4E7	2296.0302	CAP MICA 500V 1%	.003uF
C1904	4F7	2675.0333	CAP POLYC 100V 2%	.033uF
C2001	1A2	2172.0104	CAP CERAM 100V 20%	.1uF
C2002	1A2	2172.0104	CAP CERAM 100V 20%	.1uF
C2003	1A2	2172.0104	CAP CERAM 100V 20%	.1uF

Replaceable Electrical Parts List DIS-1

Board	Schematic	Part Number	Description	
C2004	1F1	2952.0105	CAP AL-EL 50V 20%	1uF
C2301	5E6	2454.0105	CAP POLYE 50V 5%	1uF
C2302	5E6	2454.0334	CAP POLYE 50V 5%	.33uF
C2303	5D8	2172.0104	CAP CERAM 100V 20%	.1uF
C2304	5E8	2172.0104	CAP CERAM 100V 20%	.1uF
C2305	5E8	2172.0104	CAP CERAM 100V 20%	.1uF
C2306	5G8	2454.0104	CAP POLYE 50V 5%	.1uF
C2401	5C8	2454.0104	CAP POLYE 50V 5%	.1uF
C2402	5G6	2454.0104	CAP POLYE 50V 5%	.1uF
C2501	5D2	2952.0105	CAP AL-EL 50V 20%	1uF
C2503	5B2	2932.0476	CAP AL-EL 25V 20%	47uF
C2504	3A3	2172.0104	CAP CERAM 100V 20%	.1uF
C2601	3G4	2675.0334	CAP POLYC 100V 2%	.33uF
C2701	3C3	2294.0470	CAP MICA 500V 5%	47pF
C2702	3G7	2675.0334	CAP POLYC 100V 2%	.33uF
C2801	4G4	2675.0334	CAP POLYC 100V 2%	.33uF
C2901	4G7	2675.0334	CAP POLYC 100V 2%	.33uF
C2902	4F6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C2903	4G6	2942.0475	CAP AL-EL 35V 20%	4.7uF
C3001	3C10	2172.0104	CAP CERAM 100V 20%	.1uF
C3101	1B3	2172.0104	CAP CERAM 100V 20%	.1uF
C3701	3C3	2294.0470	CAP MICA 500V 5%	47pF
C3702	3C7	2294.0470	CAP MICA 500V 5%	47pF
C3703	3C7	2294.0470	CAP MICA 500V 5%	47pF
C3704	3D7	2172.0471	CAP CERAM 100V 20%	470pF
C3705	3D4	2172.0471	CAP CERAM 100V 20%	470pF
C3706	3D9	2172.0104	CAP CERAM 100V 20%	.1uF
C3801	3D9	2172.0104	CAP CERAM 100V 20%	.1uF
C3901	3E5	2932.0476	CAP AL-EL 25V 20%	47uF
C4402	2F10	2296.0102	CAP MICA 500V 1%	.001uF
C4403	2E10	2932.0476	CAP AL-EL 25V 20%	47uF
C4404	2G10	2932.0476	CAP AL-EL 25V 20%	47uF
D0101	4C3	3110.4152	DIODE SIGNAL	4152
D0201	2F6	3110.4152	DIODE SIGNAL	4152
D0401	2A3	3110.4152	DIODE SIGNAL	4152
D0501	5G2	3110.4152	DIODE SIGNAL	4152
D0502	5H2	3110.4152	DIODE SIGNAL	4152
D1301	2A7	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
D1302	2B7	3130.0062	DIODE ZEN 1/2W 5% 6.2V	1N753
D1401	5C7	3110.4152	DIODE SIGNAL	4152
D1402	5C7	3110.4152	DIODE SIGNAL	4152
D1501	5F1	3110.4152	DIODE SIGNAL	4152
D1502	5F2	3110.4152	DIODE SIGNAL	4152
D1503	5G1	3110.4152	DIODE SIGNAL	4152
D1504	5G2	3110.4152	DIODE SIGNAL	4152
D1505	5H3	3110.4152	DIODE SIGNAL	4152
D1801	4E2	3110.4152	DIODE SIGNAL	4152
D1802	4F2	3110.4152	DIODE SIGNAL	4152
D1901	4E6	3110.4152	DIODE SIGNAL	4152
D1902	4F6	3110.4152	DIODE SIGNAL	4152
D2401	5G7	3110.4152	DIODE SIGNAL	4152
D2402	5G7	3110.4152	DIODE SIGNAL	4152
D2501	5B3	3110.4152	DIODE SIGNAL	4152

Board Loc.	Schematic Loc.	Part Number	Description	
D2502	5B3	3110.4152	DIODE SIGNAL	4152
D2503	5G4	3110.4152	DIODE SIGNAL	4152
D2801	4G2	3110.4152	DIODE SIGNAL	4152
D2901	4G6	3110.4152	DIODE SIGNAL	4152
D3601	3A7	3110.4152	DIODE SIGNAL	4152
D3801	3E4	3130.0051	DIODE ZEN 1/2W 5% 5.1V	1N751
E021	---	4232.0014	SOCKET IC DIP	14 PIN
ECB01	---	6200.DIS1	ECB 2 LAYER 6 X15	DIS-1
J031	2B10	4221.1008	JACK PC 2 X .1	8 PIN
J052	2C1	4221.1008	JACK PC 2 X .1	8 PIN
J41	2D10	4221.1008	JACK PC 2 X .1	8 PIN
K04	2A3	4530.0001	RELAY PC	DPDT
K08	3A7	4530.0001	RELAY PC	DPDT
K09	4B3	4530.0001	RELAY PC	DPDT
P051	2B1	4221.0072.1	PLUG PC 2X.1 X.83	72 PIN
P20	1B1	4151.1740	CABLE ASSY .05 RBN 17	40 COND
P43	1A10	4221.0072.1	PLUG PC 2X.1 X.83	72 PIN
Q0101	4B2	3211.2222	XSTR NPN TO92	PN2222A
Q0701	3B8	3214.4091.H	XSTR FET TO92 HI Vp	PN4091
Q1401	2A2	3211.2222	XSTR NPN TO92	PN2222A
Q1601	3E3	3214.5432	XSTR FET TO92	PN5432
Q1602	3F3	3214.5432	XSTR FET TO92	PN5432
Q1603	3E3	3211.2222	XSTR NPN TO92	PN2222A
Q1604	3F3	3211.2222	XSTR NPN TO92	PN2222A
Q1701	3E6	3214.5432	XSTR FET TO92	PN5432
Q1702	3F6	3214.5432	XSTR FET TO92	PN5432
Q1703	3E6	3211.2222	XSTR NPN TO92	PN2222A
Q1704	3F6	3211.2222	XSTR NPN TO92	PN2222A
Q1801	4E3	3214.5432	XSTR FET TO92	PN5432
Q1802	4F3	3214.5432	XSTR FET TO92	PN5432
Q1901	4E6	3214.5432	XSTR FET TO92	PN5432
Q1902	4F6	3214.5432	XSTR FET TO92	PN5432
Q2501	5D2	3211.5086	XSTR PNP TO92	PN5086
Q2502	5C4	3211.2222	XSTR NPN TO92	PN2222A
Q2503	5H4	3211.5086	XSTR PNP TO92	PN5086
Q2504	3A3	3211.2222	XSTR NPN TO92	PN2222A
Q2601	3G3	3214.5432	XSTR FET TO92	PN5432
Q2602	3G3	3211.2222	XSTR NPN TO92	PN2222A
Q2701	3G6	3214.5432	XSTR FET TO92	PN5432
Q2702	3G6	3211.2222	XSTR NPN TO92	PN2222A
Q2801	4G3	3214.5432	XSTR FET TO92	PN5432
Q2901	4G6	3214.5432	XSTR FET TO92	PN5432
Q3301	5G4	3211.2222	XSTR NPN TO92	PN2222A
Q4001	1F2	3211.2222	XSTR NPN TO92	PN2222A
R0001	2C6	1214.0102	RES 1/4W C FLM 5%	1K
R0002	2C6	1214.0102	RES 1/4W C FLM 5%	1K
R0003	2C6	1214.0102	RES 1/4W C FLM 5%	1K

Replaceable Electrical Parts List DIS-1

Board	Schematic	Part Number	Description	
R0004	2C6	1214.0102	RES 1/4W C FLM 5%	1K
R0101	4B2	1214.0272	RES 1/4W C FLM 5%	2.7K
R0201	2F6	1214.0472	RES 1/4W C FLM 5%	4.7K
R0202	2F5	1214.0102	RES 1/4W C FLM 5%	1K
R0203	2G3	1136.3922	RES 1/8W M FLM 1%	39.2K
R0204	2F3	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R0205	2F4	1214.0204	RES 1/4W C FLM 5%	200K
R0206	2F2	1214.0105	RES 1/4W C FLM 5%	1M
R0207	2F2	1136.7872	RES 1/8W M FLM 1%	78.7K
R0208	2G2	1214.0102	RES 1/4W C FLM 5%	1K
R0301	2F8	1214.0472	RES 1/4W C FLM 5%	4.7K
R0302	2F8	1214.0472	RES 1/4W C FLM 5%	4.7K
R0401	2A2	1214.0272	RES 1/4W C FLM 5%	2.7K
R0402	4A8	1214.0102	RES 1/4W C FLM 5%	1K
R0403	2F1	4412.0503	POT TRIM PC ENC	50K
R0404	2F4	4412.0503	POT TRIM PC ENC	50K
R0501	3E1	1214.0229	RES 1/4W C FLM 5%	2.2
R0502	5H2	1214.0152	RES 1/4W C FLM 5%	1.5K
R0600	3A5	1136.4021	RES 1/8W M FLM 1%	4.02K
R0601	3B9	1214.0512	RES 1/4W C FLM 5%	5.1K
R0602	3G1	1214.0229	RES 1/4W C FLM 5%	2.2
R0603	3A5	1139.2001	RES 1/8W M FLM .1%	2.00K
R0604	3A4	1139.2001	RES 1/8W M FLM .1%	2.00K
R0605	3C4	1136.1009	RES 1/8W M FLM 1%	10.0
R0606	3B4	1136.7501	RES 1/8W M FLM 1%	7.50K
R0607	3A4	1139.2001	RES 1/8W M FLM .1%	2.00K
R0608	3A8	1136.4421	RES 1/8W M FLM 1%	4.42K
R0609	4F5	1214.0229	RES 1/4W C FLM 5%	2.2
R0701	3C6	1214.0182	RES 1/4W C FLM 5%	1.8K
R0702	3C6	1139.2001	RES 1/8W M FLM .1%	2.00K
R0703	3B6	1136.2740	RES 1/8W M FLM 1%	274
R0704	3C7	1136.1002	RES 1/8W M FLM 1%	10.0K
R0705	3B6	1136.1501	RES 1/8W M FLM 1%	1.50K
R0706	3C7	1136.1000	RES 1/8W M FLM 1%	100
R0707	3B9	1136.8661	RES 1/8W M FLM 1%	8.66K
R0708	3B9	1136.8661	RES 1/8W M FLM 1%	8.66K
R0709	3B8	1136.4993	RES 1/8W M FLM 1%	499K
R0710	3B9	1136.5761	RES 1/8W M FLM 1%	5.76K
R0711	3C1	1136.1000	RES 1/8W M FLM 1%	100
R0713	3C1	1139.2001	RES 1/8W M FLM .1%	2.00K
R0714	3B7	1214.0181	RES 1/4W C FLM 5%	180
R0801	4C5	1139.1001	RES 1/8W M FLM .1%	1.00K
R0802	4C6	1136.1400	RES 1/8W M FLM 1%	140
R0803	4B6	1136.1241	RES 1/8W M FLM 1%	1.24K
R0901	4A5	1139.1001	RES 1/8W M FLM .1%	1.00K
R0902	4A4	1139.1001	RES 1/8W M FLM .1%	1.00K
R0903	4A3	1139.1001	RES 1/8W M FLM .1%	1.00K
R0904	4C7	1139.1001	RES 1/8W M FLM .1%	1.00K
R0905	4A3	1139.3330	RES 1/8W M FLM .1%	333.3
R0906	4B3	1136.1332	RES 1/8W M FLM 1%	13.3K
R1301	2A7	1214.0272	RES 1/4W C FLM 5%	2.7K
R1302	2B7	1214.0272	RES 1/4W C FLM 5%	2.7K
R1306	5C6	1136.1001	RES 1/8W M FLM 1%	1.00K
R1307	5C7	1136.1001	RES 1/8W M FLM 1%	1.00K

Board Loc.	Schematic Loc.	Part Number	Description	
R1402	5B5	4412.0503	POT TRIM PC ENC	50K
R1404	5B6	1214.0272	RES 1/4W C FLM 5%	2.7K
R1405	5C7	1214.0103	RES 1/4W C FLM 5%	10K
R1501	5F1	1214.0223	RES 1/4W C FLM 5%	22K
R1502	5G1	1214.0223	RES 1/4W C FLM 5%	22K
R1503	5F3	1214.0753	RES 1/4W C FLM 5%	75K
R1601	3E3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1602	3E3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1603	3E4	1214.0103	RES 1/4W C FLM 5%	10K
R1605	3F4	1214.0103	RES 1/4W C FLM 5%	10K
R1606	3F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1607	3F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1702	3E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1703	3E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1704	3E7	1214.0103	RES 1/4W C FLM 5%	10K
R1705	3F7	1214.0103	RES 1/4W C FLM 5%	10K
R1706	3F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1707	3F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1708	3E8	1214.0752	RES 1/4W C FLM 5%	7.5K
R1802	4E3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1803	4E3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1804	4E4	1214.0103	RES 1/4W C FLM 5%	10K
R1805	4F4	1214.0103	RES 1/4W C FLM 5%	10K
R1806	4F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1807	4F3	1214.0104	RES 1/4W/C/FLM 5%	100K
R1902	4E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1903	4E7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1904	4E7	1214.0103	RES 1/4W C FLM 5%	10K
R1905	4F7	1214.0103	RES 1/4W C FLM 5%	10K
R1906	4F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R1907	4F7	1214.0104	RES 1/4W/C/FLM 5%	100K
R230	1B9,1D9,1F10	1984.9472	RES NET SIP 5%	9 X 4.7K
R2401	5G6	1136.1001	RES 1/8W M FLM 1%	1.00K
R2402	5G7	1136.1001	RES 1/8W M FLM 1%	1.00K
R2403	5B5	1214.0513	RES 1/4W C FLM 5%	51K
R2404	3B9	1136.7502	RES 1/8W M FLM 1%	75.0K
R2409	5C5	1214.0300	RES 1/4W C FLM 5%	30
R2410	5C5	1214.0472	RES 1/4W C FLM 5%	4.7K
R2501	5D1	1214.0392	RES 1/4W C FLM 5%	3.9K
R2502	5C1	1136.1002	RES 1/8W M FLM 1%	10.0K
R2503	5B2	1136.1001	RES 1/8W M FLM 1%	1.00K
R2504	5C1	1136.6810	RES 1/8W M FLM 1%	681
R2505	5D2	1214.0303	RES 1/4W C FLM 5%	30K
R2506	5C3	1214.0752	RES 1/4W C FLM 5%	7.5K
R2507	5G3	1214.0752	RES 1/4W C FLM 5%	7.5K
R2508	5C4	1214.0103	RES 1/4W C FLM 5%	10K
R2509	5B3	1136.1212	RES 1/8W M FLM 1%	12.1K
R2510	5B4	1214.0201.1	RES 1/4W C FLM 5% VERT	200
R2511	3A2	1214.0272	RES 1/4W C FLM 5%	2.7K
R2512	5B3	1214.0102	RES 1/4W C FLM 5%	1K
R2513	5C4	1214.0392	RES 1/4W C FLM 5%	3.9K
R2514	5B4	1214.0361	RES 1/4W C FLM 5%	360
R2515	5B2	1214.0102	RES 1/4W C FLM 5%	1K
R2601	3G3	1214.0104	RES 1/4W/C/FLM 5%	100K

Replaceable Electrical Parts List DIS-1

Board	Schematic	Part Number	Description	
R2602	3G3	1214.0104	RES 1/4W/C/FLM 5%	100K
R2603	3G4	1214.0103	RES 1/4W C FLM 5%	10K
R2701	3C3	1214.0561	RES 1/4W C FLM 5%	560
R2702	3G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2703	3G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2704	3G7	1214.0103	RES 1/4W C FLM 5%	10K
R2801	4G3	1214.0104	RES 1/4W/C/FLM 5%	100K
R2802	4G3	1214.0104	RES 1/4W/C/FLM 5%	100K
R2803	4G4	1214.0103	RES 1/4W C FLM 5%	10K
R2901	4G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2902	4G7	1214.0104	RES 1/4W/C/FLM 5%	100K
R2903	4G7	1214.0103	RES 1/4W C FLM 5%	10K
R301	1F2,1G2	1984.9472	RES NET SIP 5%	9 X 4.7K
R3201	5D9	1214.0103	RES 1/4W C FLM 5%	10K
R3202	5E9	1214.0103	RES 1/4W C FLM 5%	10K
R3203	5E9	1214.0103	RES 1/4W C FLM 5%	10K
R3204	5E9	1214.0303	RES 1/4W C FLM 5%	30K
R3205	5E9	1214.0303	RES 1/4W C FLM 5%	30K
R3206	5D9	1214.0303	RES 1/4W C FLM 5%	30K
R3301	5G4	1214.0103	RES 1/4W C FLM 5%	10K
R3302	5G5	1214.0103	RES 1/4W C FLM 5%	10K
R3402	5G5	1214.0300	RES 1/4W C FLM 5%	30
R3403	5H8	1214.0102	RES 1/4W C FLM 5%	1K
R3404	5H9	1214.0102	RES 1/4W C FLM 5%	1K
R3405	5G7	1214.0103	RES 1/4W C FLM 5%	10K
R3406	5G6	1214.0272	RES 1/4W C FLM 5%	2.7K
R3407	5F5	1214.0513	RES 1/4W C FLM 5%	51K
R3408	5F5	4412.0503	POT TRIM PC ENC	50K
R3409	5G4	1214.0332	RES 1/4W C FLM 5%	3.3K
R3501	5H5	1214.0153	RES 1/4W C FLM 5%	15K
R3502	5H4	1214.0153	RES 1/4W C FLM 5%	15K
R3601	1G10	1214.0103	RES 1/4W C FLM 5%	10K
R3602	1H10	1214.0103	RES 1/4W C FLM 5%	10K
R3603	1H10	1214.0103	RES 1/4W C FLM 5%	10K
R3701	3C7	1214.0561	RES 1/4W C FLM 5%	560
R3702	3D3	1214.0101	RES 1/4W C FLM 5%	100
R3703	3D4	1214.0270	RES 1/4W C FLM 5%	27
R3704	3D7	1214.0270	RES 1/4W C FLM 5%	27
R3705	3C7	1214.0101	RES 1/4W C FLM 5%	100
R3706	3E5	1214.0102	RES 1/4W C FLM 5%	1K
R4001	1F2	1214.0203	RES 1/4W C FLM 5%	20K
R4401	2G9	1214.0100	RES 1/4W C FLM 5%	10
R4402	2E9	1214.0100	RES 1/4W C FLM 5%	10
R4403	2G8	1136.2671	RES 1/8W M FLM 1%	2.67K
R4501	2G9	1136.2552	RES 1/8W M FLM 1%	25.5K
R4503	2G8	4412.0201	POT TRIM PC ENC	200
R4701	1H9	1214.0152	RES 1/4W C FLM 5%	1.5K
R4702	1H9	1214.0123	RES 1/4W C FLM 5%	12K
S301	1G3	4310.0004	SWITCH DIP	4 POLE
U001	2C5	3321.4052	MULTIPLEX 4X DIFF	4052
U011	2E7	3321.4052	MULTIPLEX 4X DIFF	4052
U021	2F5	3441.0637	CONVERTER RMS TO DC	AD637J

Board Loc.	Schematic Loc.	Part Number	Description	
U022	2F3,2F8	3412.0353	OP AMP DUAL	TL072/LF353
U061	3C5	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U062	3A4	3411.5534	OP AMP SINGLE	5534A
U063	3C1	3411.5534	OP AMP SINGLE	5534A
U071	3B7	3412.5533	OP AMP DUAL	5533A
U091	4A5	3411.5534	OP AMP SINGLE	5534A
U092	4B5	3411.5534	OP AMP SINGLE	5534A
U101	1C2	3313.0245	TRANSCVR 8X TRI-STATE	74LS245
U111	1C3	3313.0670	REGISTER FILE 4X4	74LS670
U112	1C5	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U121	1C7	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U122	1C9	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U151	5F2	3424.0339	COMPARATOR QUAD	LM339
U201	1G7	3313.0139	DECODER 2 X 2-LN/4-LN	74LS139
U211	1D3	3313.0670	REGISTER FILE 4X4	74LS670
U212	1D5	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U221	1D7	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U222	1D9	3313.0374	FLIP-FLOP 8X D TRI-ST	74LS374
U231	5D6	3321.4052	MULTIPLEX 4X DIFF	4052
U232	1E9,1E10	3313.0244	BUFFER 8X TRI-STATE	74LS244
U241	5B6,5C9	3412.0353	OP AMP DUAL	TL072/LF353
U242	5G8	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U243	5C2	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U251	5C8	3411.3080	OP AMP TRANSCONDUCTANCE	3080
U252	5C3	3412.0353	OP AMP DUAL	TL072/LF353
U301	1G2	3313.0085	COMPARATOR 4-BIT MAG	74LS85
U302	1F5	3313.0155	DECODER 2 X 2-LN/4-LN	74LS155
U311	1A7,1G9	3313.0139	DECODER 2 X 2-LN/4-LN	74LS139
U312	1A3,1F4,1F6,1F9	3313.0240	BUFFER 8X INV TRI-ST	74LS240
U331	5D7	3424.0339	COMPARATOR QUAD	LM339
U341	5G6,5G9	3412.0353	OP AMP DUAL	TL072/LF353
U371	3D3	3411.5534	OP AMP SINGLE	5534A
U372	3D7	3411.5534	OP AMP SINGLE	5534A
U381	4D3,4D7	3412.5532	OP AMP DUAL	5532
U421	1A5	3313.0174	FLIP-FLOP 6X D W/CLR	74LS174
U441	2F9	3441.0654	CONVERTER VOLT TO FREQ	AD654J
U461	1G10	3424.0339	COMPARATOR QUAD	LM339
X80	—	7160.0001	SHIELD ECB	2X5.75
X90	—	7160.0001	SHIELD ECB	2X5.75